USB 3.2 COMPLIANCE TESTING

Pascal Berten, Eurofins Digital Testing, Senior Test Engineer
Johannes Ganzert, Rohde&Schwarz, Senior Application Engineer, Oscilloscopes

ROHDE&SCHWARZ
Make ideas real

AGENDA

- Introduction (Johannes Ganzert)

- Details about USB Compliance Testing (Pascal Berten)
  - More than 20 years of experience in USB testing at Eurofins Digital Testing Belgium
  - Certified over 1000 products
  - Often help customers debug and get them through compliance
  - Developed several USB test fixtures

- Demonstration with the R&S RTP164 Oscilloscope (Johannes Ganzert)

- Summary

INTRODUCTION

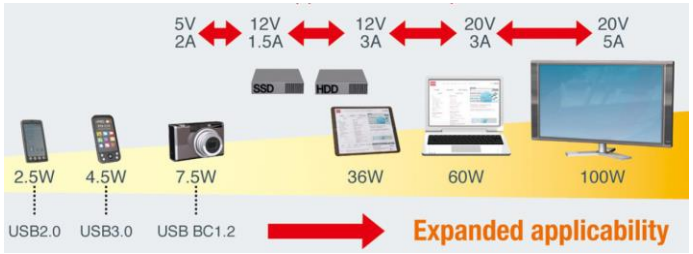
OVERVIEW

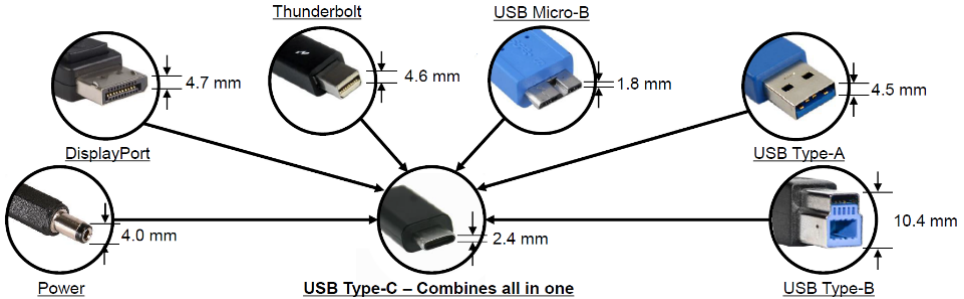
- Universal Serial Bus (USB), introduced in 1996
  - Wired connection for computer and peripherals
- USB Implementers Forum, Inc. (usb.org)
  - Standard body
- Growing application areas
  - Consumer electronics, IT & telecom devices, automobiles, medical devices and much more

Apple iMac G3 (1998)

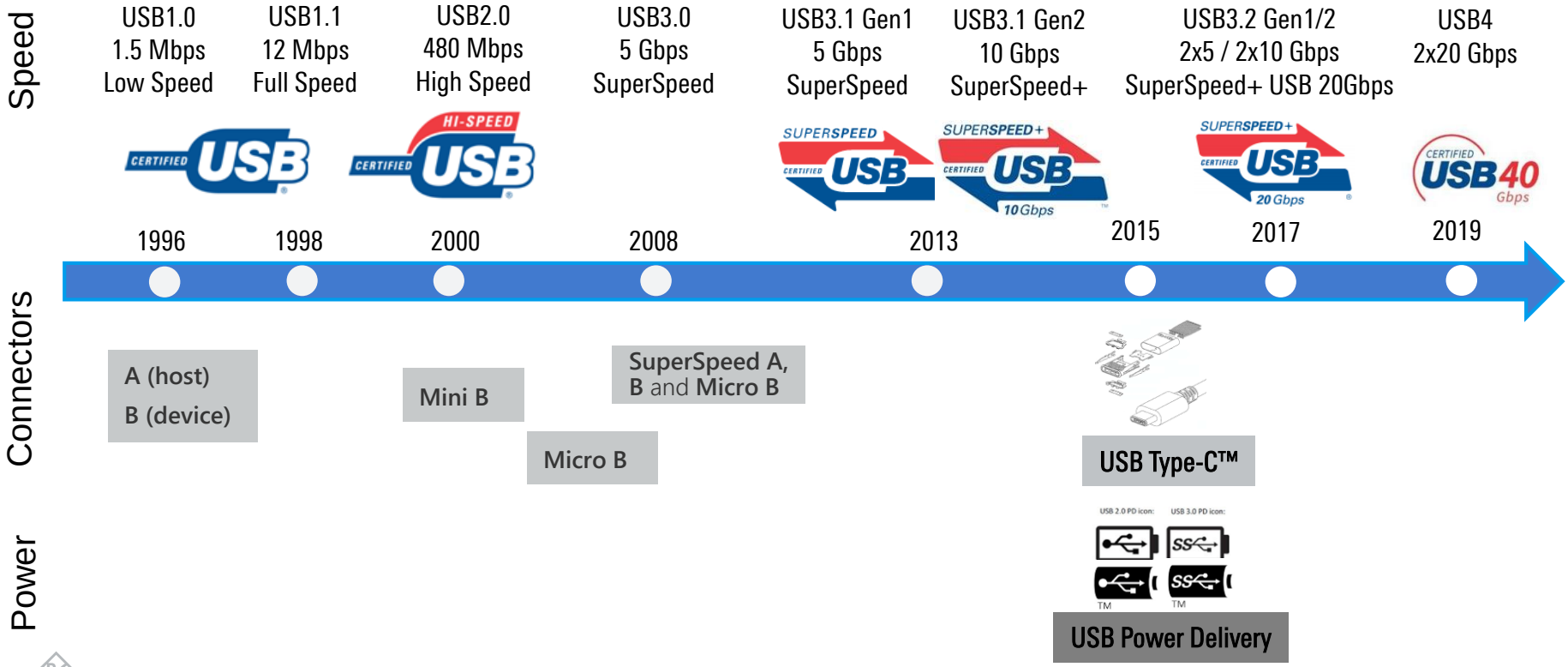
TRENDS

- **More data:**
  - All industries are impacted
  - ➢ *USB 3.2/ 4 specifications*
- **Flexible power:**
  - Power supply and charging
  - ➢ *USB-PD specification*
- **Unified connector:**
  - Applicable beyond USB
  - ➢ *USB Type-C™ specification*





THE EVOLUTION OF THE STANDARD



USB ECOSYSTEM

A to Type-C

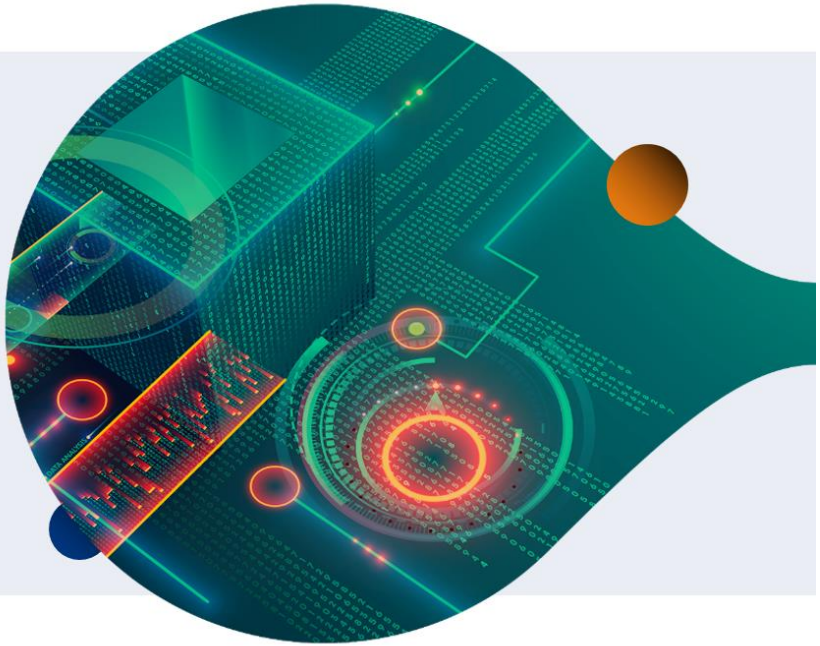
A to Std B

A to µB

Goal of USB.org:
Any certified host works with any certified hub or device.

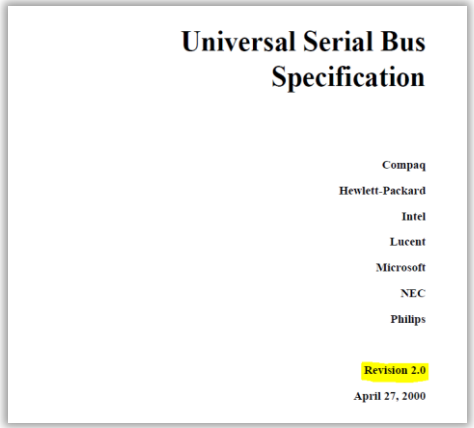
eurofins | Digital Testing

USB-IF Compliance USB 2.0 Physical Layer Testing

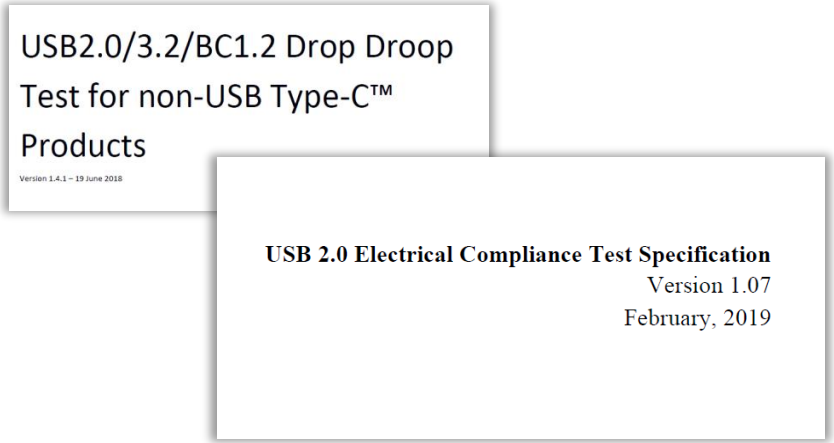


USB 2.0 COMPLIANCE TESTING

USB 2.0 ELECTRICAL COMPLIANCE



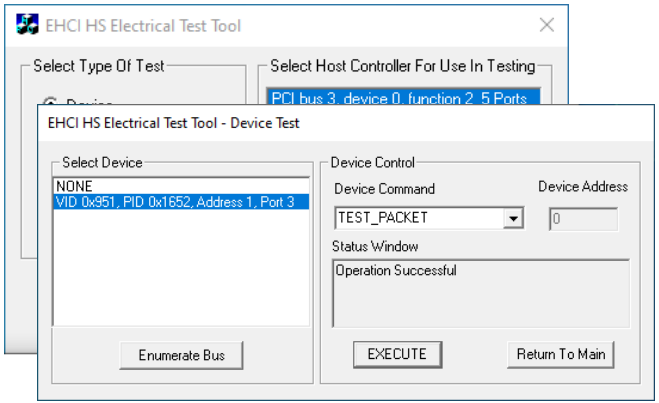
USB 2.0 Spec + ECN



https://compliance.usb.org/

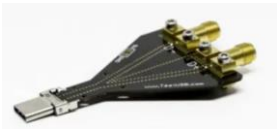
USB-IF USB 2.0 Electrical Compliance

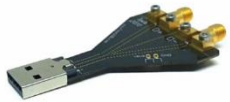
SETUP REQUIREMENTS

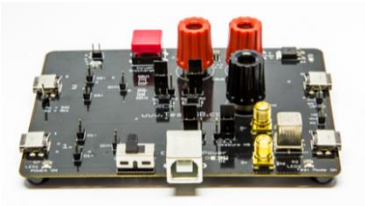


USBHSETT

Use the official USB-IF fixtures and correct cable length



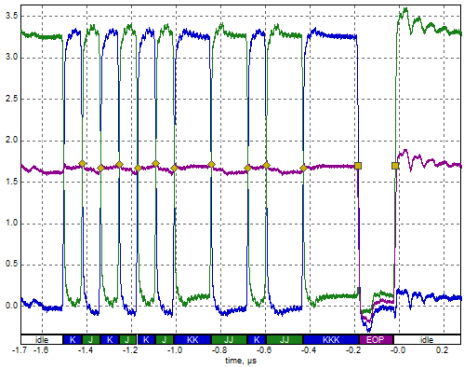




www.fixturesolution.com

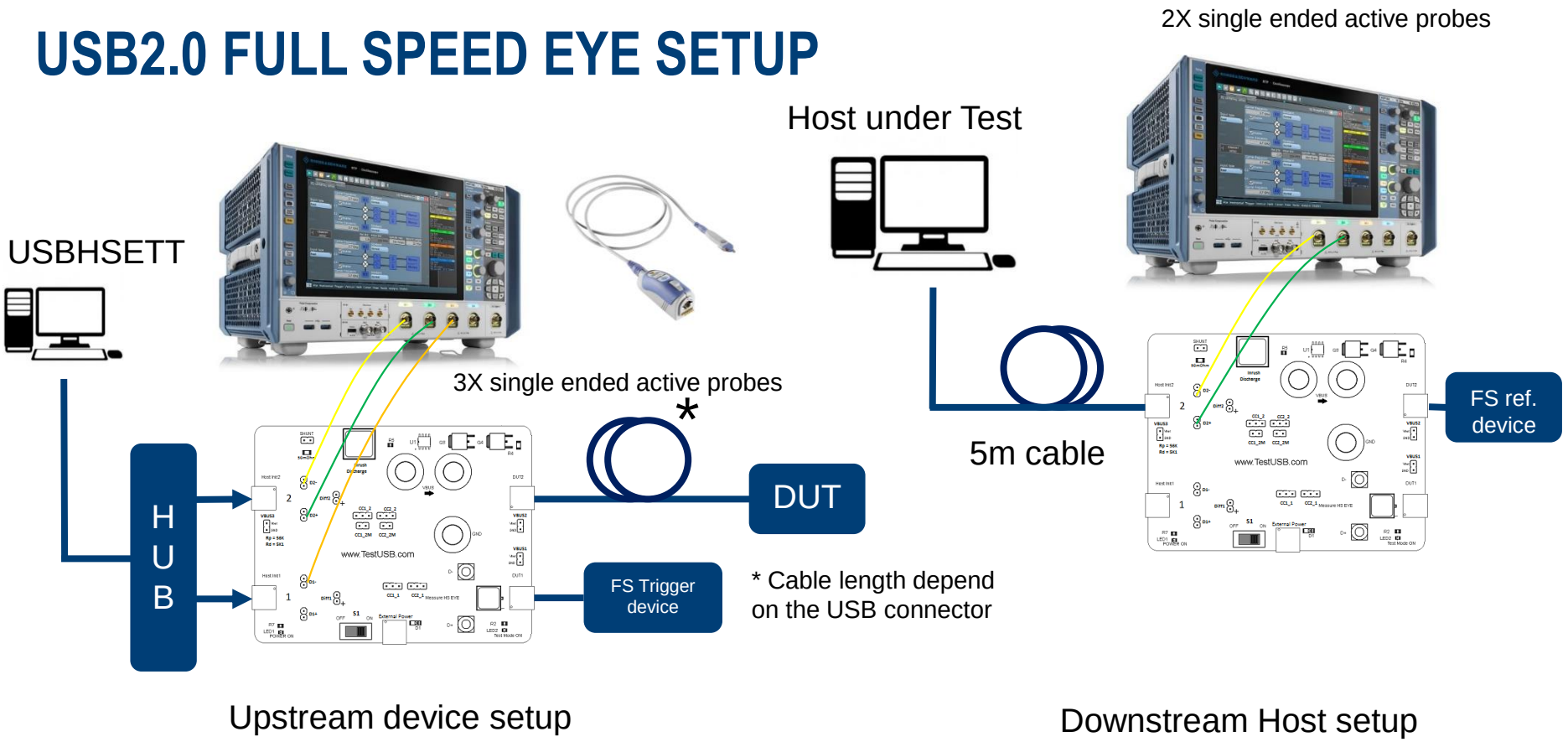
USB2.0 FULL & LOW SPEED EYE

- Full Speed upstream is measured far end:
  - Standard B -> 5m
  - Mini B -> 4.5m
  - Micro B -> 2m
  - Type-C -> 4m
  - Captive cable -> measured as it is



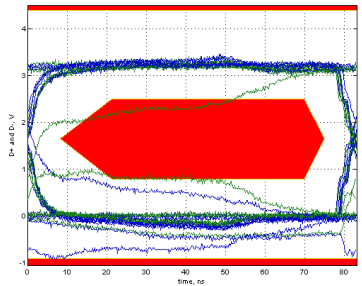
- Use good quality (preferred USB-IF certified) USB cables
- Full Speed downstream shall always be measured behind 5m for A-port and 4m for C-Port
- Low Speed device shall always have a captive cable and are measured as it is
- Any packet from the product under test can be used to calculate the eye
- It is not required anymore to measure this behind 5 tier of hubs as it was required a few years back
- Measurement is done with single ended active probes
- You need to downgrade a high speed device with a full speed hub

USB2.0 FULL SPEED EYE SETUP

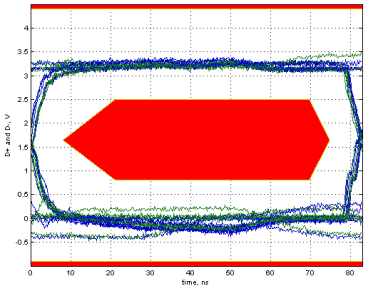


USB2.0 FULL & LOW SPEED EYE

- Signal Integrity problem may have following effects:
  - Product doesn't operate, behaves unstable, has poor performance, many CRC error's and/or retries in protocol trace, product not operate behind long cable
- Bad or too long cables
- Components like common mode chokes effect the eye diagram

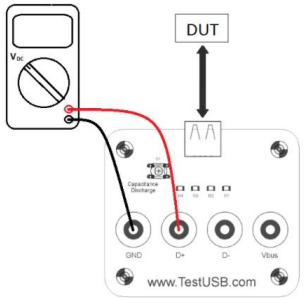


With common mode choke



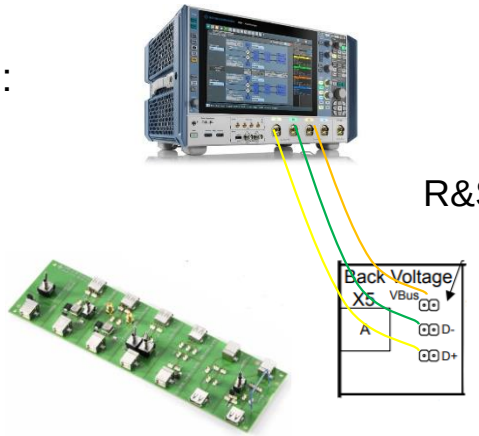
Without common mode choke

BACK VOLTAGE



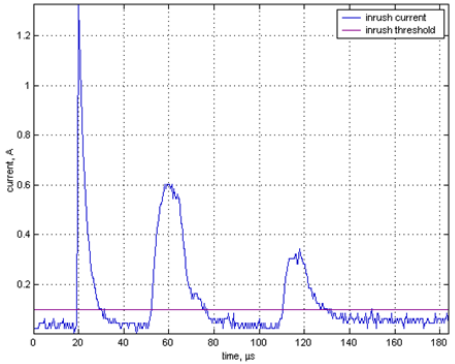
- A device may only draw current on Vbus not give current
- Pull-up resistor on D+ or D- may only become present when Vbus is available
- Measure DC Voltage before and after enumeration of the device < 400mV
- Common failure is a device put their pull-up resistor active even when Vbus is not available resulting in ~3.3V on D+ for Full Speed device and on D- for Low Speed device

- Products failing this test show following failures in the field:
  - PC fail to boot
  - Hub fail to enumerate downstream devices
  - Resume from suspend failures
  - Knocks out adjacent devices



R&S®RT-ZF1

INRUSH CURRENT



- Device inrush (< 50µC)
- Too high inrush current has following effects:
  - When connecting a device it might disconnect on another port
  - Causes the hub/host to go in overcurrent protection
- Condition
  - If product have external power that can be removed the Inrush test shall be done with and without external power.
  - For Type-C DRP (**d**ual **r**ole **p**ort) inrush shall be done in SNK (sink) mode = Rp by tester
  - Type-C SNK and DRP inrush shall be done in unattached mode = No Rp by tester
- How to avoid
  - Don’t use a too large capacitor over Vbus and GND (> 10µF)
  - If soft-start circuit is available, make sure it’s well adjusted

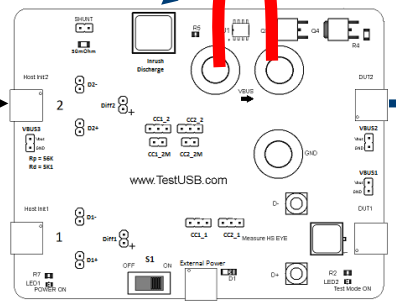
INRUSH SETUP

1X Current clamp probe

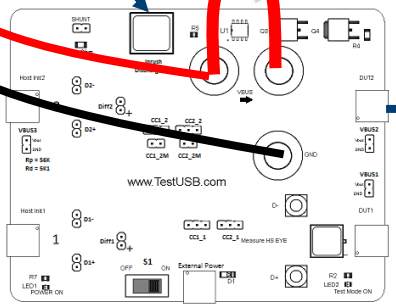
Discharge device by pressing discharge button
at release of button the inrush event occur

External +5V on Vbus

Type-C plug to A-Plug cable
Have internal Rp



DUT



DUT

Any Device and Type-C DRP in SNK mode

Type-C SNK only & DRP in Unattached mode

TEST J/K/SE0_NAK

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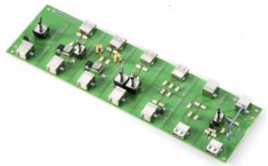
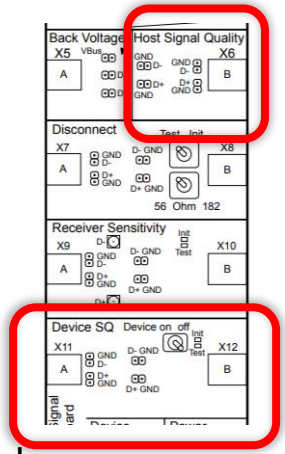


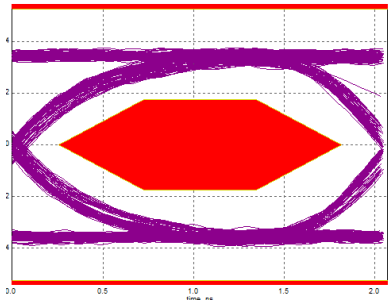


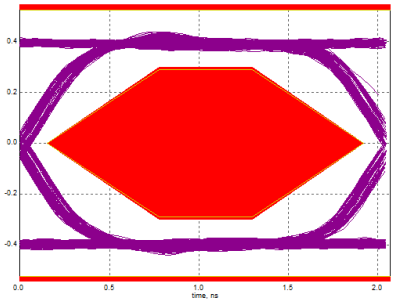
- DC voltage measurement High-speed Test_J and Test_K
- Ideal

	Test_J (mV)	Test_K (mV)	SE0_NAK (mV)
D+	400	0	0
D-	0	400	0

- Use USBHSETT to force Device, Hub or Windows system in the required test mode.
- For Embedded Host use PIDVID to force system in required test mode.
- Measurement shall be done with termination 45Ohm
- The driven lines of Test_J and Test_K (±10% 400mV) are removed as requirements. They are however still interesting value.
- Maximum allowed voltage on non-driven lines are relaxed from 10mV up to 20mV

USB HIGH SPEED EYE





- Measurement shall be done with SMA termination
- Official USB-IF Test fixtures are very crucial
- Compared to USB3.2 fixtures that are 50Ohm the USB2.0 fixtures are compensated to 45Ohm what result in a smaller EYE
- Keep the SMA cable length to scope short (≤ 50cm)
- Run the test multiple times to make sure the result always pass
- For Type-C product measure in both connection positions

Additional Information

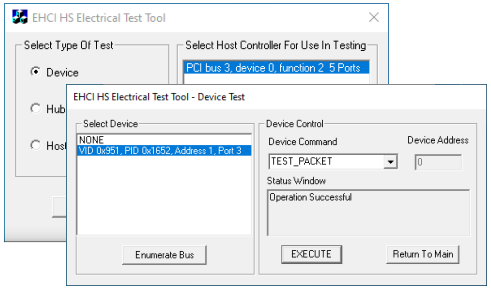
- Consecutive jitter range: -56.909 ps to 69.769 ps, RMS jitter 29.469 ps
- Paired JK jitter range: -16.193 ps to 16.172 ps, RMS jitter 6.642 ps
- Paired KJ jitter range: -35.756 ps to 16.287 ps, RMS jitter 7.970 ps
- Margin Above eye: 59.4812 mV
- Margin Below eye: 72.1321 mV
- Maximum Voltage: 437.8684 mV
- Margin Below Top: 87.1316 mV
- Minimum Voltage: -441.6691 mV
- Margin Above Bottom: 83.3309 mV

Required Tests

- Overall result: pass!
- Sync result:
  sync passes
- Signal eye:
  eye passes
- EOP width: 7.93 bits
  EOP width passes
- Measured signaling rate: 479.9876 MHz
  signal rate passes
- Edge Monotonicity: 0 mV
  Monotonic Edge passes
- Rising Edge Rate: 1073.01 V/us (596.45 ps equivalent risetime) passes
- Falling Edge Rate: 1104.21 V/us (579.60 ps equivalent falltime) passes

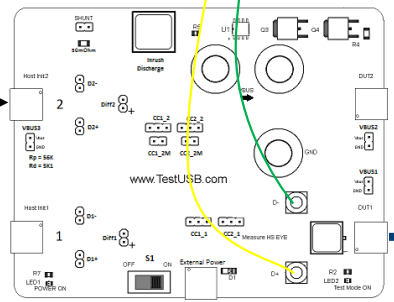
HIGH SPEED EYE SETUP

For Ehost use PIDVID to enter Test_Mode



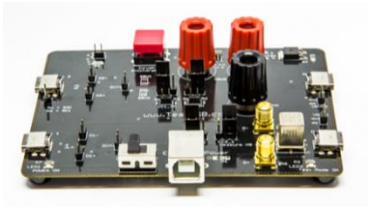
xHSETT

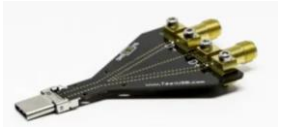
SMA cables

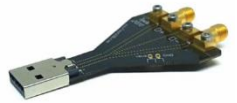


Use short as possible cable between DUT and Fixture

DUT

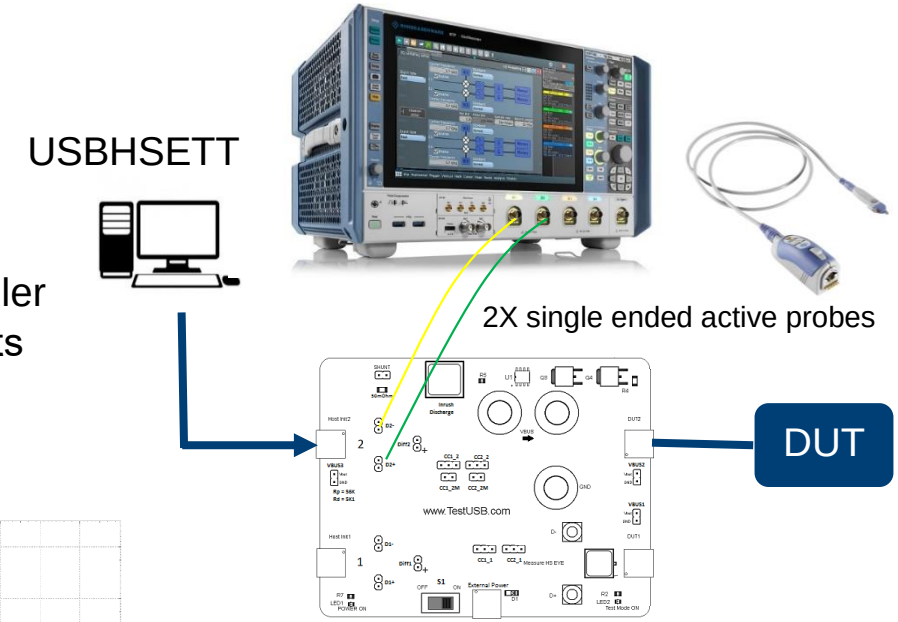


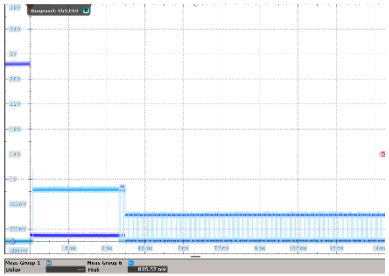


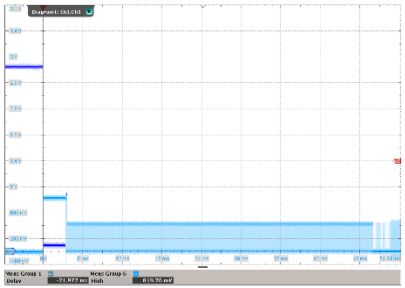


USB 2.0 HIGH SPEED CHIRP

- Chirp is the negotiation between host and device to identify a device support high speed
- If the negotiation is not successful the device fallback in full speed
- Very strong depending on the USB silicon/controller Therefore certified silicon ‘should’ pass these tests
- Enumeration in HSETT can be used but also real enumeration can be used

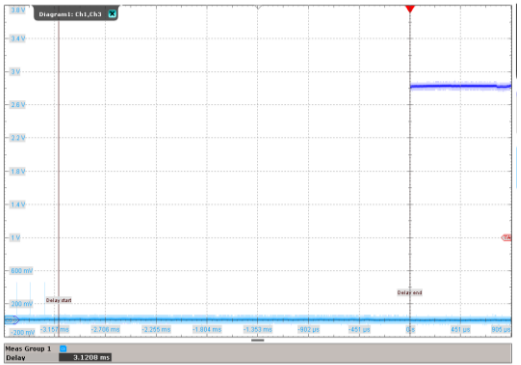




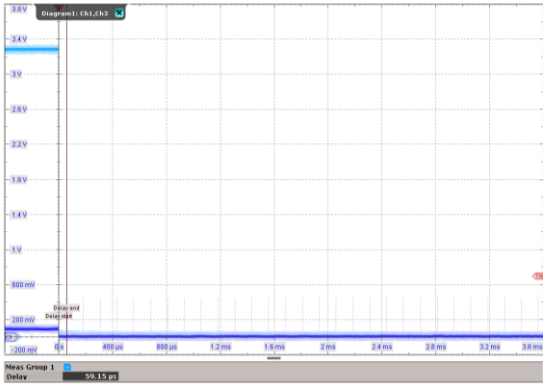


USB 2.0 SUSPEND RESUME

- Same setup chirp setup
- USBHSETT can force the device, hub or windows system in the require mode.
- A high speed embedded host may support suspend and if so it is triggered with the PIDVID
- For suspend and resume verify the timing and voltage
- Very strong depending on the USB silicon/controller
  Therefore certified silicon ‘should’ pass these tests



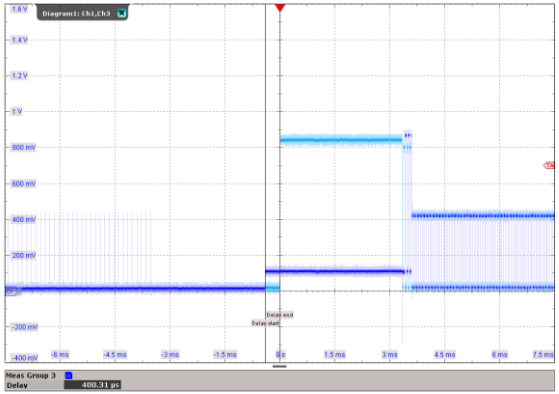
Suspend



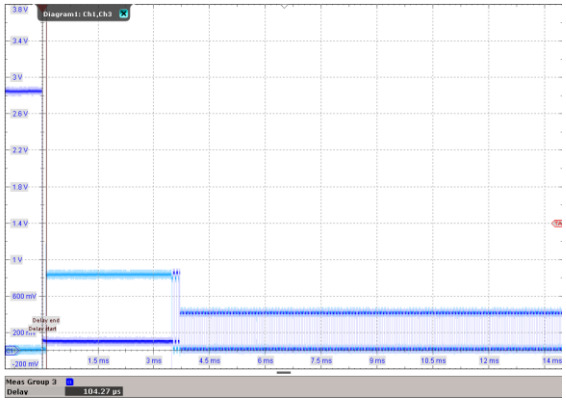
Resume

USB 2.0 RESET AND RESET FROM SUSPEND

- Same setup chirp setup
- Only applicable for device and hub and is triggered with USBHSETT
- Very strong depending on the USB silicon/controller
  Therefore certified silicon ‘should’ pass these tests



Reset



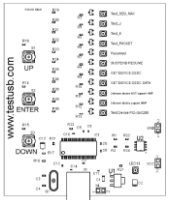
Reset from suspend

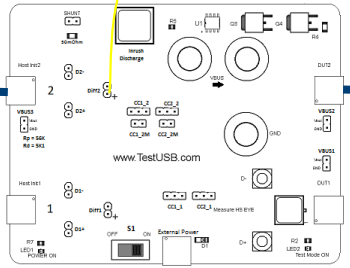
USB 2.0 HIGH SPEED PACKET PARAMETER

- ► For device, host and windows host testing HSETT can be used
- ► For embedded host PIDVID can be used or real data communication between host and device

(often Ehost implement the PIDVID test step feature incorrect)

PIDVID

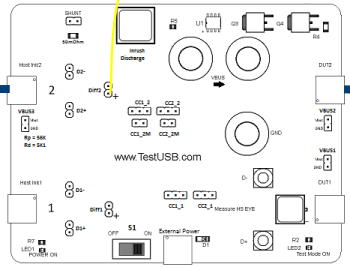




EHost

USBHSETT

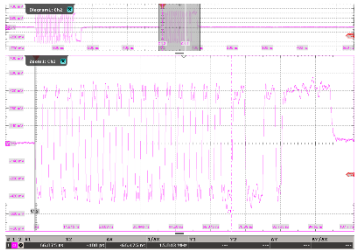
1X differential active probe

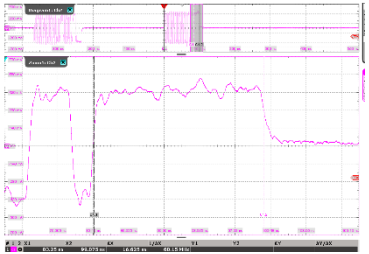


DUT

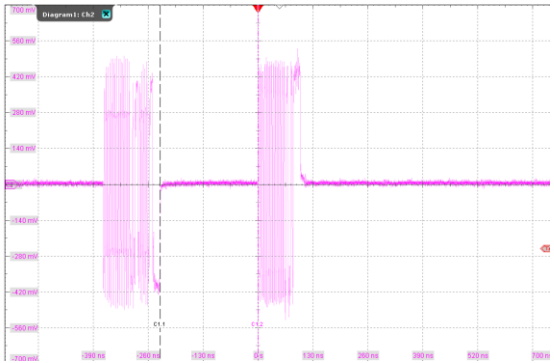
USB 2.0 HIGH SPEED PACKET PARAMETER

- Verify the SYNC (32bit) and EOP (8bit) field





- Verify the response time between host and device
- Hubs affect the results
  - Can truncate 4 Sync bit
  - Can add 4 EOP bit
  - Add additional delay in the response time
- Very strong depending on the USB silicon/controller
  Therefore certified silicon ‘should’ pass these tests



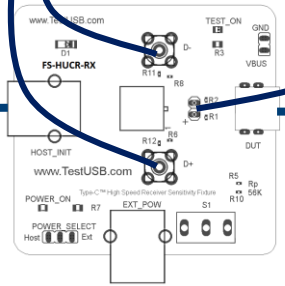
USB 2.0 HIGH SPEED RECEIVER

Absolute Values (mV)	Squelch EL_16	No Squelch EL_17
200	PASS	FAIL
150		WAIVER
100		PASS
50	FAIL	
0		

AWG or Pulse Generator

1X differential active probe

USBHSETT



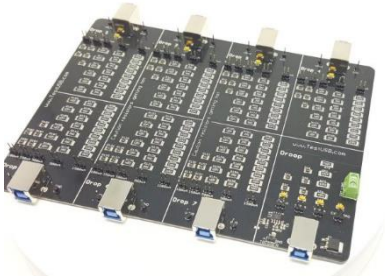
DUT

Put device in SE0_NAK test mode

VBUS DROP

- Under all condition shall Vbus not be more than 5.5V on an A-Port
- DC Vbus min and load for A-Port

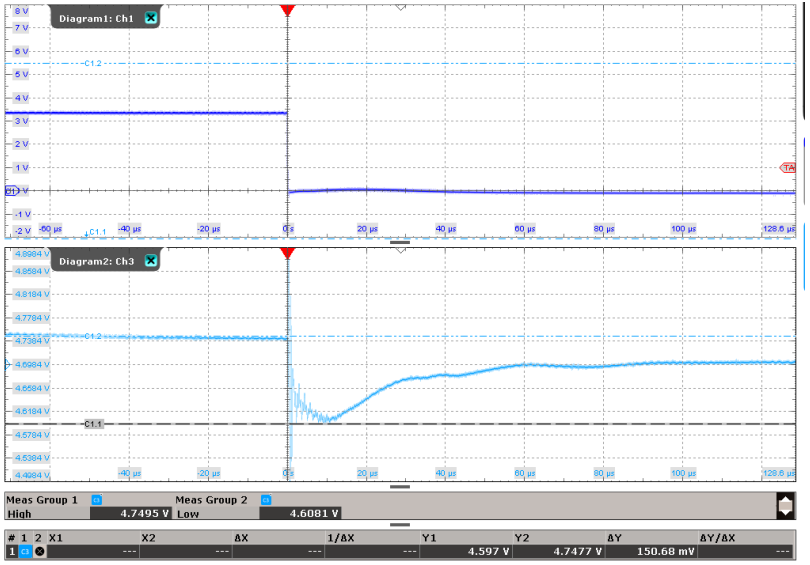
A-Port	Load (mA)	Vbus min (V)
USB 2.0 Bus-Powered hub	100	4.4
USB 2.0 Self-Powered hub	500	4.75
USB 3.2 Self-Powered hub	900	4.75
USB 2.0 Host system	500	4.75
USB 3.2 Host system	900	4.75
CDP BC1.2 Hub or Host	1500	4.75

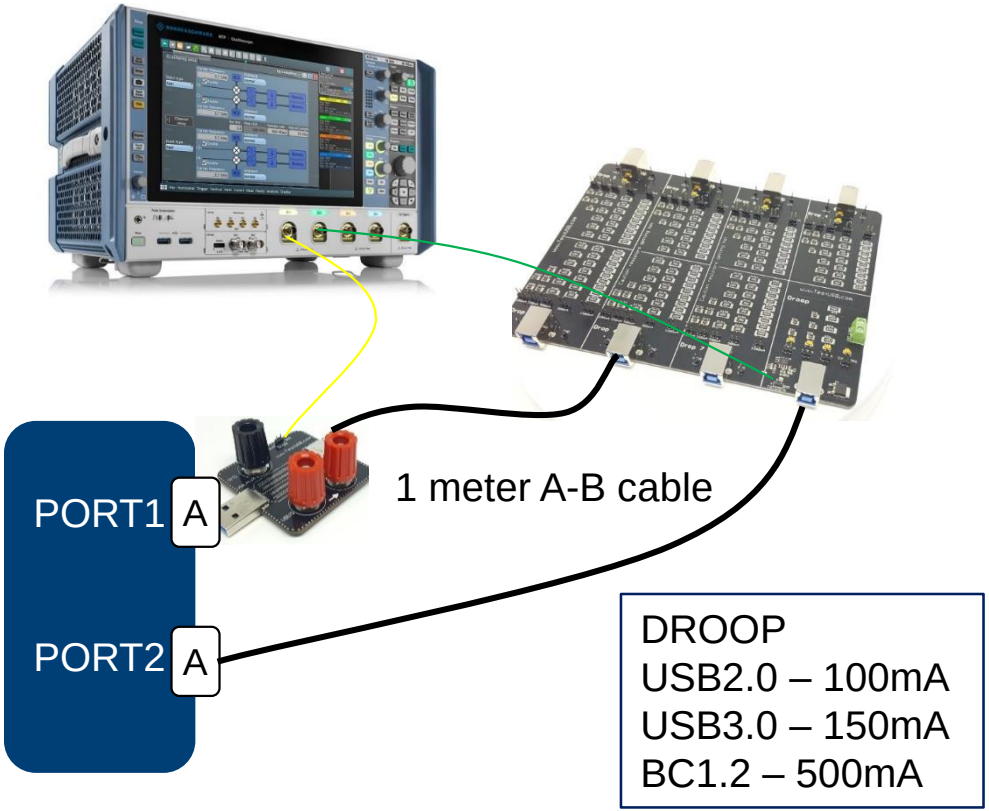


- Vbus DC voltage shall be measured without load and with fully loaded

VBUS DROOP

Adjacent port shall not droop more than 330mV





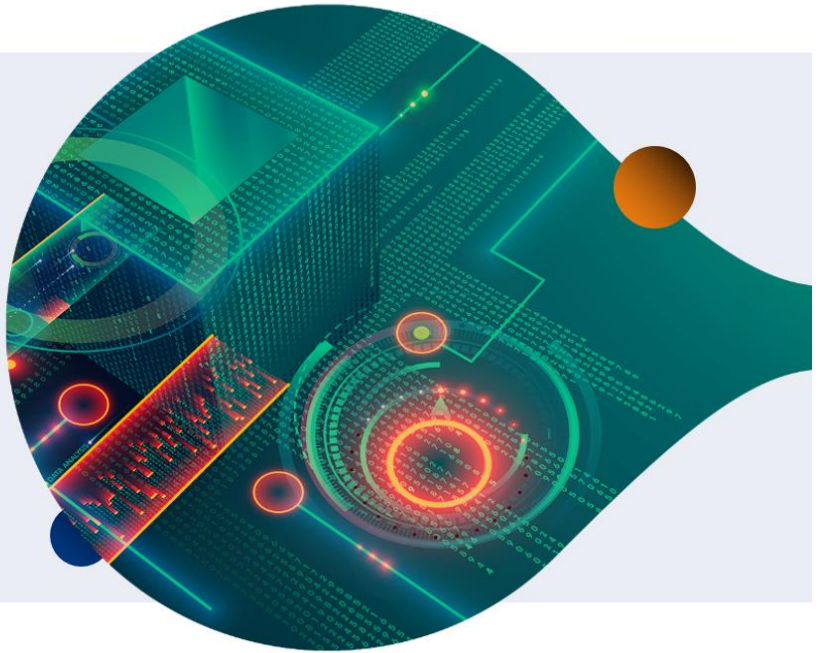
Droop load switch on/off every second

VBUS MEASUREMENTS

- Failing Vbus Drop may cause devices that draw high current not to enumerate
- Failing Vbus Droop may cause to drop devices on the adjacent USB ports
- The drop droop board use resistive load approach what is not ideal
- The cable has significant impact in the setup
- Vbus drop failures are typical caused by not have enough power in the setup or an issue with DC-DC convertor
- Vbus droop failures are typical caused by a too low capacitor over Vbus to GND
- The nearest adjacent port typical have the largest droop effect
- For Type-C downstream ports the USB-IF QuadraMax shall be used instead of drop droop board
  - Current source approach
  - Type-C PD protocol aware
  - Takes cable loss into account
  - Covers more test like Inrush Droop

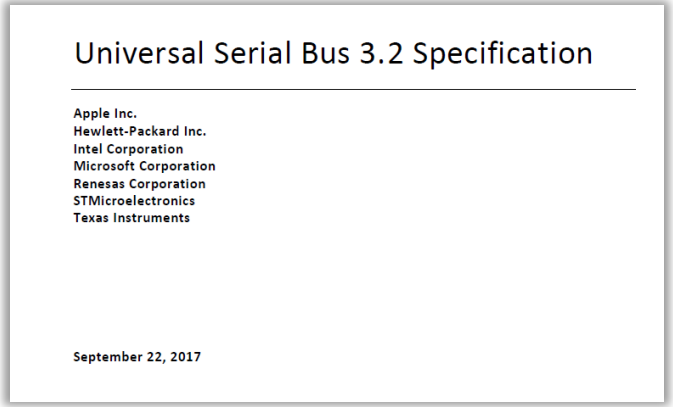
eurofins | Digital Testing

USB-IF Compliance USB 3.2 Physical Layer Testing

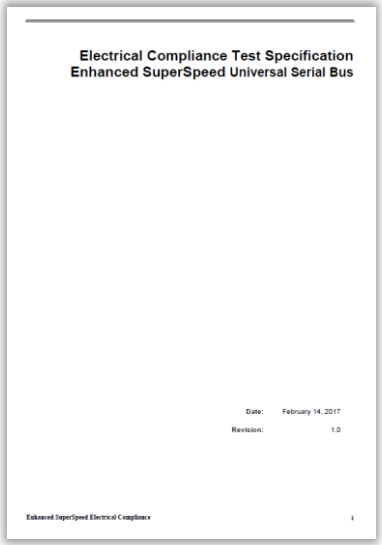


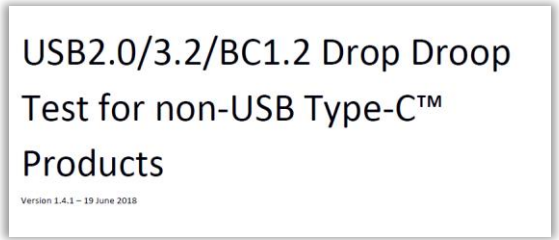
USB 3.2 COMPLIANCE TESTING

USB 3.2 ELECTRICAL COMPLIANCE



USB 3.2 Spec + ECN





https://compliance.usb.org/

USB-IF USB 3.2 Electrical Compliance

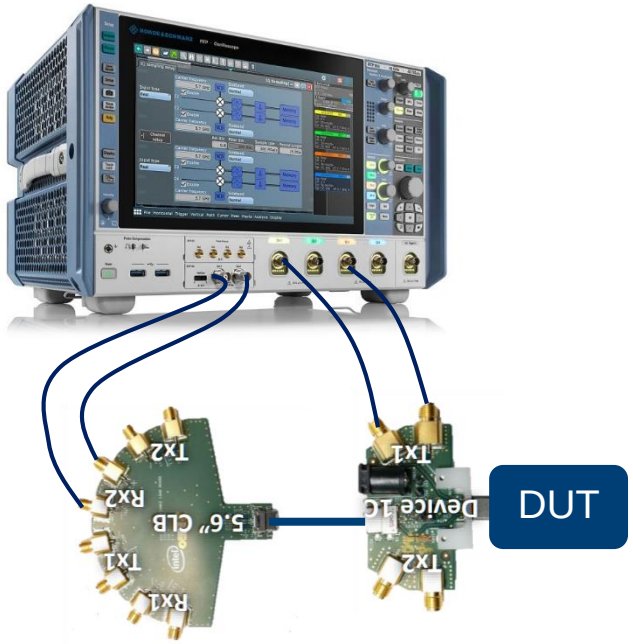
SETUP REQUIREMENTS

www.usb.org

USB 3.2 GEN1 & GEN2 TRANSMITTER SETUP

- Tx EYE and Jitter
- Tx LFPS
- Tx SSC
- Tx Gen2 Pre-Shoot / De-emphasis

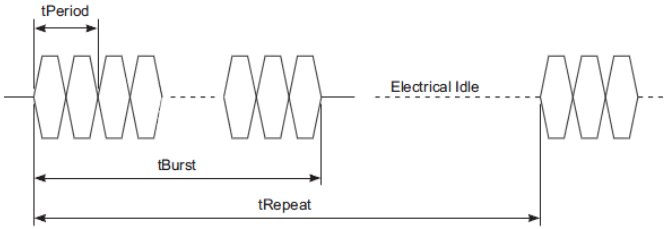
- Use appropriate USB-IF fixture
- All Tx measurements are done near end
- The long channel Tx eye and jitter will be embedded with the USB-IF provide S-parameter
- The CTLE and DFE equalizer will be done by scope
- Toggling between test patterns is by sending Ping.LFPS

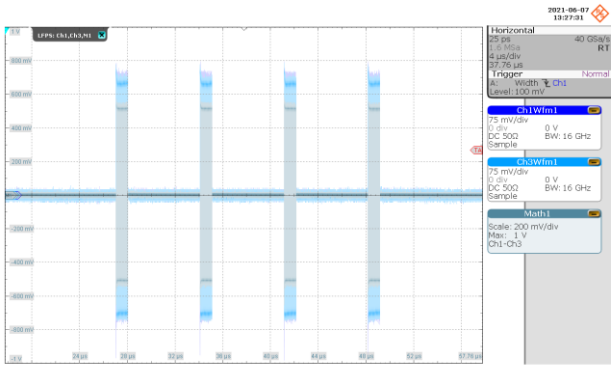


USB 3.2 LOW FREQUENCY PERIODIC SIGNALING

USB-IF Compliance test Polling.LFPS
Vpp >=800mV <= 1.2V
tPeriod >= 20ns <= 100ns
tBurst >= 600ns <= 1.4 µs
tRepeat >= 6µs <= 14 µs
Rise/Fall time <= 4ns
Duty cycle >= 40% <= 60%
AC Common Mode Voltage <= 100mV

From the moment the product under test is powered on it will send this Polling.LFPS





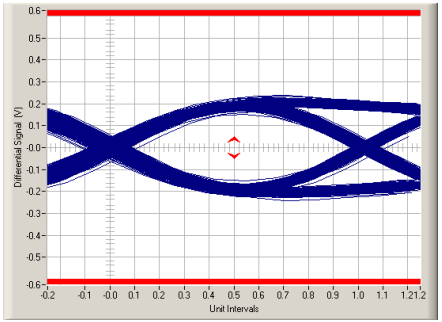
USB 3.2 SPREAD SPECTRUM CLOCKING

- Spread Spectrum Clocking is mandatory in the Tx
  - However some vendors disable this feature
- SSC reduce the emitted energy from a signal
- SSC distributes energy from a single frequency to a frequency band near the original frequency
- CP1 is used for measuring

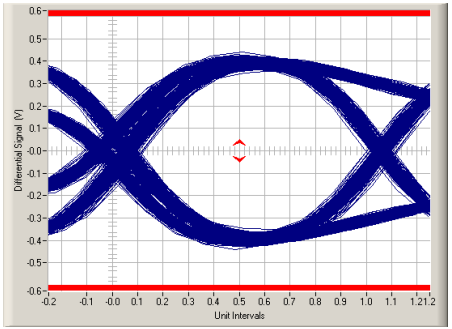
Measurement	Value	Limits
SSC Modulation Rate	32.949 kHz	30 kHz <= x <= 33 kHz
SSC Deviation Max (max)	119.27 ppm	-300.00<= x <= 300.00 ppm
SSC Deviation Max (min)	118.95 ppm	-300.00<= x <= 300.00 ppm
SSC Deviation Min (max)	-4890.97 ppm	-5300.00<= x <= -3700.00 ppm
SSC Deviation Min (min)	-4893.88 ppm	-5300.00<= x <= -3700.00 ppm
SSC DfDt	360.98 ppm	x < 1250.00 ppm

USB 3.2 GEN1 JITTER AND EYE

- Near end measurement is done with CP0 and CP1
- Toggling between test modes is done by sending Ping.LFPS on the Rx pair



Long Channel Transmitted Eye - Transition Eye

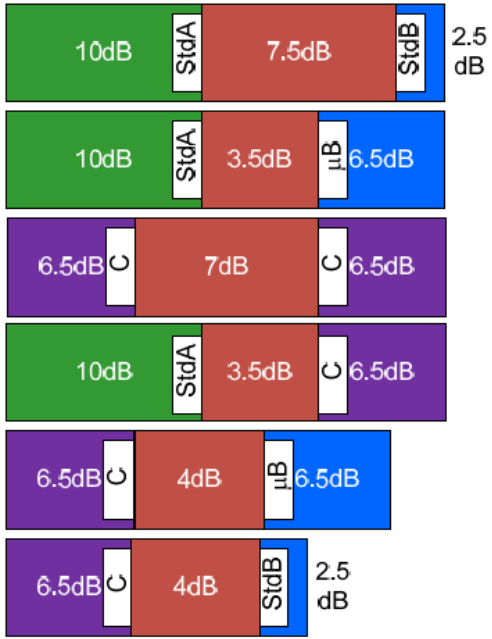


Short Channel Transmitted Eye - Transition Eye

Measurement	Value	Limits
Tj CP1	8.469 ps	x <= 132 ps
Rj (rms) CP1	631.209 fs	x <= 3.27 ps
Tj CP0	16.153 ps	x <= 132 ps
Rj (rms) CP0	631.209 fs	x <= 3.27 ps
Dj CP0	7.278 ps	x <= 86 ps
Avg UI	200.514 ps	199.94 ps <= x <= 201.06 ps
Min Time Between Crossover	0 s	Information Only
Max Peak to Peak Jitter	14.711 ps	Information Only
Non Transition Eye Violation	0 hits	x = 0 Violation Point
Transition Eye Violation	0 hits	x = 0 Violation Point
Total Eye Violation Points	0 hits	x = 0 Violation Point
Max Non Transition Voltage	428.486 mV	Information Only
Min Non Transition Voltage	-425.668 mV	Information Only
Max Transition Voltage	487.185 mV	Information Only
Min Transition Voltage	-481.629 mV	Information Only
Min Non Transition Upper Margin	242.434 mV	Information Only
Min Non Transition Lower Margin	-235.718 mV	Information Only
Min Transition Upper Margin	341.311 mV	Information Only
Min Transition Lower Margin	-345.84 mV	Information Only
Transmitted Eye Height	578.151 mV	Information Only
Transmitted Eye Width	183.847 ps	Information Only

USB 3.2 GEN1 JITTER AND EYE

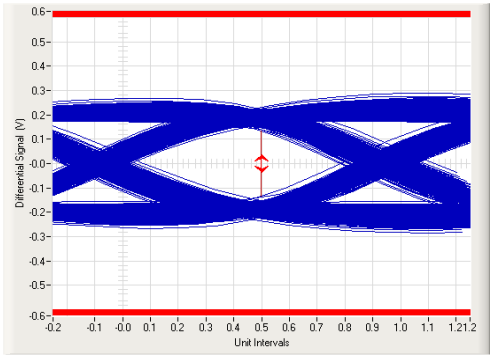
- The CTLE equalization is done in making the EYE diagram
- Tj at BER-12 <= 132 ps with CP0 at TP1
- Dj <= 86 ps with CP0 at TP1
- Rj <= 3.27 ps with CP1 at TP1 (Informative and no PASS FAIL criteria)
- Long channel measurement is the same as the short channel measurement with the difference that the RTP scope embedded the USB-IF S-Parameter to the signal
- The long channel loss depend on:
  - Up or downstream port
  - Type of USB connector



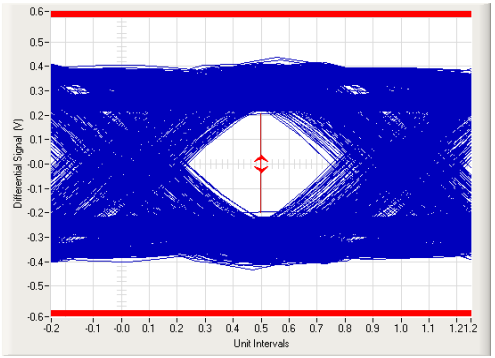
USB3.2 Gen1
IL @ 2.5GHz
max -20dB

USB 3.2 GEN2 JITTER AND EYE

- Same setup Gen1
- Test modes CP9 and CP10 are used



Long Channel Transmitted Eye - Transition Eye

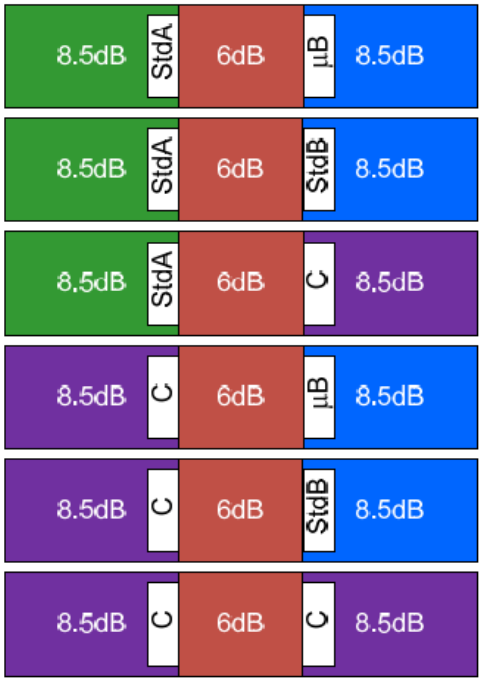


Short Channel Transmitted Eye - Transition Eye

Measurement	Value	Limits
Tj CP10	5.839 ps	x <= 67.1 ps
Rj (rms) CP10	463.816 fs	x <= 1 ps
Tj CP9	25.723 ps	x <= 67.1 ps
Rj (rms) CP9	463.816 fs	x <= 1 ps
Dj CP9	21.314 ps	x <= 53 ps
Avg UI	100.242 ps	99.96999 ps <= x <= 100.5301 ps
Min Time Between Crossover	85.699 ps	Information Only
Max Peak to Peak Jitter	29.768 ps	Information Only
Non Transition Eye Violation	0 hits	x = 0 Violation Point
Transition Eye Violation	0 hits	x = 0 Violation Point
Total Eye Violation Points	0 hits	x = 0 Violation Point
Max Non Transition Voltage	278.073 mV	Information Only
Min Non Transition Voltage	-275.339 mV	Information Only
Max Transition Voltage	274.19 mV	Information Only
Min Transition Voltage	-267.792 mV	Information Only
Min Non Transition Upper Margin	106.139 mV	Information Only
Min Non Transition Lower Margin	-106.451 mV	Information Only
Min Transition Upper Margin	110.654 mV	Information Only
Min Transition Lower Margin	-109.801 mV	Information Only
Transmitted Eye Height	282.589 mV	Information Only
Transmitted Eye Width	74.277 ps	Information Only

USB 3.2 GEN2 JITTER AND EYE

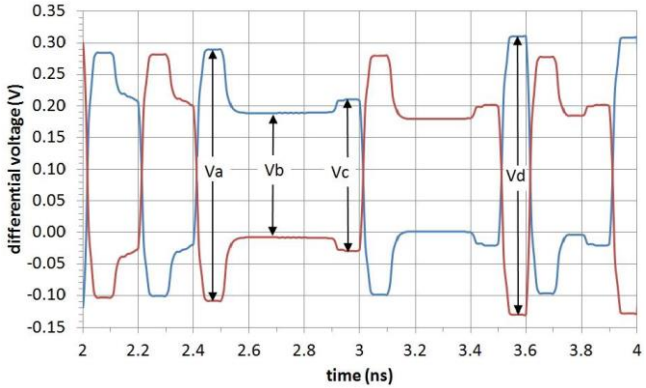
- The CTLE + DFE equalization is done in making the EYE diagram
- Tj at BER-12 <= 67.1 ps with CP0 at TP1
- Dj <= 53 ps with CP0 at TP1
- Rj <= 1 ps with CP1 at TP1 (Informative and no PASS FAIL criteria)
- Long channel measurement is the same as the short channel end setup measurement with the difference that the RTP scope embedded the USB-IF S-Parameter to the signal.
- Different than Gen1 the long channel is always same S-parameter except for devices with captive cable



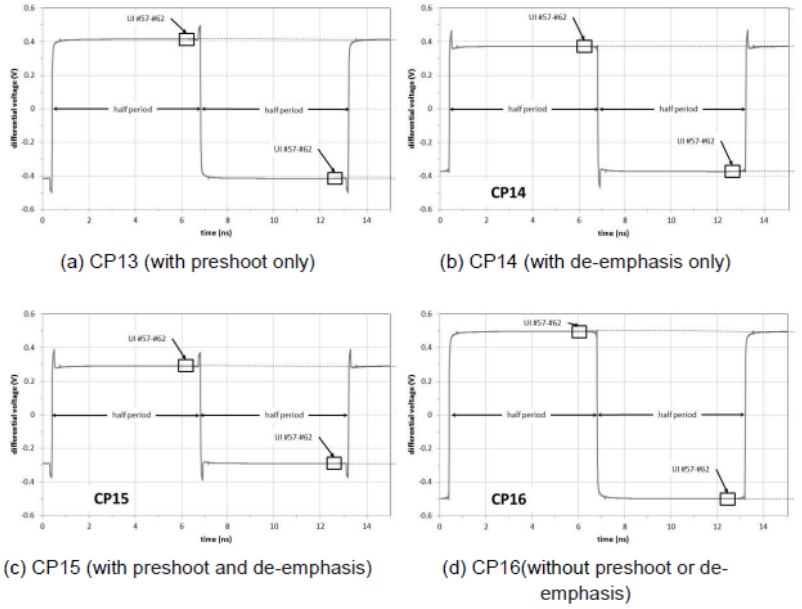
USB3.2 Gen2
IL @ 5GHz
-23dB

USB 3.2 GEN2 PRE-SHOOT/DE-EMPHASIS

- Only applicable for Gen2
- CP13, CP14 and CP15 required
- Can be difficult to differentiate the patterns



Preshoot = 20log(Vc/Vb)
De-emphasis = 20log(Vb/Va)



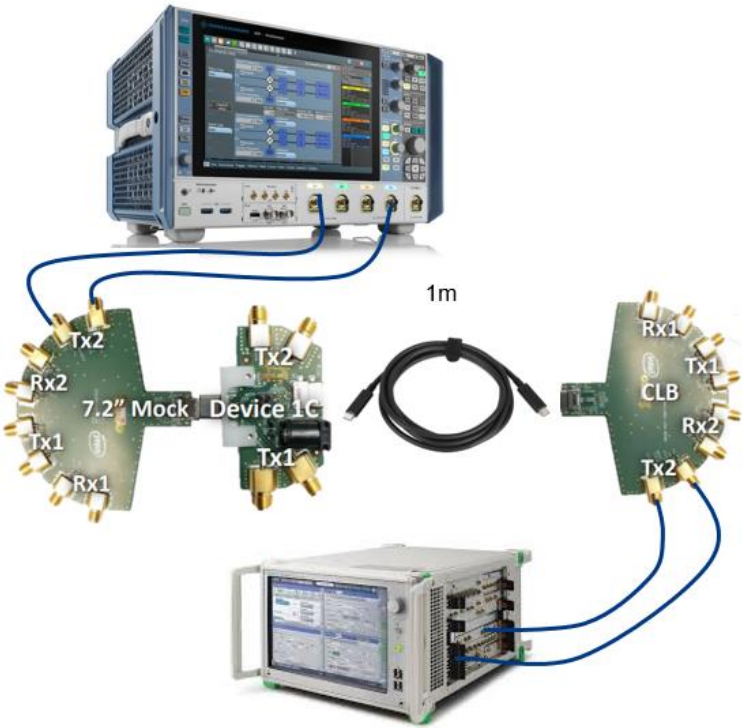
(a) CP13 (with preshoot only)

(b) CP14 (with de-emphasis only)

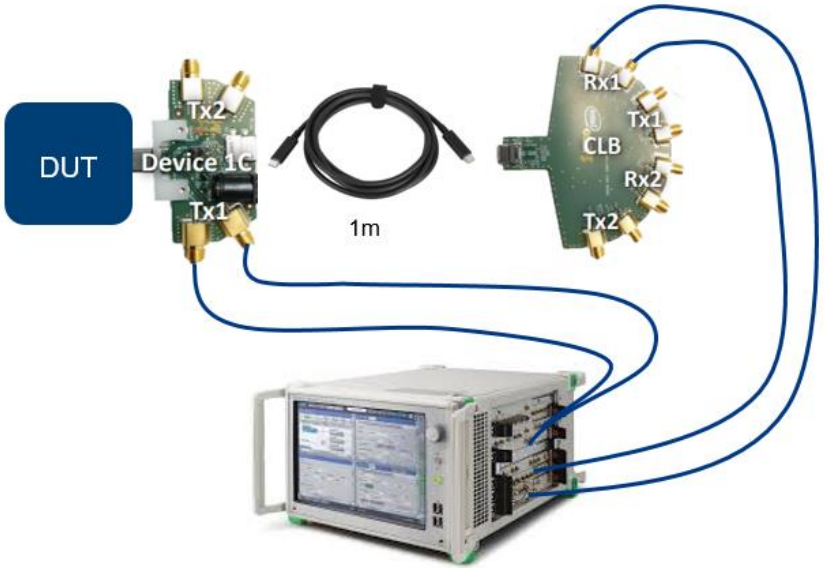
(c) CP15 (with preshoot and de-emphasis)

(d) CP16(without preshoot or de-emphasis)

USB 3.2 RECEIVER TESTING



Calibration example Device Type-C USB3.2 Gen2



Measurement example Device Type-C USB3.2 Gen2

MOST COMMON SIGNAL INTEGRITY ISSUE

- Bad PCB design:
  - Traces too long or not matched
  - Not follow PCB design rules
- Bad internal cabling
- ESD, EMI components on the data lines that do not meet the USB requirements
- Wrong bias resistor
- Wrong PHY settings (Boost, Emphasis, Equalizer,..)
- Improper crystal oscillator
- Re-driver or Re-timer not set properly
- Noisy power supply
- Interference from other signals

- Unable to enter the required test modes
- Capture the wrong USB packet for analysis
- Make sure the probe settings are accordingly to the probe tip used
- Wrong or broken test fixture
- Setup of probe and SMA cable not de-skewed

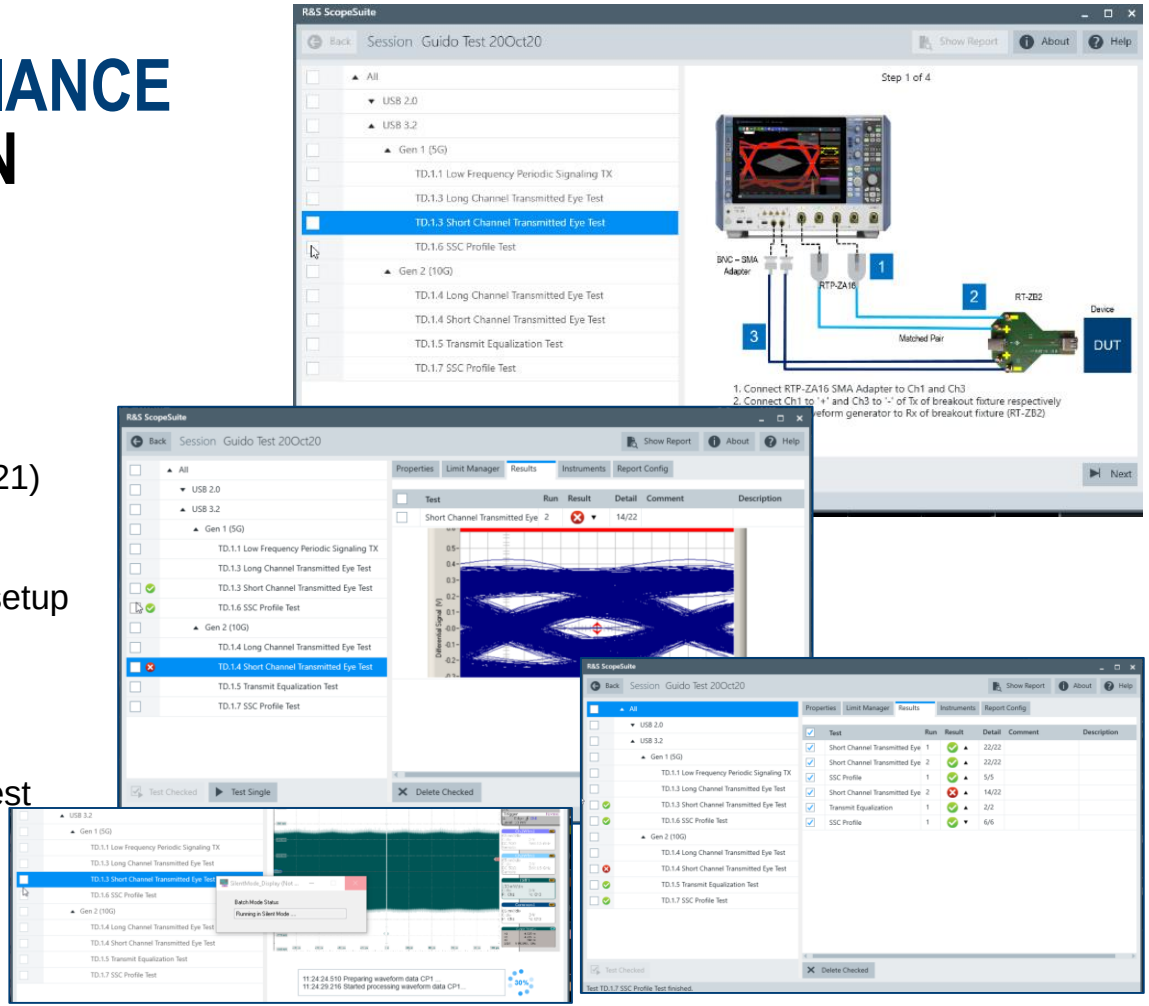
check
www.testusb.com
for more tips

DEMONSTRATION WITH R&S RTP OSCILLOSCOPE

SUMMARY

USB3.2 GEN1/2 COMPLIANCE AUTOMATED SOLUTION

- Option: R&S®RTP-K101
- Functions:
  - TX compliance test for USB 3.2 Gen1 & 2
  - Includes USB1.x/2.0 test (R&S®RTP-K21)
- Advantages:
  - Automated test execution with guided setup steps and final report
  - Integrated generator option to toggle compliance pattern
  - Channel embedding for long channel test without additional options
  - R&S®RT-ZB2 test fixture for USB3.2 Gen1 pre-compliance



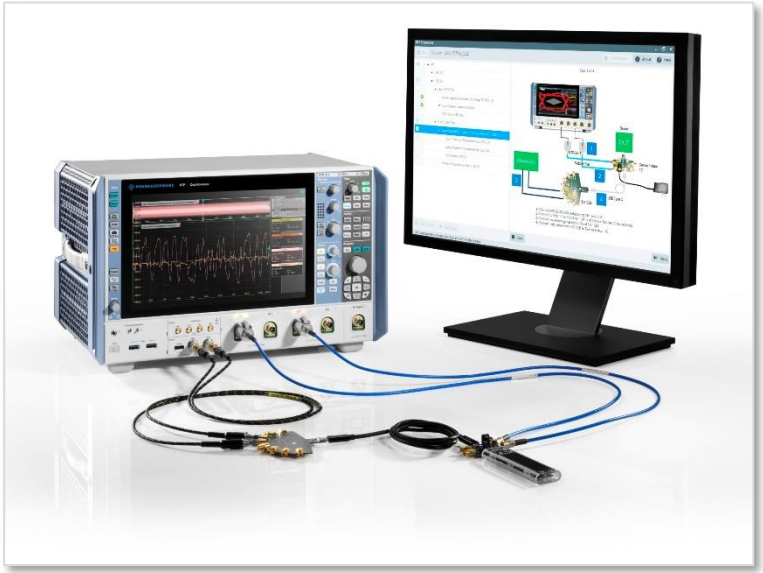
SUMMARY

- The USB interface gains more and more popularity
- To assure interoperability use compliance test

- <some points from Eurofins >
- ...

- R&S offers a full suite of compliance test options up to USB 3.2 Gen 2

- Close cooperation between Eurofins Digital Testing and R&S on Compliance Test solutions for Highspeed interfaces



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Thank you!

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