HOW TO ENSURE MultiGigabit AUTOMOTIVE ETHERNET COMPLIANCE WITH OPEN ALLIANCE TC15

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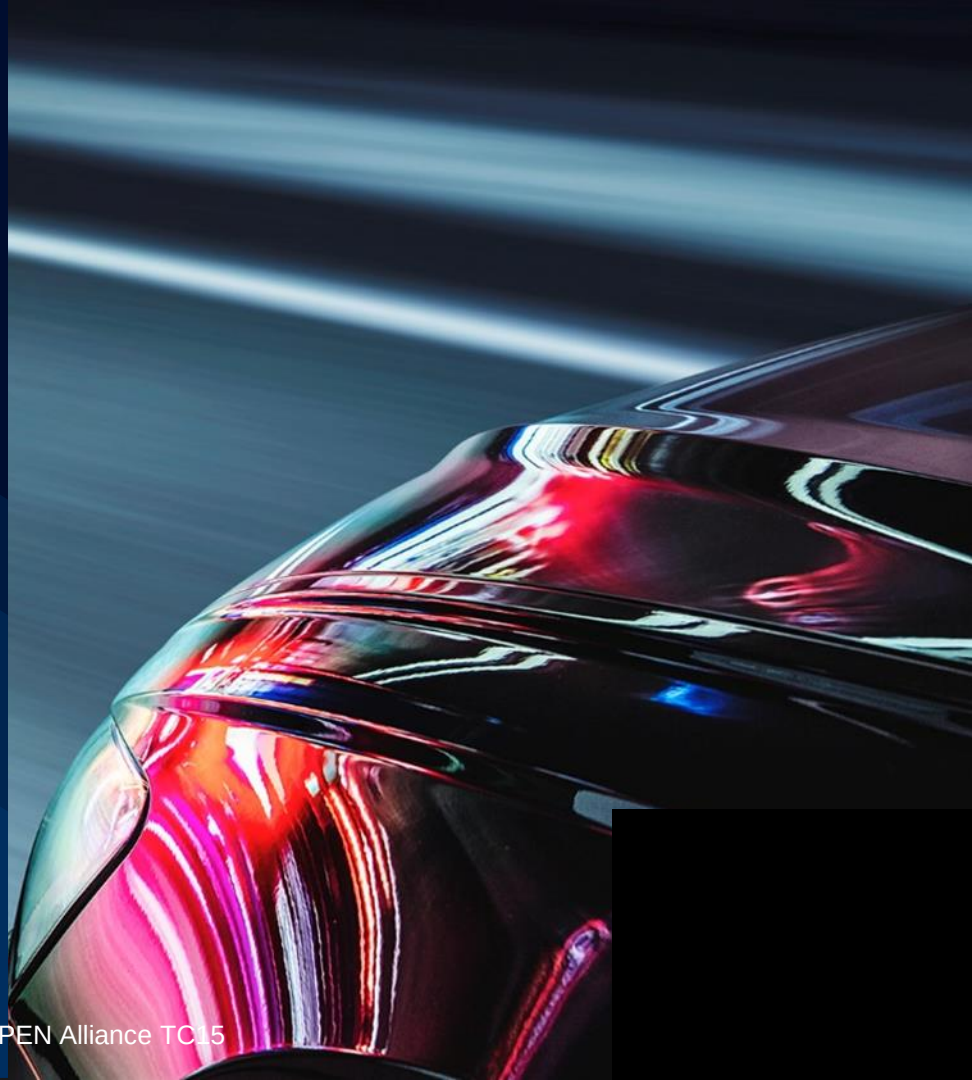
ROHDE&SCHWARZ
Make ideas real

CONTENT

Automotive Ethernet

- An update on OA TC15 & TC9 for MultiGBASE-T1
- PHY Layer compliance testing
- Q&A session



FUTURE AUTOMOTIVE ETHERNET STANDARDS

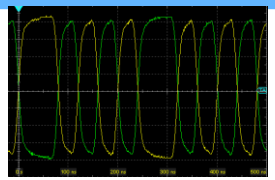
10BASE-T1S

IEEE 802.3cg

Multidrop
PoDL

OA TC6 & TC14

Coding NRZ



Symbol Rate 12.5 MBaud

Scope 600MHz oscilloscope
RTO/RTP

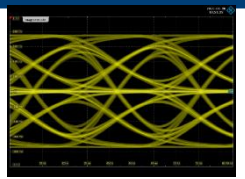
VNA ZNB/ZND (4.5GHz)

100BASE-T1

IEEE 802.3bw

Established &
On the road

Coding PAM3



66 MBaud

600MHz oscilloscope
RTO/RTP
ZNB/ZND (4.5 GHz)

1000BASE-T1

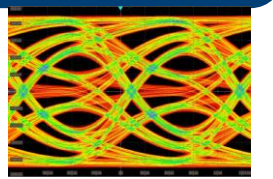
IEEE 802.3bp

3 PHYs released

SOP 2020

OA TC8/TC9/TC12

Coding PAM3



750 MBaud

2GHz oscilloscope
RTO/RTP
ZNB/ZND (4.5GHz)

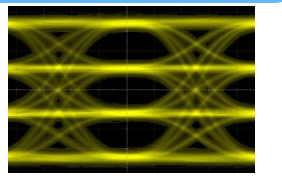
Multi-gig

2.5/5/10GBASE-T1
STP cable

IEEE 802.3ch
OA TC15 PMA spec
under preparation

OA TC9 (3rd draft released)

Coding PAM4

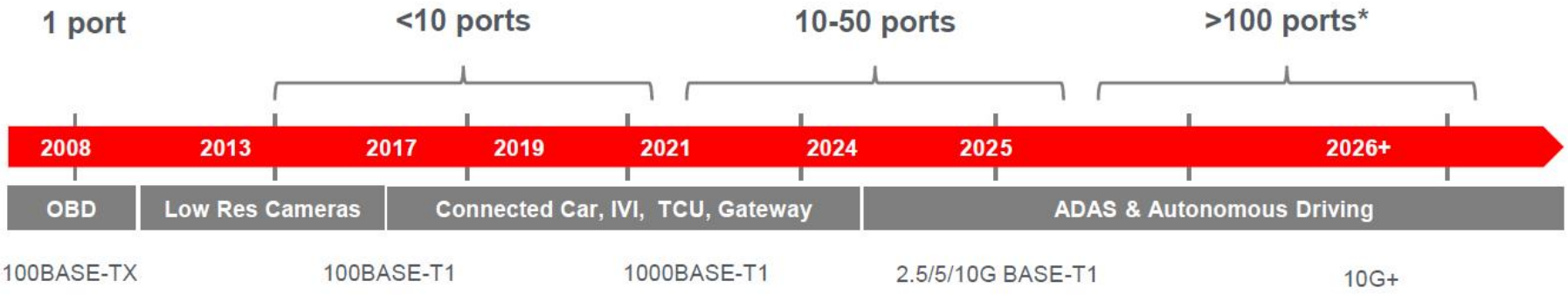


1.4/2.8/5.6 GBaud

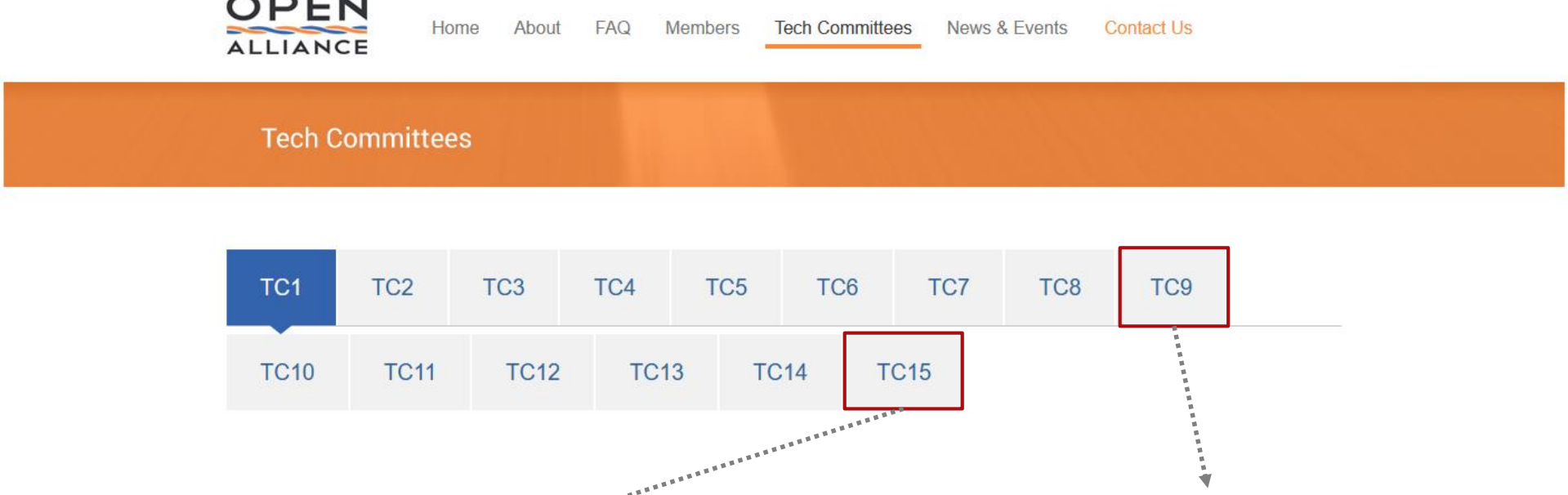
2.5GBASE-T1: 4GHz → RTP4
5GBASE-T1: 8GHz → RTP8
10GBASE-T1: 16GHz → RTP16
ZNB/ZND (8.5GHz)

...

Trends in Automotive Ethernet



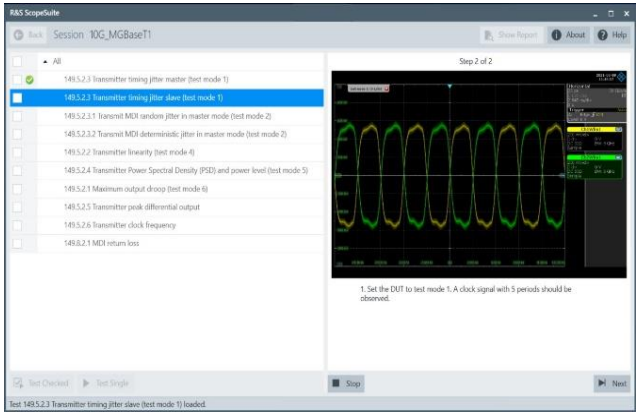
*average Ethernet ports per vehicle
** Photo courtesy of Marvell Technology Group



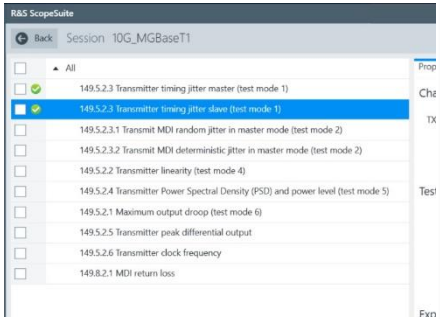
TC15 group created for MultiGig Ethernet for 2.5/5/10GBASE-T1. (PMA under preparation)

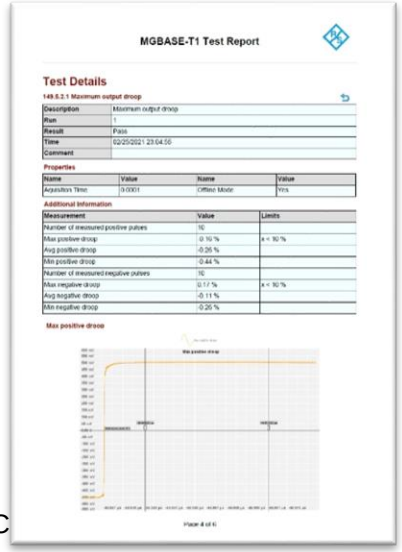
1000BASE-T1 Ethernet Channel & Passive Components (v2.3)
NGAuto Channel & Components for 1000BASE-T1
2.5/5/10GBASE-T1 Link Segments (draft v0.3)

NEW MULTIGBASE-T1 COMPLIANCE TEST SOLUTION



- New K88 AUT Ethernet compliance option for 2.5/5/10G speeds
- Based on the IEEE 802.3ch
- Uses PAM4 modulation with symbol rates of 1.4/2.8/5.6 GHz
- Runs exclusively on shielded twisted pair (STP)
- Additional information:
  - Available on both the RTO (up to 2.5G) and RTP
  - Coverage of all relevant test cases
  - No additional options required (e.g. jitter)
  - Complete solution with VNA & fixtures





OPEN TC15 TEST SPEC COVERAGE LAYER 1

- **Group 1: PMA Transmit Tests:**
  - Maximum Output Droop
  - Transmitter Linearity
  - Transmitter **T**iming **J**itter
  - Transmit MDI **R**andom **J**itter in master mode
  - Transmit MDI **D**eterministic **J**itter in master mode
  - Transmitter Power Spectral Density (PSD) and power level
  - Transmitter Peak Differential Output
  - Transmitter Clock Frequency
  - Transmitter Distortion
- **Group 2: PMA Receive Tests:**
  - Bit Error Rate Verification
  - Alien Crosstalk Noise Rejection
  - Receiver Frequency Tolerance (Optional)
- **Group 3: MDI Impedance Requirements:**
  - MDI return Loss

Specification is in draft version

CONTENT

Automotive Ethernet

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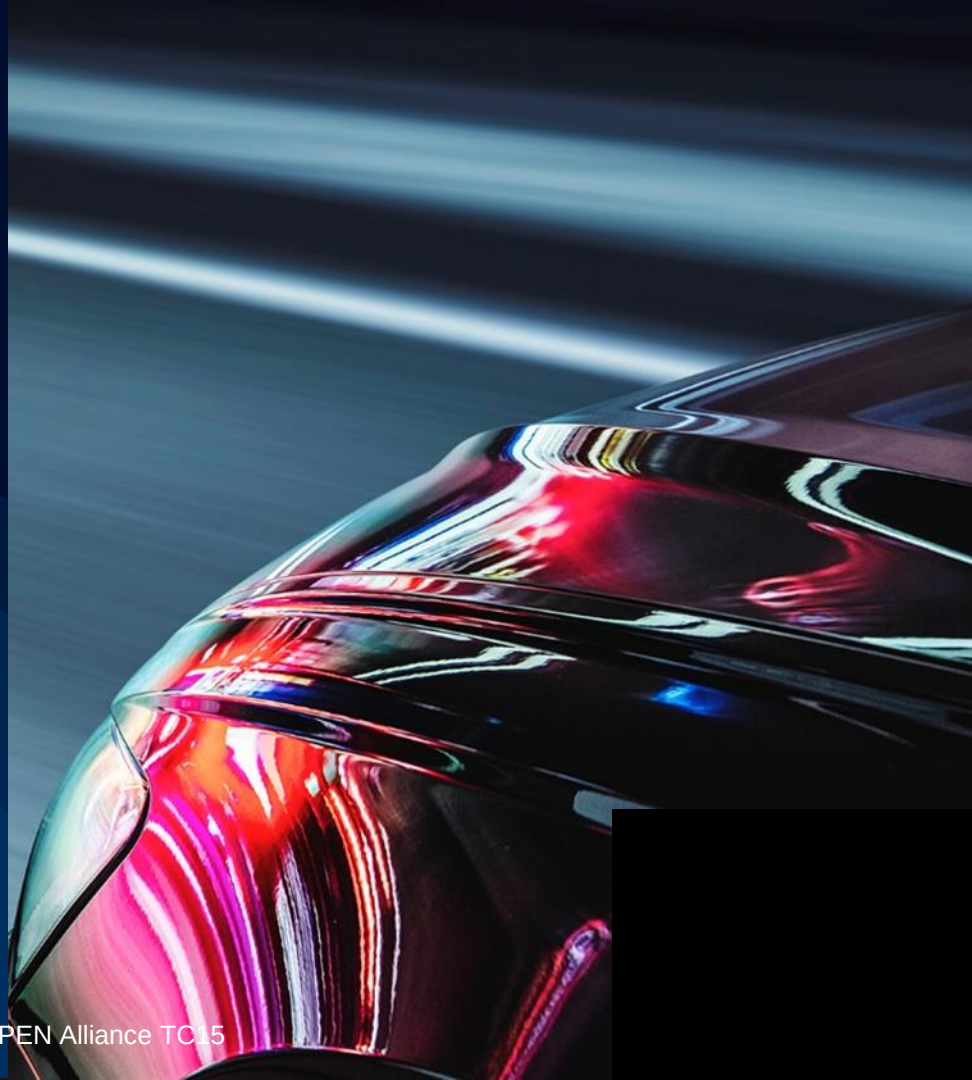
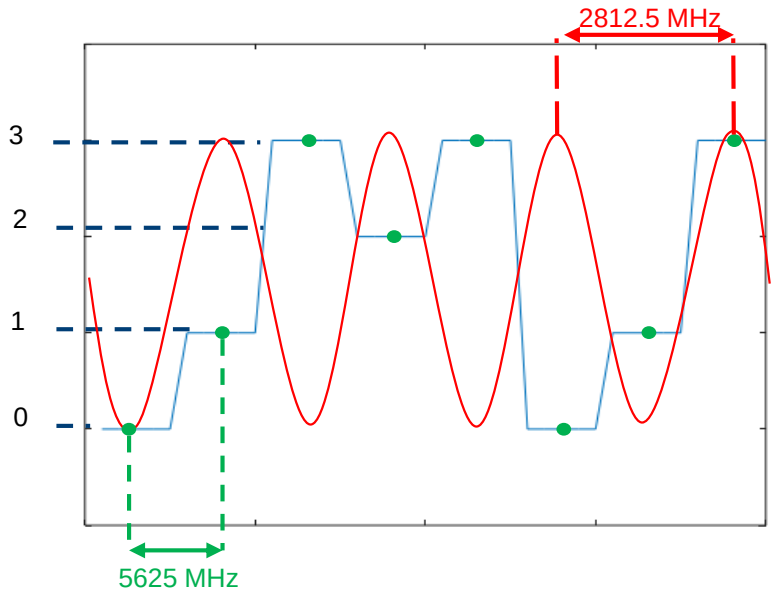
- PHY Layer compliance testing
- Q&A session



BAUD RATES

PHY Type	Symbol Rate	Associated 'S' Value See Table 149-1	Highest Output Frequency
10GBASE-T1	5625 Mbaud	1.0	2812.5 MHz
5GBASE-T1	2812.5 MBaud	0.5	1406.25 MHz
2.5GBASE-T1	1406.25 MBaud	0.25	703.125 MHz

BAUD RATES



Key

PAM4 Sequence

Symbol Sample Time

Highest Output Frequency

IEEE 802.3CH CLAUSE 149 TEST PATTERNS TABLE 149-17

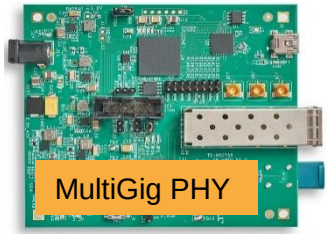
149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.



MultiGig PHY

MDI fixture

R&S®RTP oscilloscope

TEST MODE 1

149.5 PMA electrical specifications

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Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- “Normal operation” test mode
- Transmit reduced PHY symbol clock (TX_TCLK_175)
- Clock frequency of 175.78125 MHz
- Access through SMA connector or pin header

TEST MODE 2

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
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Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

TEST MODE 2.1

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

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Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

- 175.78125 MHz square wave
- Measures MDI random jitter

TEST MODE 2.2

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
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Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

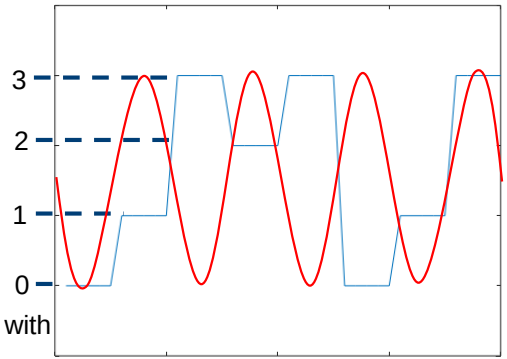
Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

- High frequency (sine wave) test pattern
- PAM4 encoded {0,3} sequence
- Measures MDI deterministic jitter

PAM4 Sequence

JP03A



TEST MODE 2.3

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
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Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

- Mixed frequency test pattern
- PAM4 encoded sequence of {0,3} (15x) + {3,0} (16x)
- Inserts “33” and “00” every 30 symbols
- Measures MDI Even-Odd jitter

TEST MODE 4

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
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Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- Used for transmitter linearity
- PRBS13Q – “Q” for quad or 4-level PRBS
- 8191 symbol sequence created from Gray coding two PRBS13 patterns into PAM4 symbols

TEST MODE 5

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- Used for TX PSD / Power level
- Scrambled PAM4 symbols
- MASTER mode scrambler from idle sequence

TEST MODE 6

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

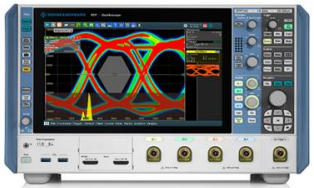
149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- Low frequency square wave for measuring TX droop
- {+1} (128x) + {-1) (128x)

OA COMPLIANCE TESTING PHY LAYER SUMMARY

	R&S®RTP	Max freq. 16GHz	OA TC8 & OA TC15 Supports speeds up to 10GBASE-T1
	R&S®RTO6	Max freq. 6GHz	OA TC8 & OA TC15 Supports speeds up to 2.5GBASE-T1
	R&S®ZNB	4-port VNA 9kHz – 40GHz	OA TC9, OA TC8 & OA TC15 8GHz VNA sufficient for 10GBASE-T1

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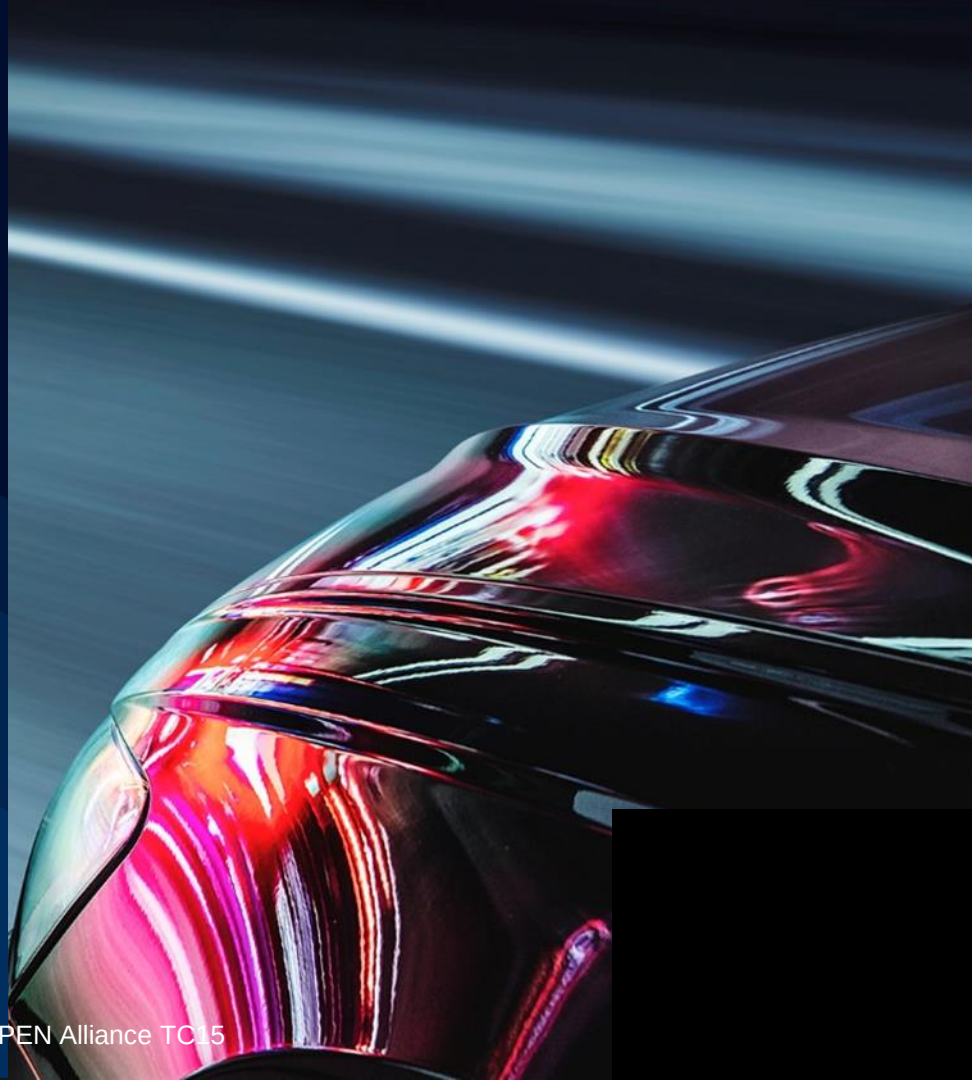
- PHY Layer compliance testing
- Q&A session



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