Webinar

5-STEPS TO A REALTIME EYE DIAGRAM

SIGNAL INTEGRITY DEBUGGING

Guido Schulze, Product Manager Oscilloscopes
Dr. Mathias Hellwig, Application Engineer Oscilloscopes

ROHDE&SCHWARZ

Make ideas real

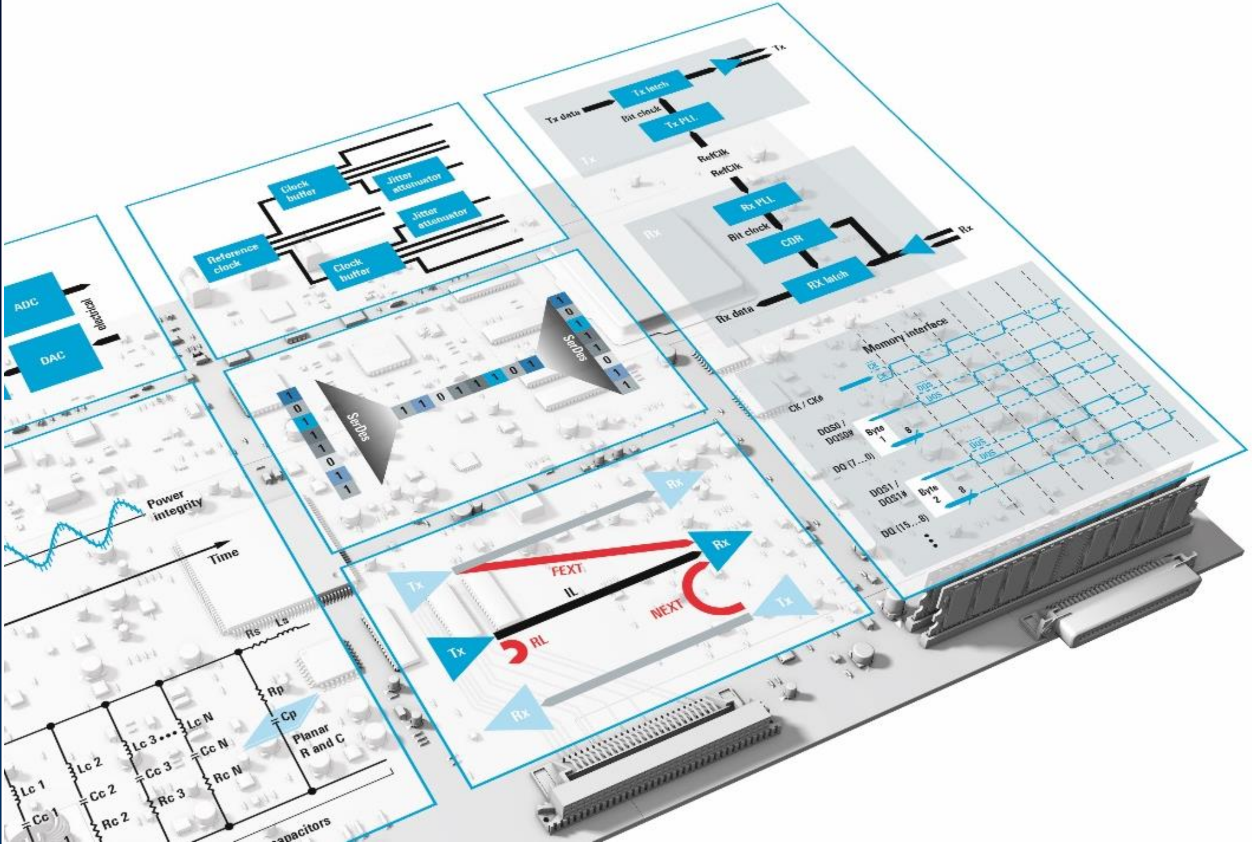
OUTLINE

- ► What can go wrong on Highspeed Interfaces
- ► Approaches for Signal Integrity Debugging
- ► Eye Diagram Basics
- ► 5-Steps to a Realtime Eye
  - – Differential Signal
  - – Clock-Data-Recovery
  - – Eye Diagram Analysis with Mask and Histogram
  - – Serial Pattern Trigger
  - – Channel Deembedding
- ► Live-Demonstration
- ► Summary

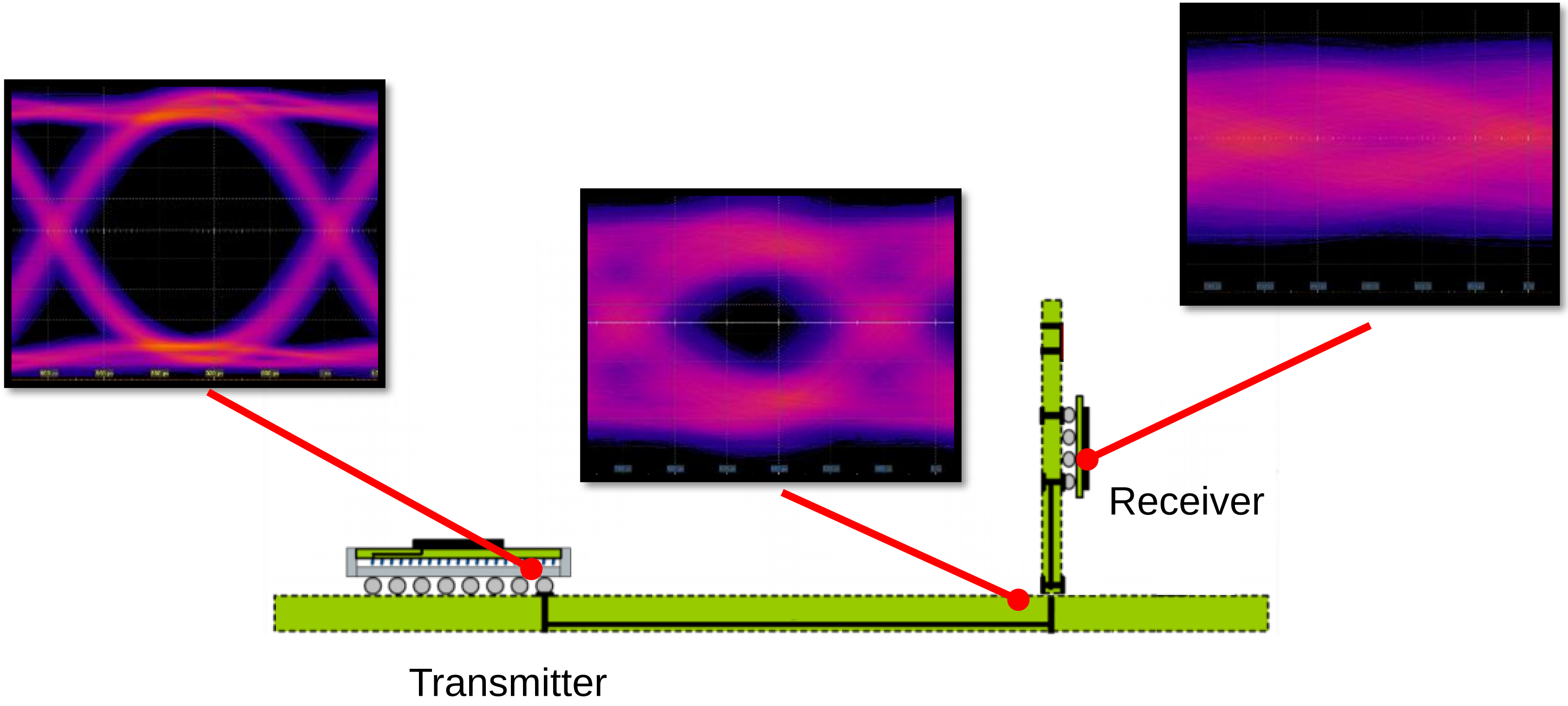
HIGHSPEED DIGITAL INTERFACES

- ► Signal integrity challenges due to increasing data rates
- ► Interference issues due to increasing level of integration

Signal Integrity analysis: T&M needs to collect statistical data fast.

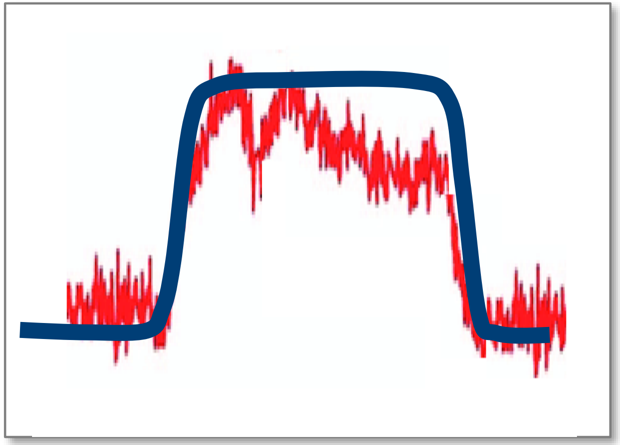


HIGH SPEED DIGITAL INTERFACES
WHAT COULD POSSIBLY GO WRONG?



HIGH SPEED DIGITAL INTERFACES
COMMON SIGNAL INTEGRITY PROBLEMS

- Channel-related effects
  - Ringing (overshoot/undershoot)
  - Signal loss/attenuation
  - Crosstalk
  - Reflections due to impedance mismatches
- Transmitter effects
  - Rise/fall imbalance
  - Timing jitter
- External sources (can be intermittent)
  - EMI within or from outside the components in the system
  - Noise from power and distribution networks
  - Interferer from other functional cores

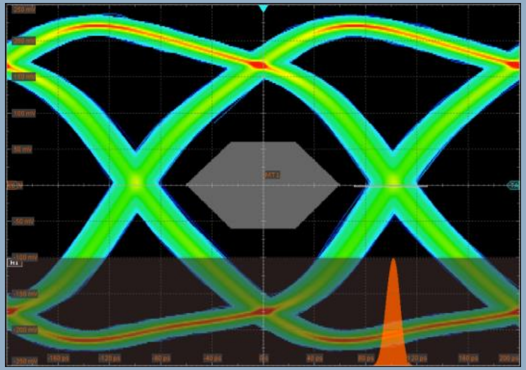


HIGH SPEED DIGITAL INTERFACES

Dedicated Tests for Verification & Debugging

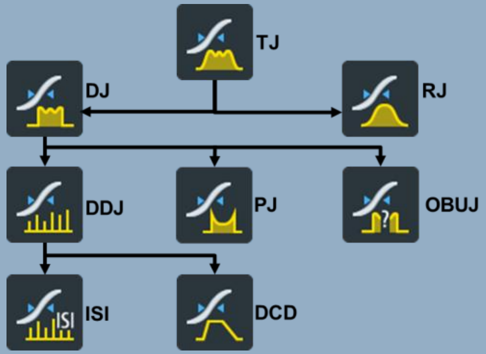
Eye Diagram

- Fast update rate for statistical confidence
- Clock-Data-Recovery (CDR)
- Mask tests, Histogram



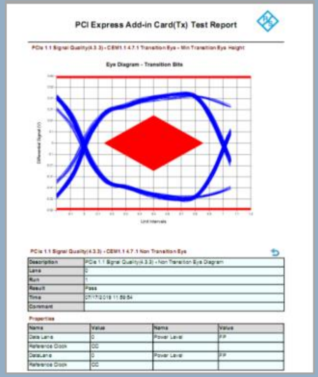
Jitter Analysis

- Break-down of jitter and noise into individual components for characterization & debugging



Automated Compliance Tests

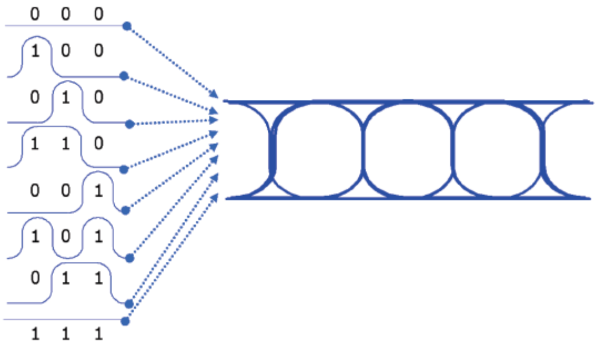
- Verify compliance of the physical layer to interface standards and report results



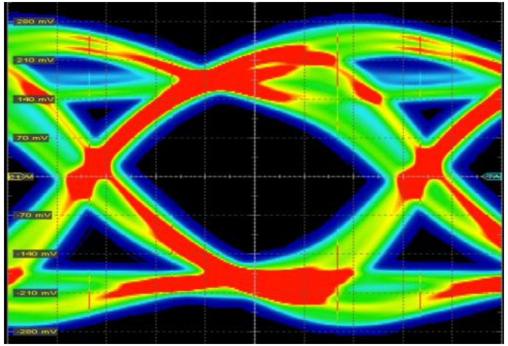
EYE DIAGRAM BASICS

EYE DIAGRAM
INTRODUCTION

► Intuitive graphical tool for the evaluation of the quality and integrity of data signals
► Generated by superposition of multiple signal waveform segments aligned to well-defined reference time instants
  – Waveform segments commonly correspond to a data symbol
  – Reference clock provides timing information for alignment (e.g. symbol start instant)

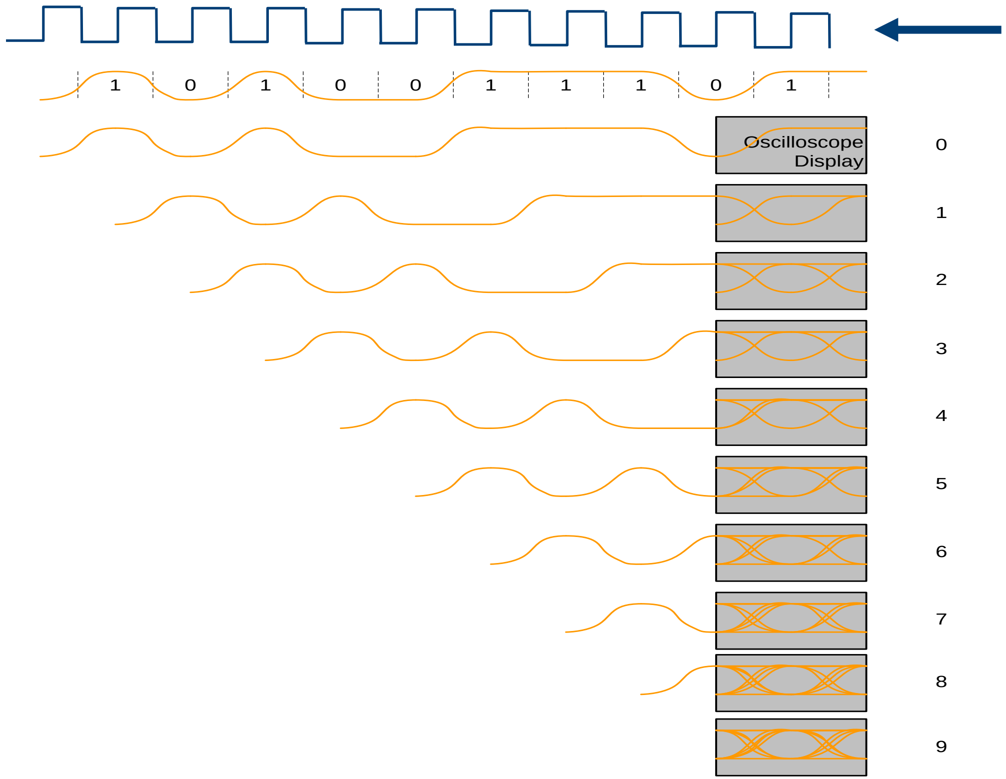


Superposition of bit sequences form the eye diagram



Eye diagram with color-coded frequency

GENERATING EYE DIAGRAMS

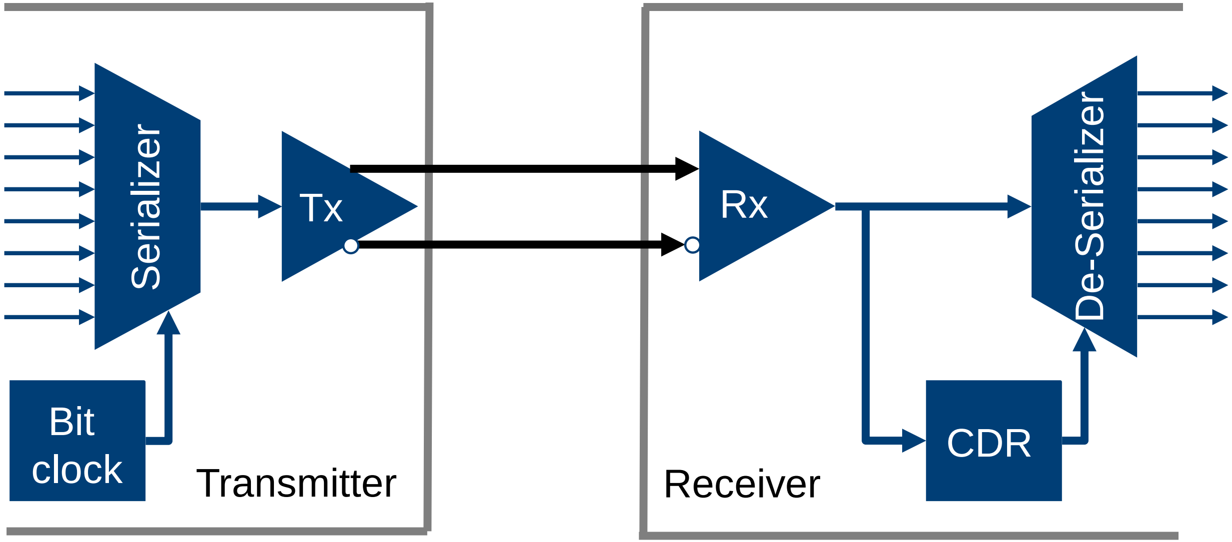


Reference clock
Triggers oscilloscope

Waveform is sampled synchronous with the bit rate of the signal and randomly over time

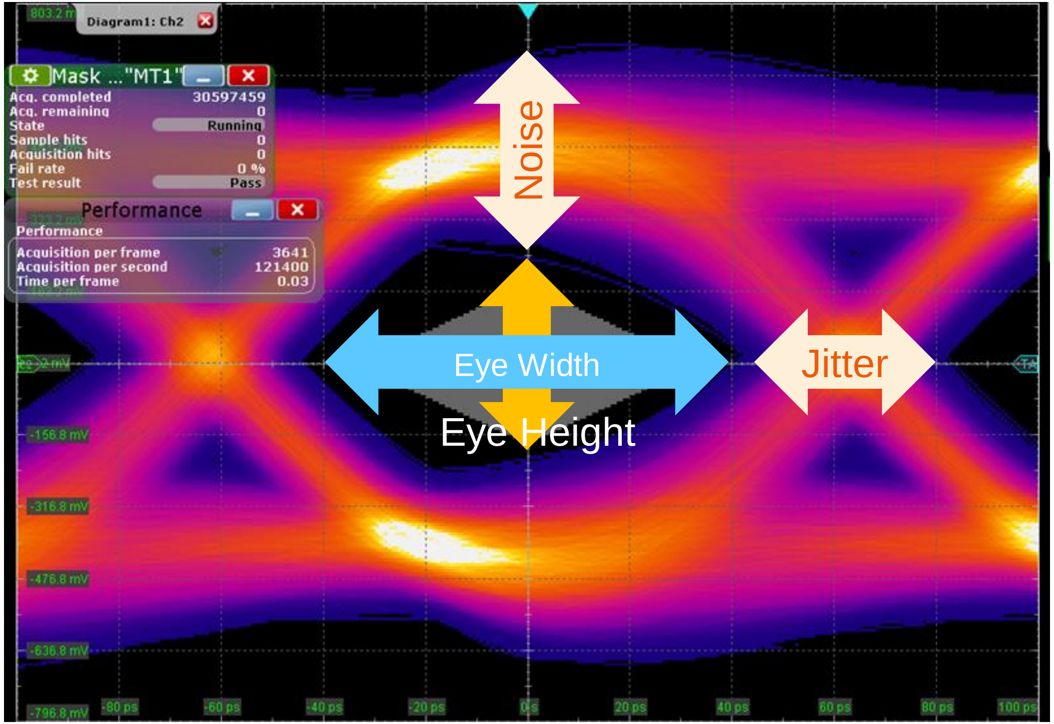
REFERENCE CLOCK GENERATION FOR EYE DIAGRAMS
CLOCK-DATA-RECOVERY

- ► Timing Reference can be from a reference clock (parallel clock signal) or from the data signal itself (embedded clock signal)
- ► Clock data recovery is typically uses a Phase Locked Loop (PLL) or Delay Looked Loop (DLL)



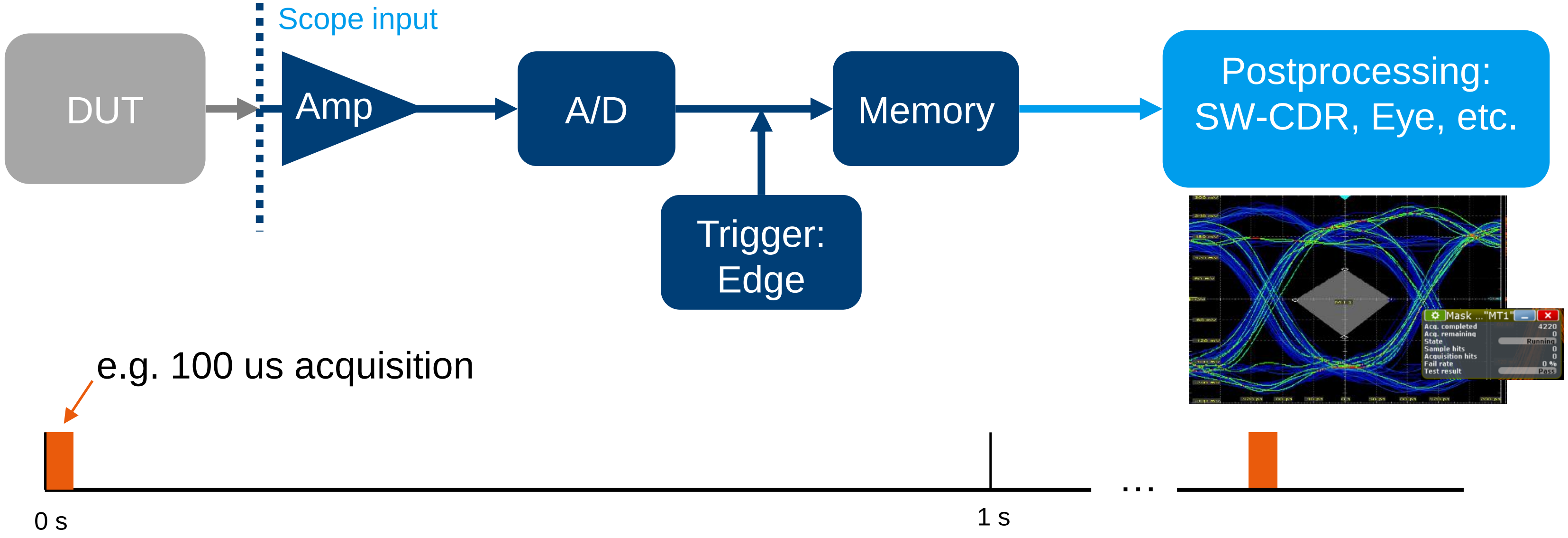
INFORMATION CONTAINED IN AN EYE DIAGRAM

- Timing jitter: peak to peak, standard deviation
- Noise: peak to peak, standard deviation
- Eye width: the minimum time interval over which no signal transition will occur
- Eye height: the minimum amplitude over which the signal level occur
- Eye parameters are based on statistics and require large sample size for repeatable measurements



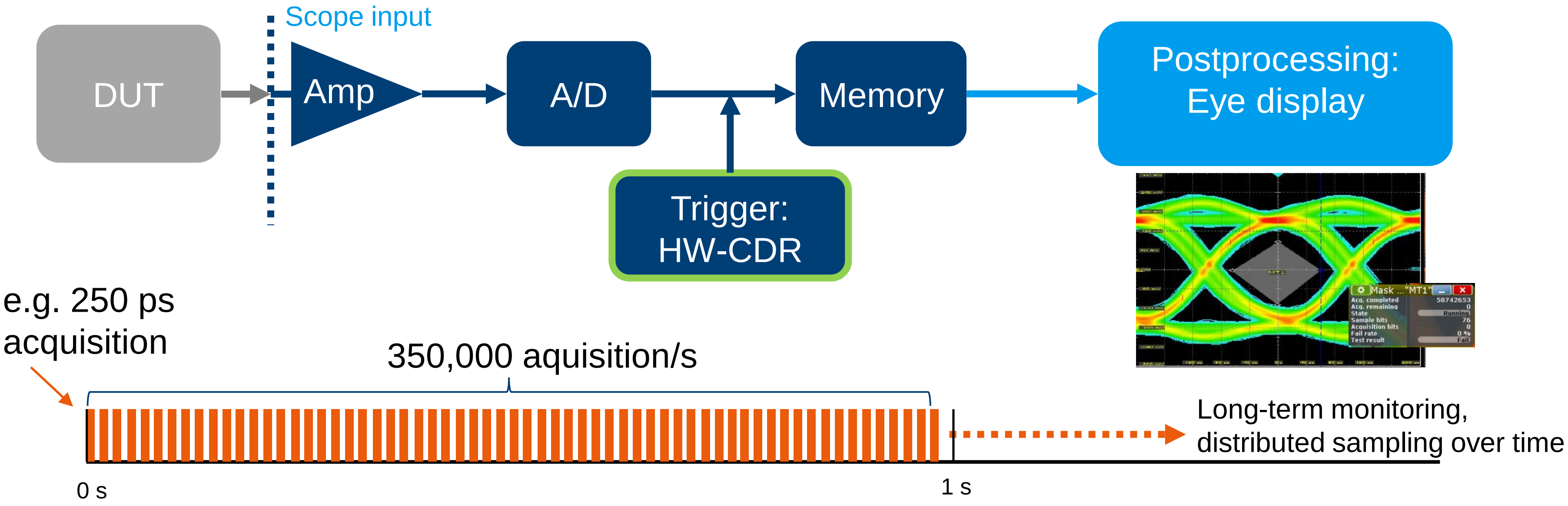
Eye Diagram in Post-Processing

- ► Analysis based on a single acquisition with long Record length and SW-CDR in postprocessing
  - – Acquired waveform is “folded” over into an eye based on software recovered clock
  - – CDR – settling time (typ. >10us) and new synchronization for every new acquisition



Realtime Eye Diagram

- ► Analysis based on a multiple acquisition, short Record Length and CDR in Hardware
  - – Acquired bits are overlaid to an eye based on HW-CDR timing
  - – CDR – looked once and runs continuously

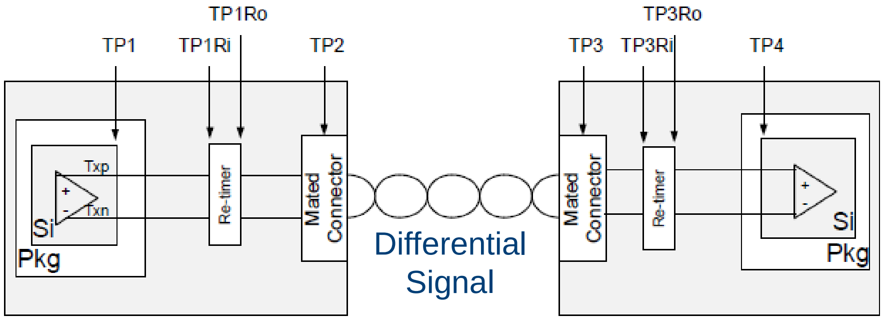


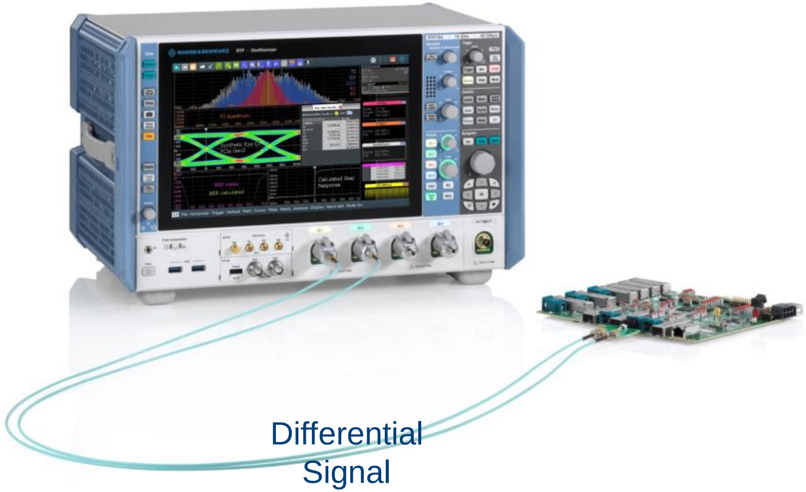
5-STEPS TO A REALTIME EYE DIAGRAM

1. DIFFERENTIAL SIGNALS

- Highspeed interfaces use typically differential signals
- Connection to test equipment with two cables

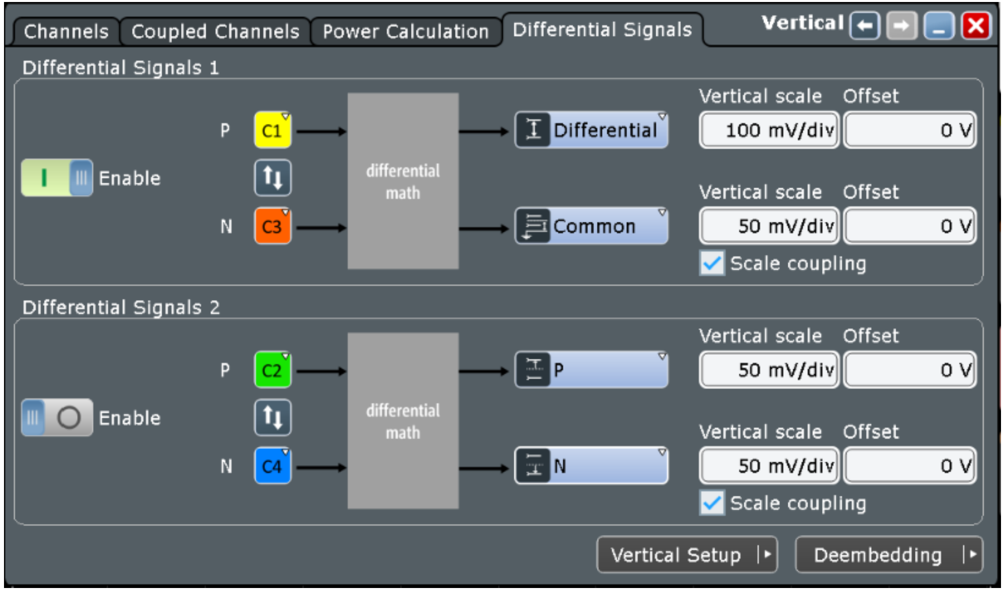
- Challenge:
  - Trigger on differential signal
  - Analyze differential or common mode signal
  - Common mode conversion





1. DIFFERENTIAL SIGNALS
ROHDE & SCHWARZ SOLUTION

- **Differential Math block in realtime acquisition path**
- **Setup step 1:**
  - Connect 2 scope channels to differential signal of the DUT
  - Switch on differential math with Differential and Common Mode signal as output.
- **Advantages:**
  - Trigger on true V_{diff} or V_{CM}
  - No math in post-processing
  - Fastest analysis on differential signals

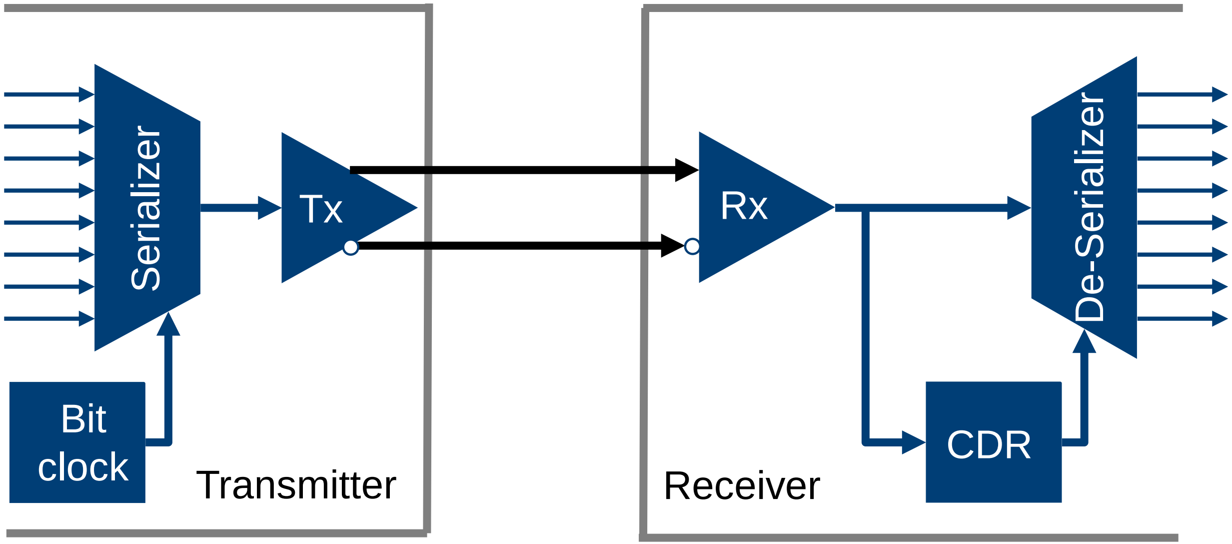


2 input signals (P/N):
- any input signals of the scope

2 output signals:
- P-Signal / N-Signal, or
- Differential Signal (V_{diff}), or
- Common Mode Signal (V_{CM})

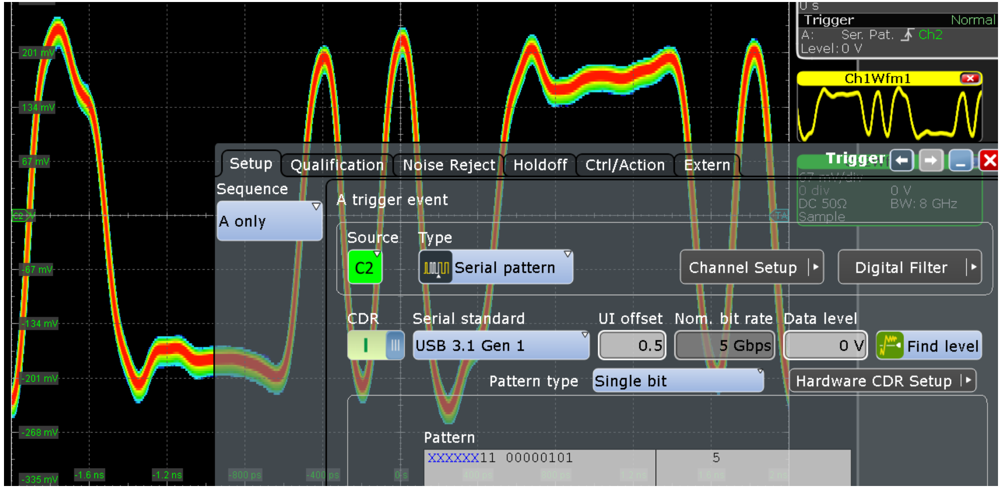
2. CLOCK DATA RECOVERY (CDR)

- Highspeed Serial Signals use an embedded Clock
- CDR is used to extract embedded clock
- Challenges:
  - Derive triggering timing from embedded clock signal



2. CLOCK DATA RECOVERY
ROHDE & SCHWARZ SOLUTION

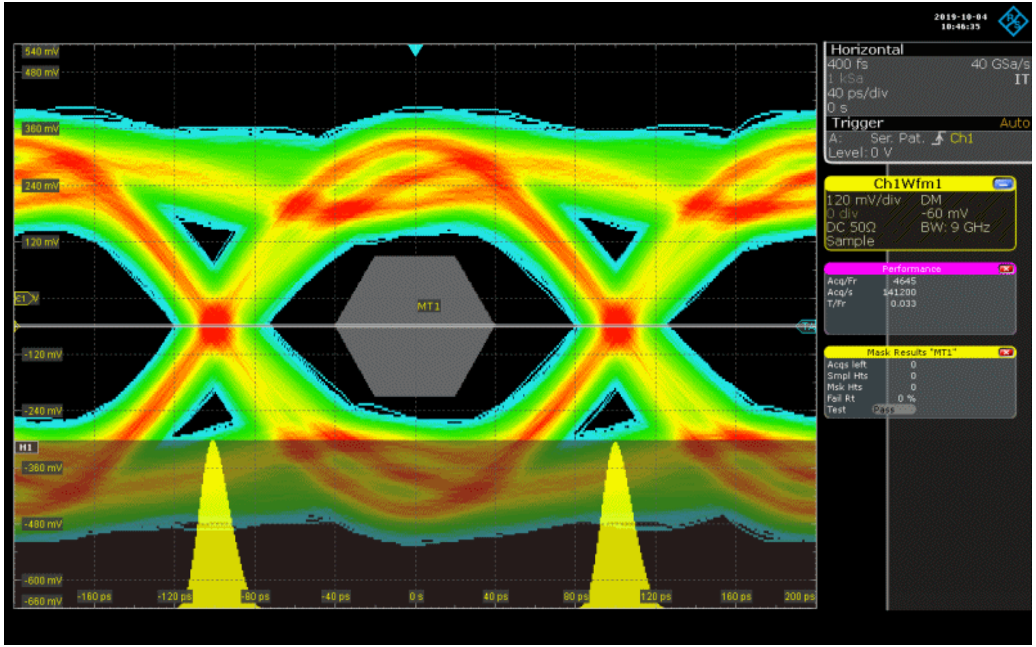
- **8 / 16 Gbps HW-based CDR option**
- **Setup step 2:**
  - Select „Serial Pattern“ as trigger event
  - Enable CDR and select Serial standard to define Nominal bit rate
- **Advantages:**
  - Trigger on true V_{diff} or V_{CM}
  - No math in post-processing
  - Fastest analysis on differential signals



3. MASK TEST AND HISTOGRAM

- Use Mask test to validate open eye
- Use Histogram to verify jitter and noise

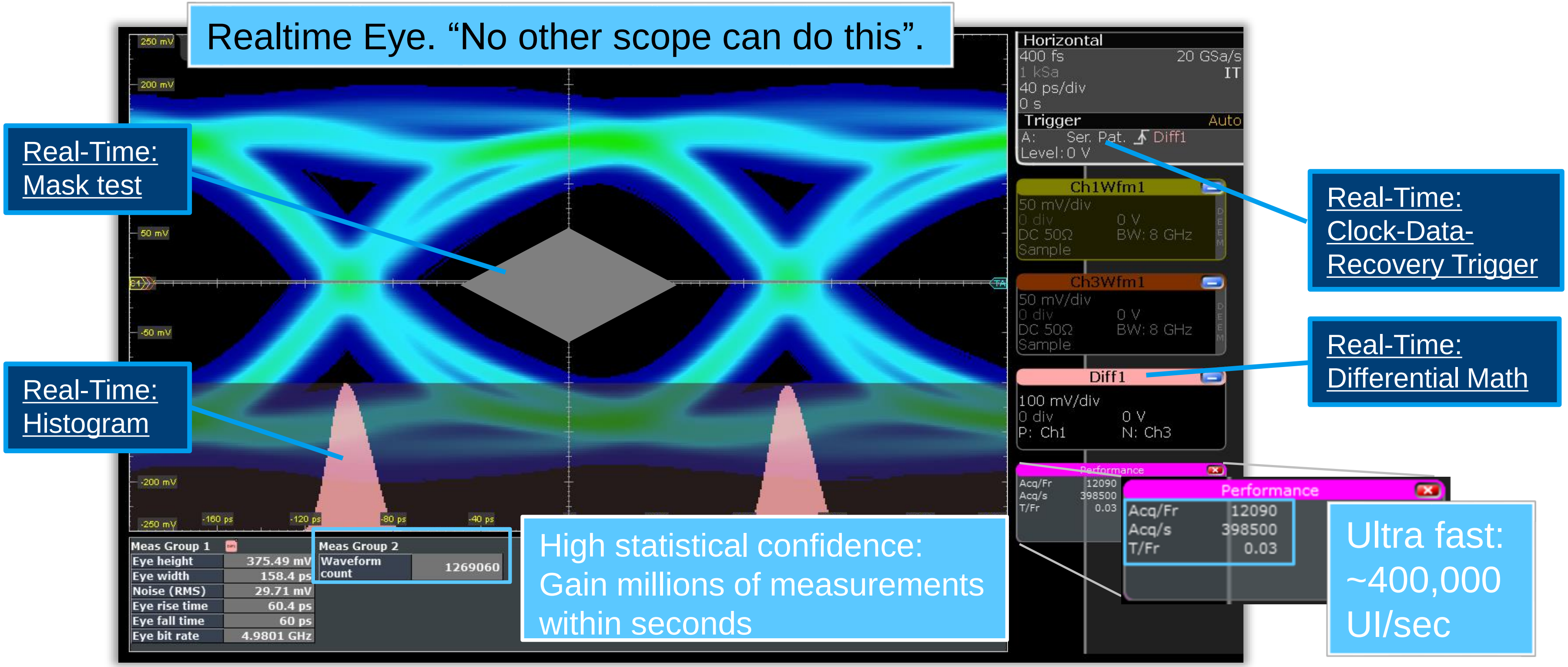
- Challenges:
  – Collect enough data for high statistic *confidence*



Histogram at the Eye edge

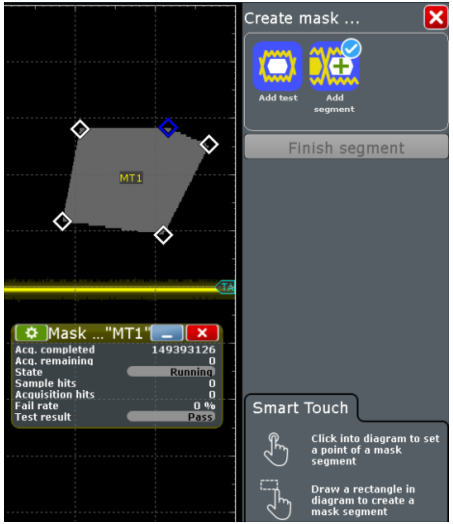
Mask in the Eye center

3. FASTEST MASK TEST AND HISTOGRAM ANALYSIS
ROHDE & SCHWARZ SOLUTION

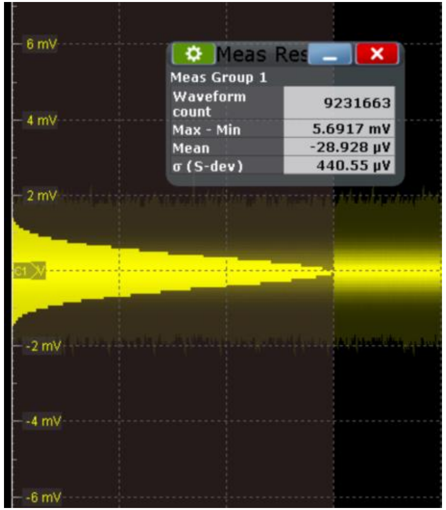


3. MASK TEST AND HISTOGRAM ANALYSIS
ROHDE & SCHWARZ SOLUTION

- ▶ **Max. 750,000 wfms/s**
- ▶ **Hardware Mask & Histogram**
- ▶ **Setup step 3:**
  - – Define Mask at the display or load defined masks
  - – Define histogram at the display and add automated measurement
- ▶ **Advantages:**
  - – Fastest collection of data bits
  - – Catch rare interferer
  - – Monitor long-term behaviour



Easy Mask test definition at the display

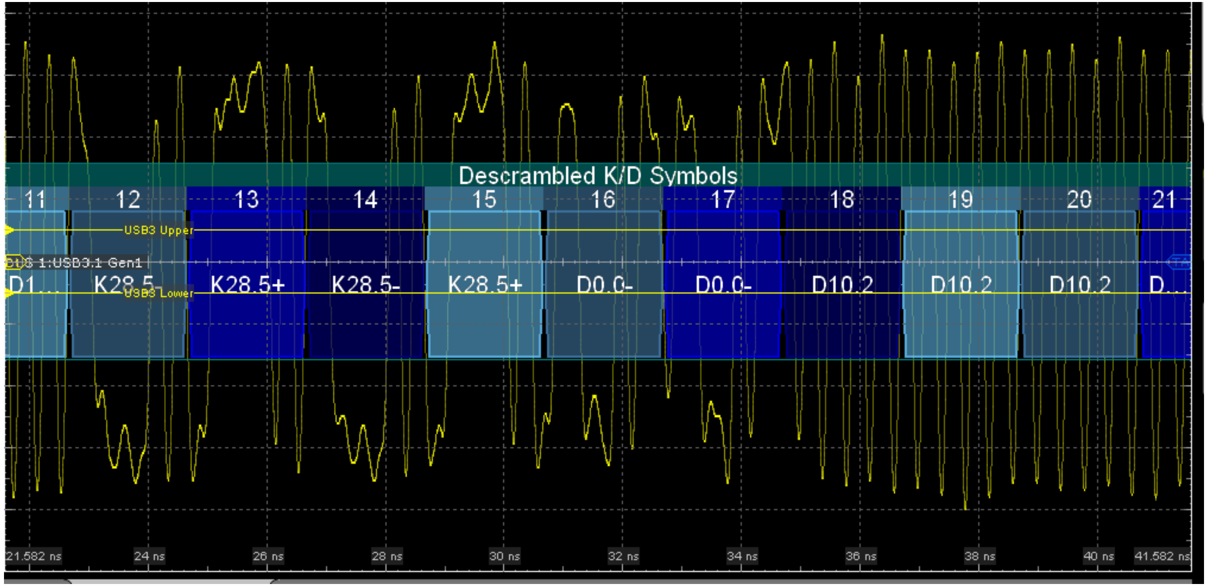


Vertical histogram with statistics

4. SERIAL PATTERN TRIGGER

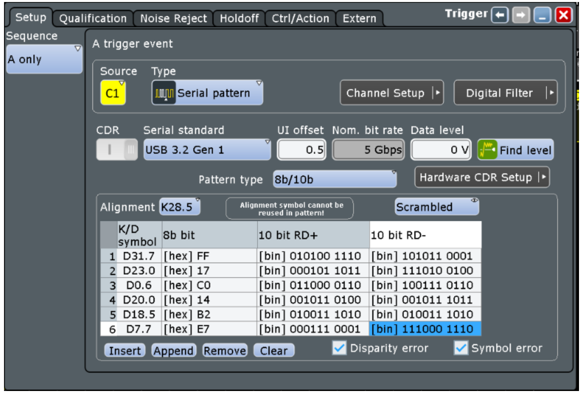
- Highspeed serial interfaces use line coding

- Challenge:
  - Trigger in realtime on specific code pattern



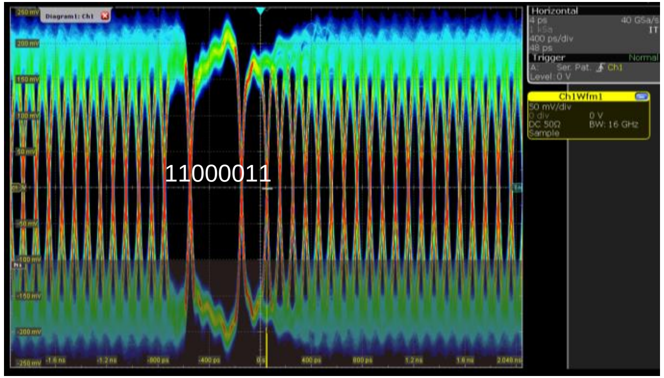
4. SERIAL PATTERN TRIGGER
ROHDE & SCHWARZ SOLUTION

- 8 / 16 Gbps Serial Pattern and HW-based CDR options
- **Setup step 4:**
  - Select „Serial Pattern“ as trigger event
  - Define Alignment and Trigger pattern
- **Advantages:**
  - Industry highest data rate
  - Powerful triggering capabilities
    - Up to two time 160 bits w/ OR
    - 8B10B, 128B/130B, 128B/132B
    - PRBS errors, etc.
  - Catch all possible events



Highspeed serial pattern trigger

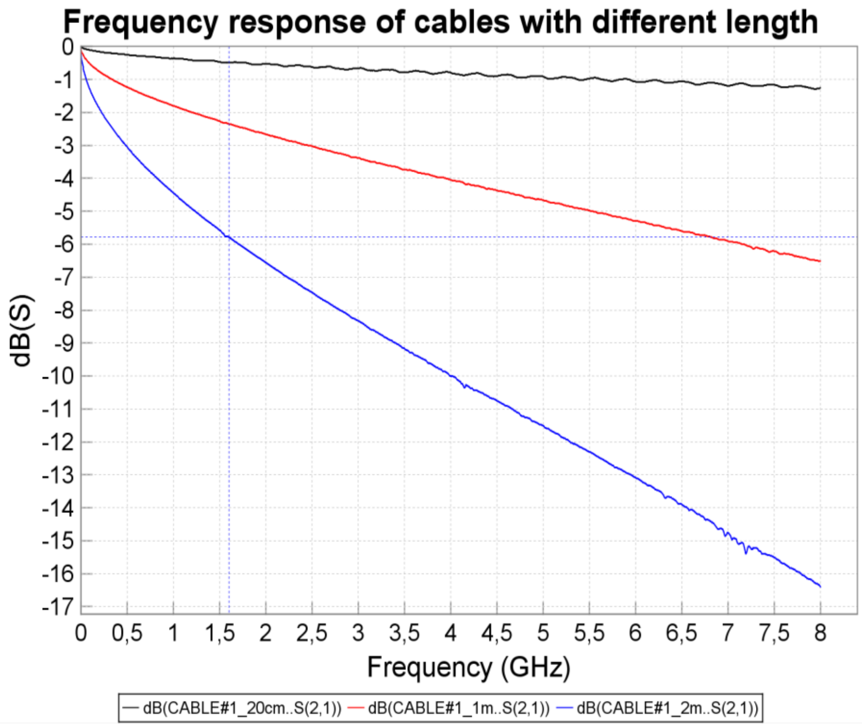
USB3.2 Gen2 Data Eye w/ serial pattern trigger



5. DEEMBEDDING CABLE LOSS

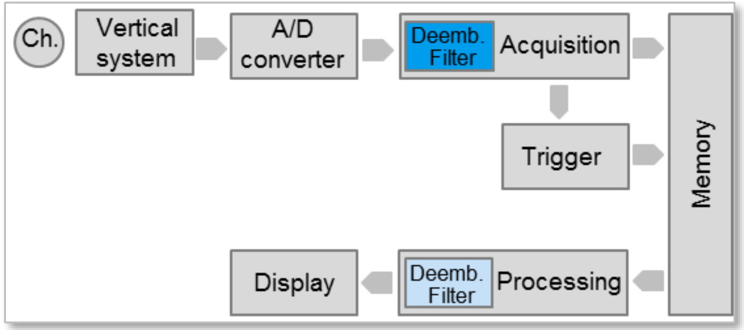
- Probes, cables and fixtures have non ideal frequency response.

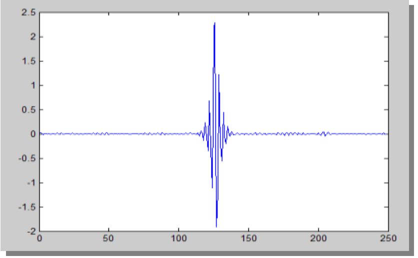
- Challenge:
  - Correction of transmission loss effects in post-processing is slow



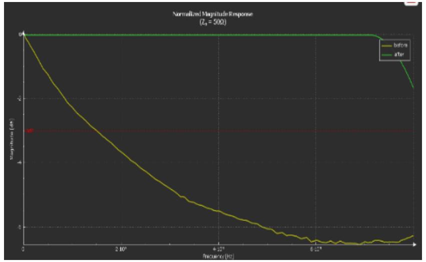
5. DEEMBEDDING
ROHDE & SCHWARZ SOLUTION

- ▶ **Realtime Deembedding:**
  - Clustered FIR filter structure in acquisition path
  - Configurable Filter design based on imported S-Parameters
- ▶ Full FIR filter structure in post-processing
  - Correction of arbitrary (complex) responses





Calculation of FIR filter (IFFT) based on imported S-Parameters

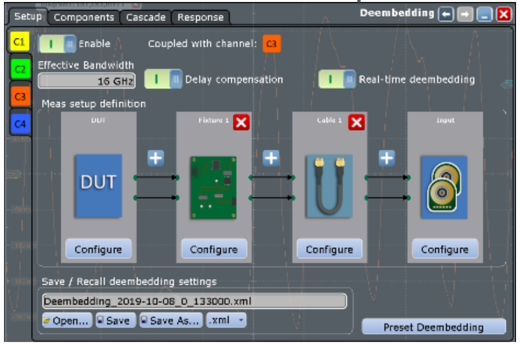


Corrected Frequency response (green)

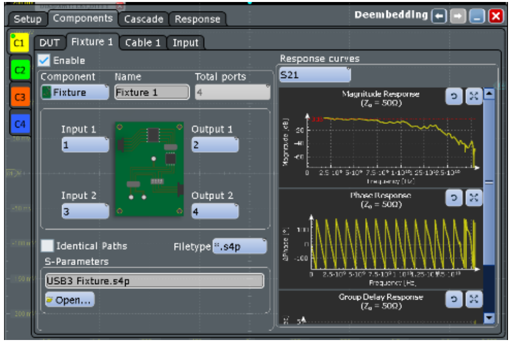
5. DEEMBEDDING
ROHDE & SCHWARZ SOLUTION

- **Deembedding and HW-acceleration options**
- **Setup step 5:**
  - Define deembedding path based on imported S-Parameters
- **Advantages:**
  - Enables highest update rate
  - Allows math and triggering on corrected signals

Define Measurement path

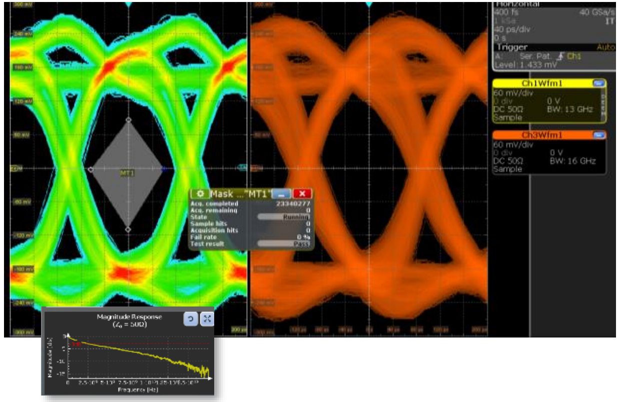


Import S-parameter



Analyse corrected signals

„lossy“ cable „ideal“ cable



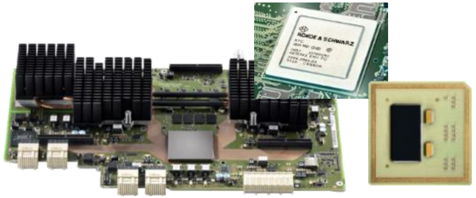
Realtime Signal Integrity

R&S RTP HIGH-PERFORMANCE OSCILLOSCOPE

Realtime Signal Integrity up to 16 GHz

R&S RTP HIGH PERFORMANCE OSCILLOSCOPE

	4 GHz	6 GHz	8 GHz	13 GHz	16 GHz
2-Ch Sample Rate	40 Gsample/s				
4-Ch Sample Rate	20 Gsample/s				
Memory Depth	50 Msample Std, 2 Gsample Max				
CDR/Serial Trigger	Up to 8 Gb/s			Up to 16 Gb/s	
Pulse source	16 GHz differential				
Standard Warranty	3 Years				



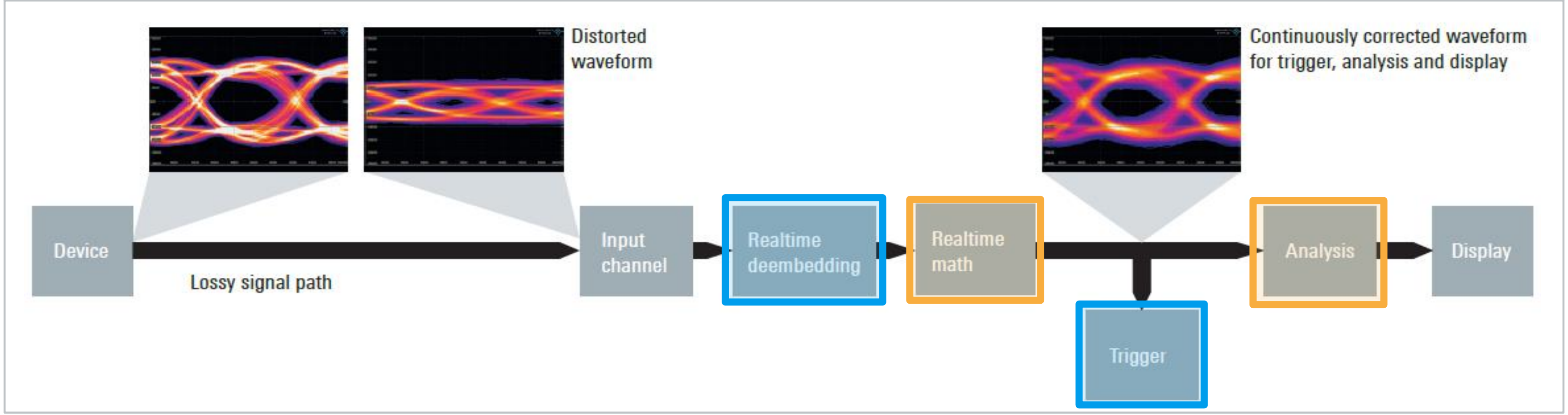
Realtime Deembedding

16 GHz TDR / TDT

750,000 Waveforms/sec

REALTIME SIGNAL INTEGRITY UP TO 16 GHZ

Realtime Deembedding Architecture



Fast debugging
- ► 20 GSa/s: 750k wfm/s
- ► 40 GSa/s: 300k wfm/s

RT-Deembedding:
- ► Realtime transmission loss compensation

Realtime Math:
- ► V_{Diff} signal
- ► V_{CM} signal

Digital Trigger System:
- ► 16 Gbps Serial Trigger/CDR
- ► 25 ps glitch trigger

HW accelerated analysis:
- ► Mask Test
- ► Histogram

No time consuming post-processing

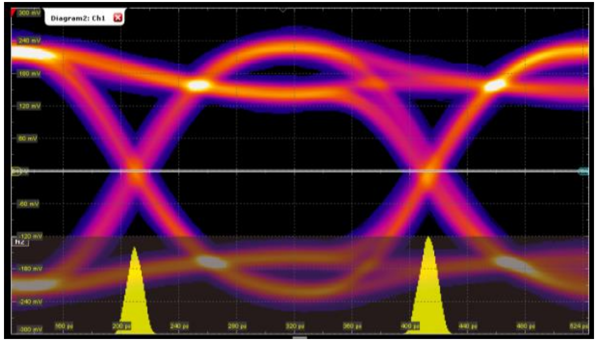
LIVE DEMO

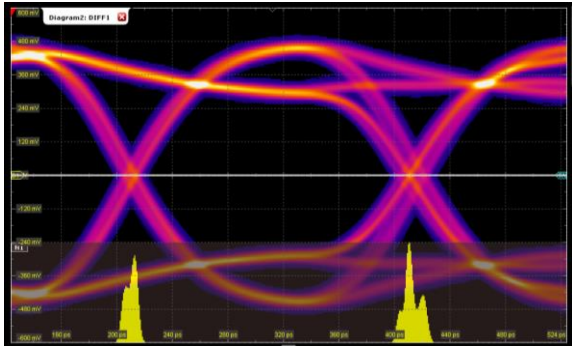
LIVE DEMO
RESULTS – 1 MILLION WAVEFORMS

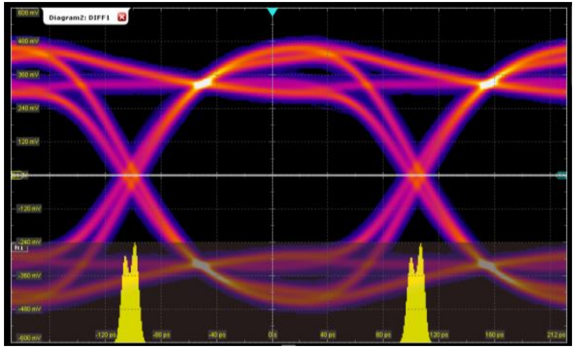
Trigger:
Edge
Single-ended

Trigger:
Edge
Differential

Trigger:
HW-CDR
Differential





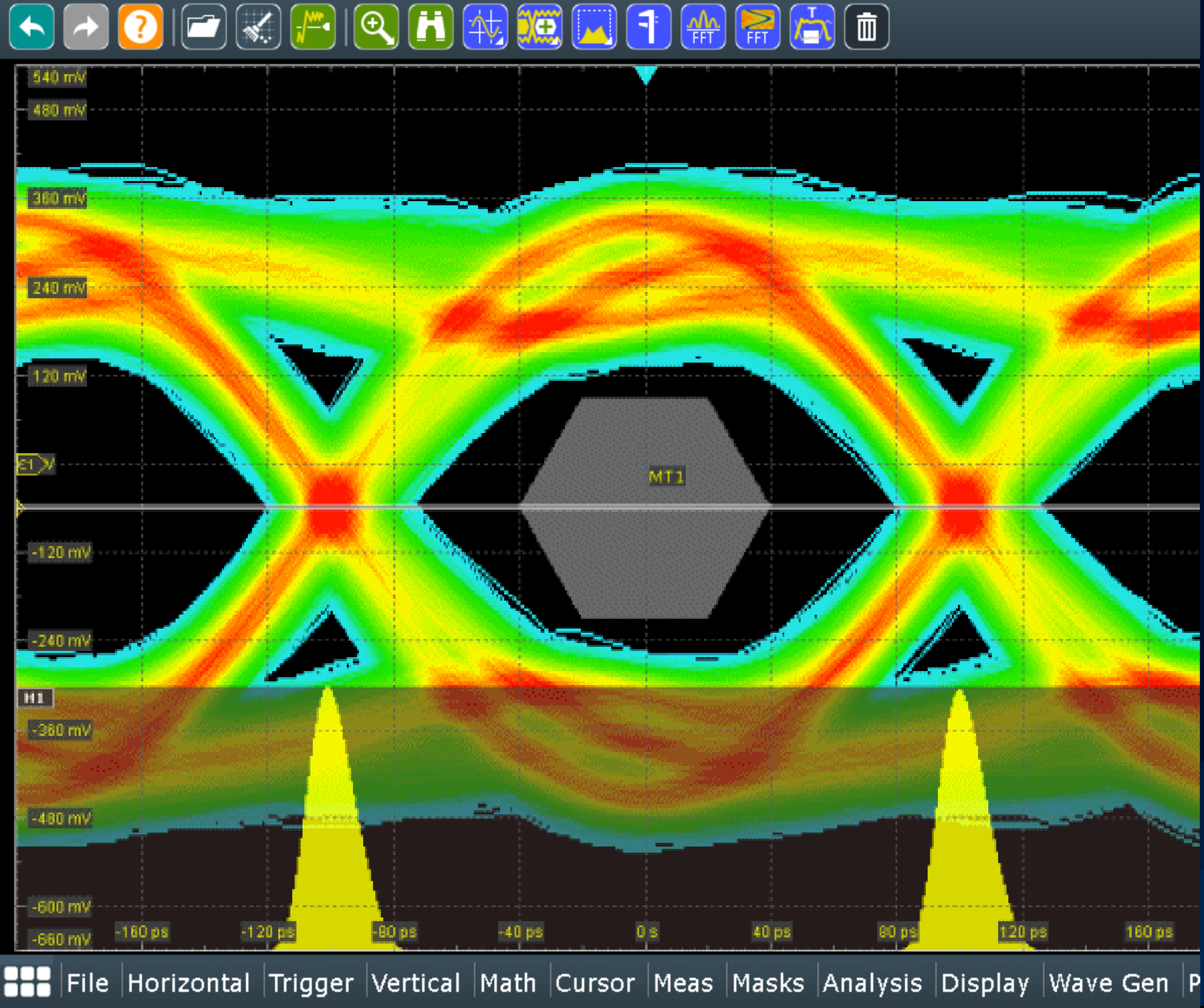


Depending on position	Depending on position	Independent on position
S-dev: 5.1 ps	**4.16 ps**	**4.46 ps**
PP: 36.5 ps	**27.7 ps**	**30.1 ps**
Extinction ratio 93.4 %	**104.3 %**	**102.9 %**
Q factor 7.6	**7.9**	**8.3**

SUMMARY

SUMMARY – A FRESH LOOK AT SIGNAL INTEGRITY
ULTRA FAST EYE DIAGRAMS

- ► Traditional measurements of eye diagram
  - – Based on a single acquisitions
  - – SW-CDR in post-processing
- ► HW clock recovery enables realtime eye diagram
  - – Fastest approach to high statistical confidence
  - – RTP oscilloscope offers additional HW support
    - Differential signal math
    - HW based mask and histogram
    - Realtime deembedding



ULTRA FAST EYE DIAGRAMS

- "Realtime" eye
  - Up to 750,000 UI/second
  - 16 Gbps HW CDR and Trigger
- Mask test, histogram, etc.
- Benefits:
  - Builds eyes in seconds
  - Analyze jitter characteristics
  - Catch rare interferer

*Updates @ 150k/s

Find out more

www.rohde-schwarz.com

Thank you!

Guido.Schulze@Rohde-Schwarz.com

Mathias.Hellwig@Rohde-Schwarz.com

ROHDE & SCHWARZ

Make ideas real