Oscillosope Introduce and Application

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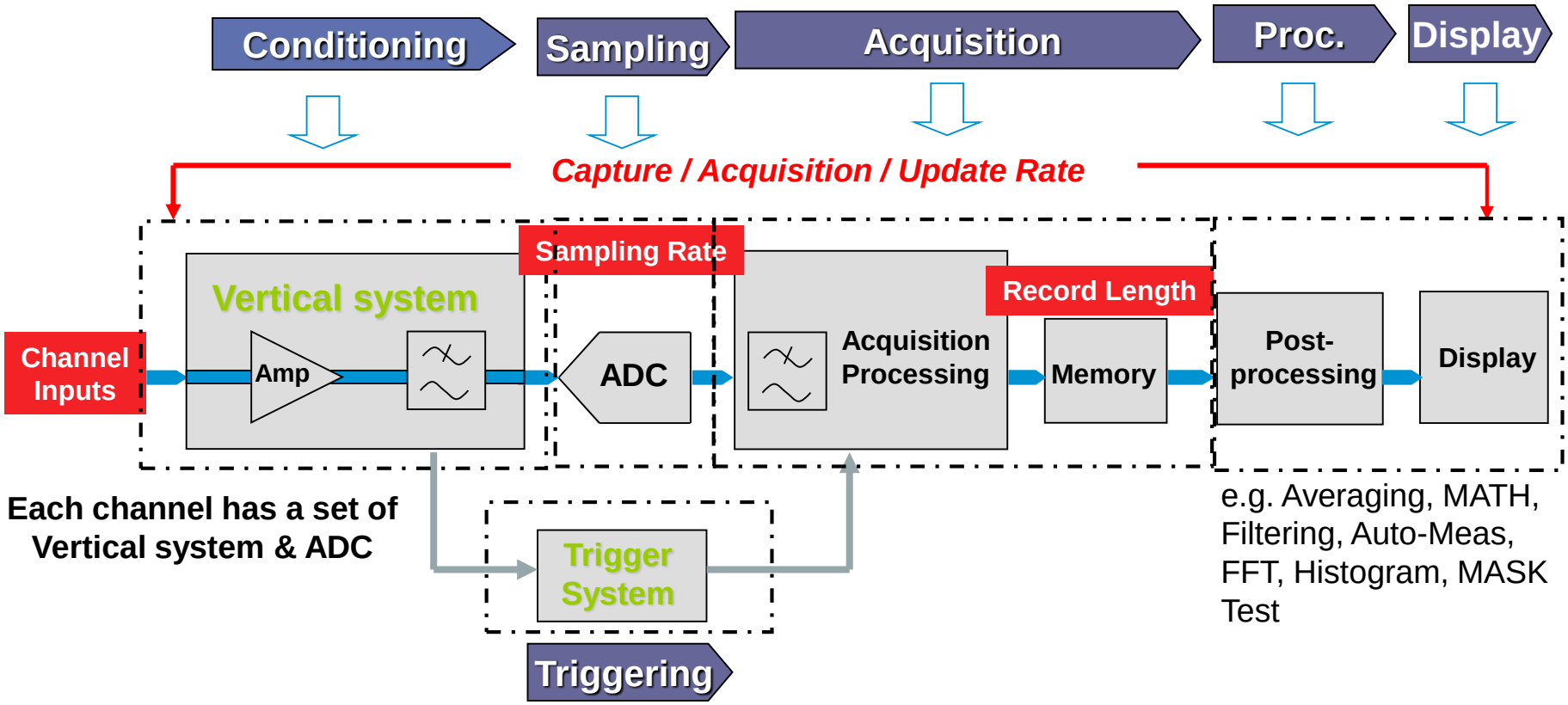
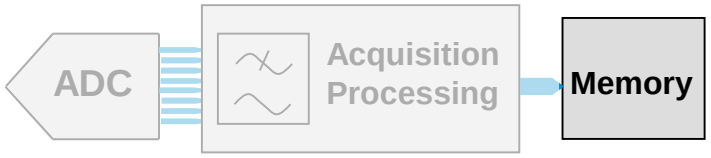
ROHDE&SCHWARZ

Architecture vs Specifications



Oscilloscope Record Length

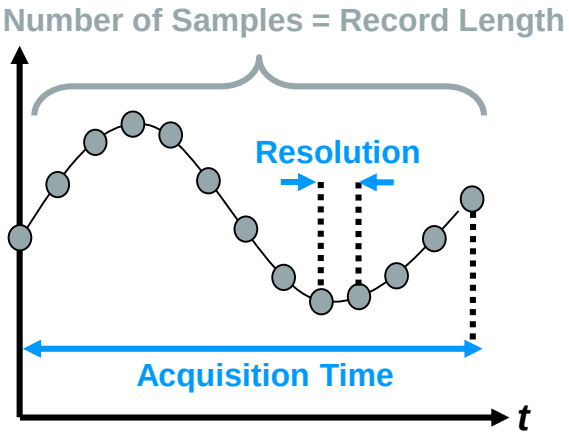


- Record Length is the total number of sampling point in an acquisition of the signal.

Acquisition time

Sample Rate / 1 / Resolution X Time Scale X # of Div's = Record Length

e.g. 10 GS/s X 100 ps/div X 10 Div's = 10 samples



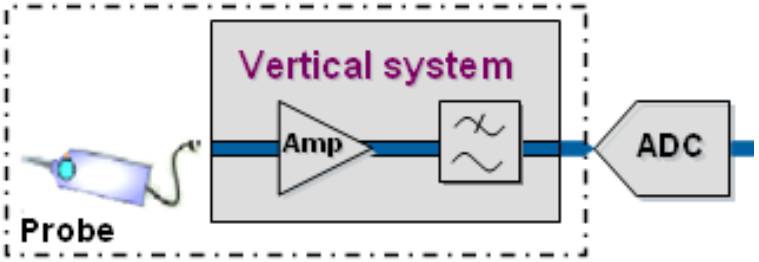
- Scope has a finite memory, thus choosing a suitable sampling rate and time scale is critical for user to determine the record length needed for observing the waveform.

Signal processing requires memory too, heavy signal processing can result in drop in record length

System Bandwidth Considerations

Filtering :

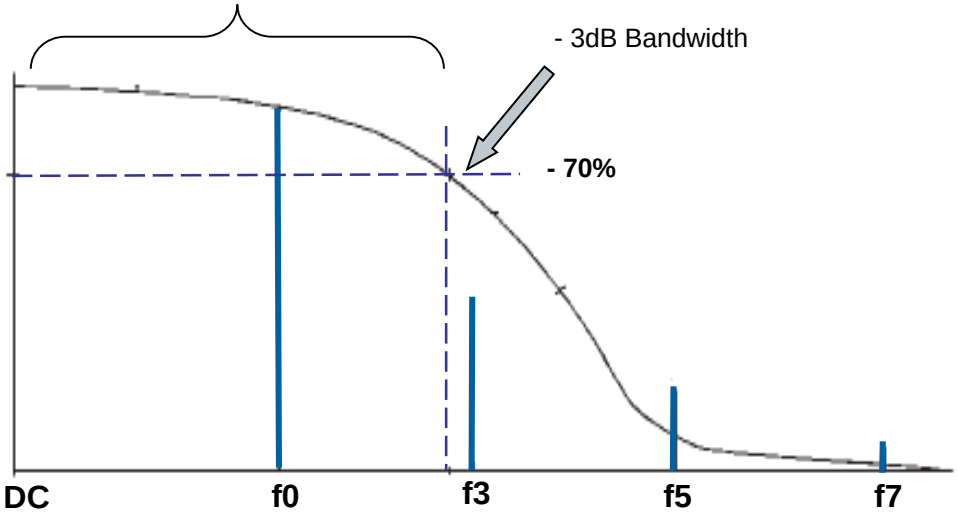
Due to the system (probe + scope) bandwidth, higher frequencies tend to be attenuated (bandwidth limitation)

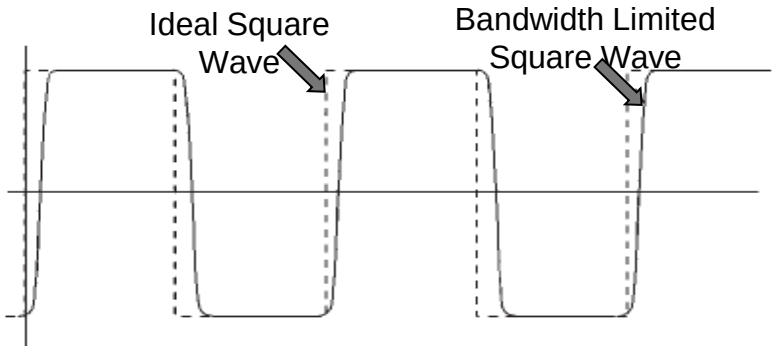


$$\left(\frac{1}{BW_{system}}\right) = \sqrt{\left(\frac{1}{BW_{probe}}\right)^2 + \left(\frac{1}{BW_{scope}}\right)^2}$$

1GHz BW Scope + 1 GHz BW Probe = System BW of 707MHz

System Bandwidth



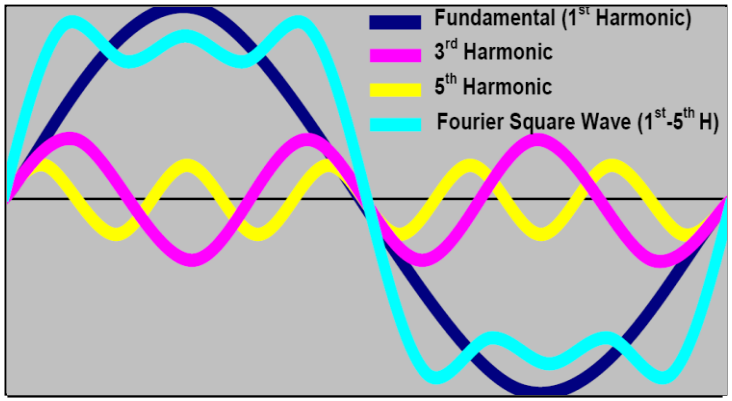


Bandwidth & Rise Time Considerations

Rise Time Measurement Accuracy

$$BW * t_{rise\_10\text{-}90} = 0.35$$

$$t_{rise\_10\text{-}90} = 0.35 / BW$$



- **Measured rise time depends on intrinsic rise time of the scope**

$$t_{rise\_measure}^2 = t_{rise\_intrinsic}^2 + t_{rise\_signal}^2$$

- **Example:**
  - maximum 3% error for 2 ns rise time
  - limit of measured rise time: 2.06 ns
  - <=0.5 ns intrinsic rise time (~700 MHz Bandwidth)

Vertical System

Channel Input

BNC Input Channel

4 Analog Channels

Input Impedance

Input Voltage Rating

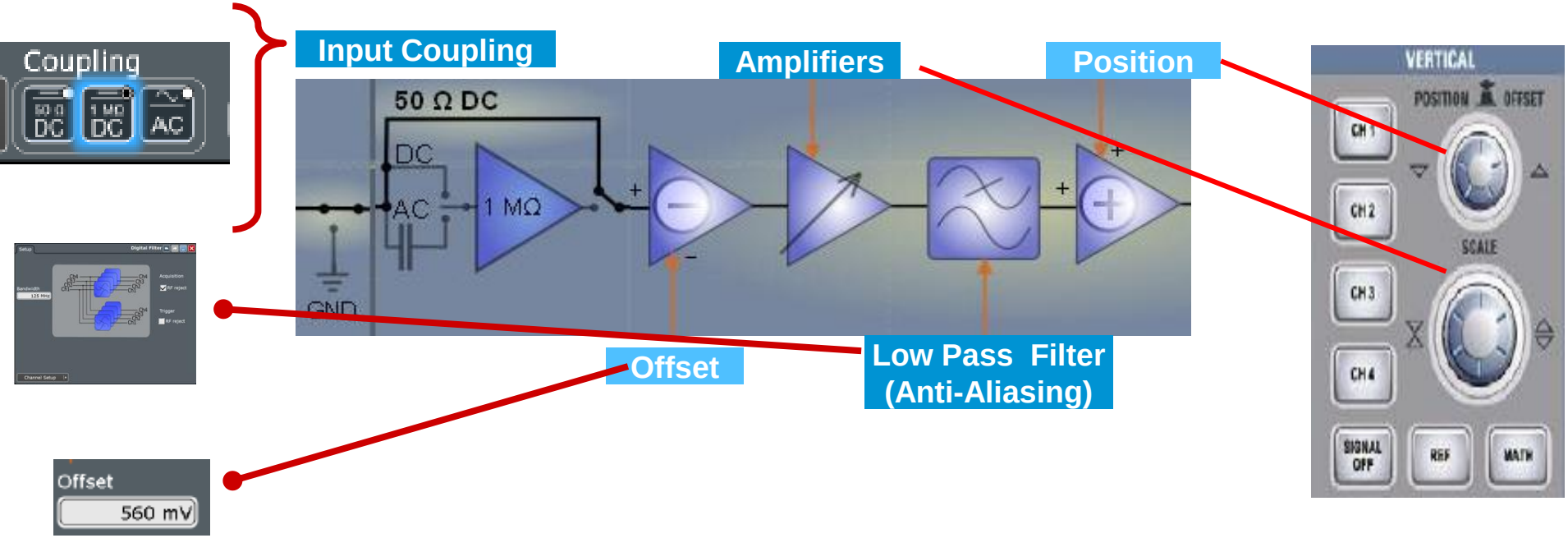
- Input is either 2 or 4 Channels
- Input Voltage Rating: Installation Category I or II
- Active Probe is not compatible with other vendors, but it is able to use a converter for achievement

+

Vertical System

Amplifiers

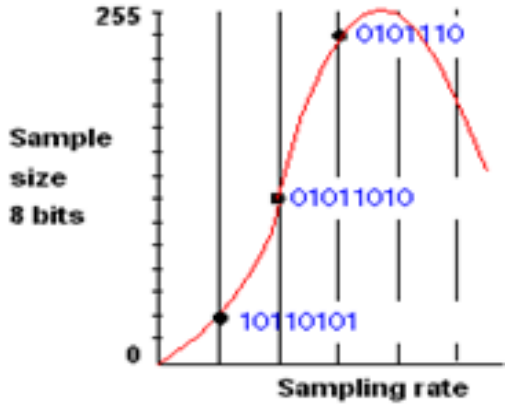
- Input sensitivity (typically): 1mV/div (0.5mV/div @HD model) … 5V/div in 1-2-5 steps
- Instrument usually has 3-4 set of Amplifiers by sensitivity range
- The higher sensitivity range set of amplifiers do have limitation on bandwidth.



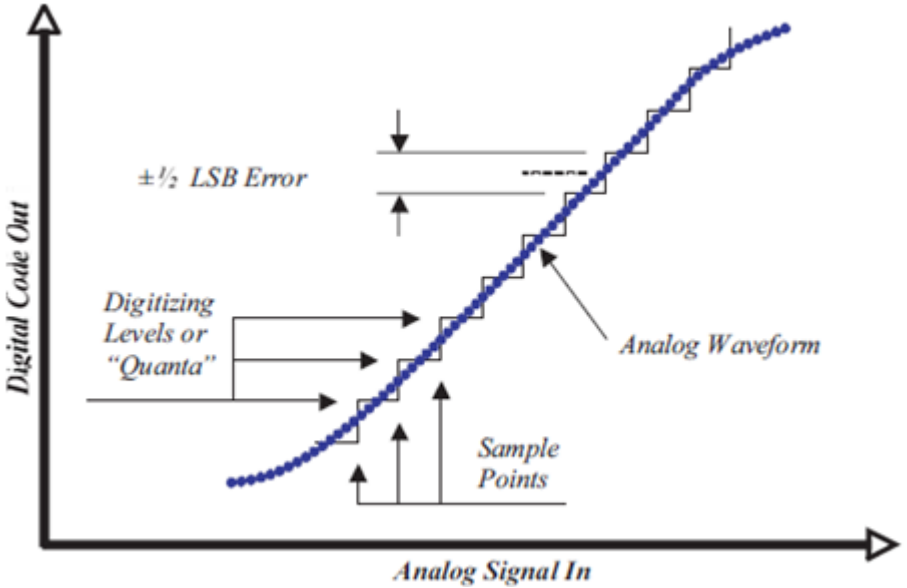
Digital Oscilloscope Architecture: Sampling & Acquisition

ADCs Vertical Bits Resolution

- An 8-bit ADC represent up to 256 quantization levels.
- A full-scale signal will utilize the full range of the ADC.



Resolution n	Digital Levels in Full Scale range: 2^n	At 1V Full Scale 1 LSB =
8-bit	256	3.9 mV
10-bit	1,024	976 µV
12-bit	4,096	244 µV
14-bit	16,384	61 µV
16-bit	65,536	1.5 µV



Note

Resolution ≠ **Accuracy**

Other possible considerations;
e.g. Noise floor, ENOB@V-scale, Input sensitivity etc…

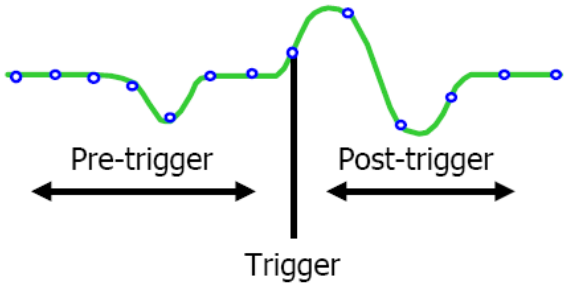
Triggering

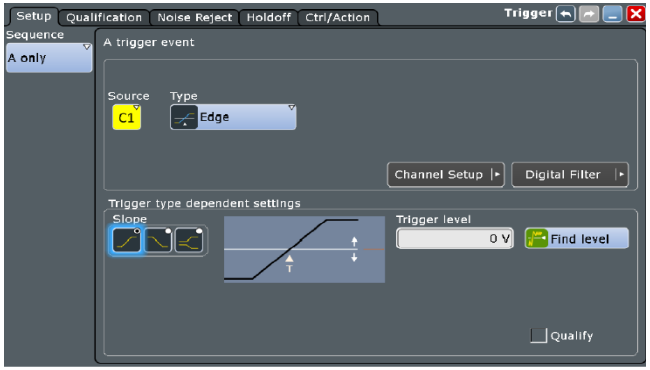
Trigger System

- Get stable display of repetitive waveforms

  -Howard C. Vollum and Jack Murdock invented the triggered oscilloscope in 1946, allowing engineers to display a repeating waveform in a coherent, stationary manner on the phosphor screen

- Isolate events & capture signal before and after event
- Define dedicated condition for acquisition start



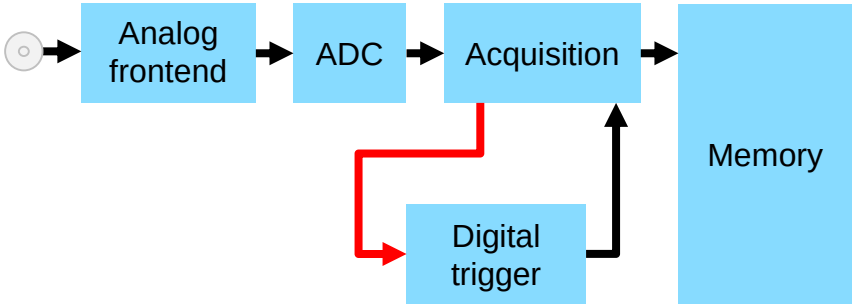


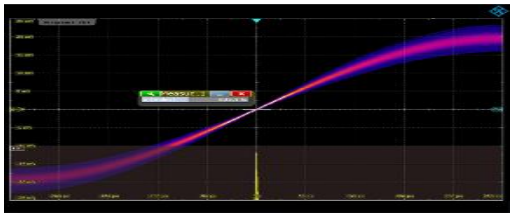
Trigger system basically work by aligning the position of all the samples that meet the required trigger condition relatively

R&S®RTx Features: Digital Trigger

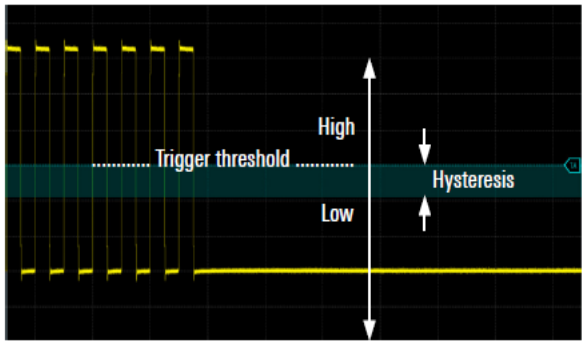
R&S® digital trigger:

- Identical path for trigger and acquisition

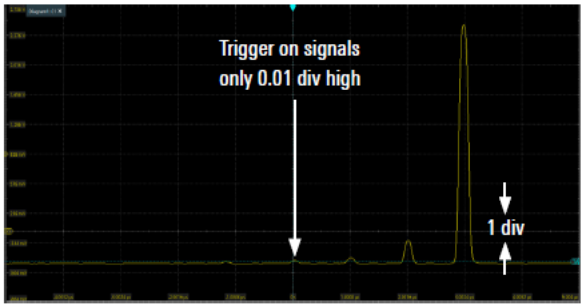




trigger jitter < 1 ps



- No mismatch between displayed signal and trigger point
- Signal processing of acquisition applicable to trigger signal (deskew, lowpass filter)



Overview

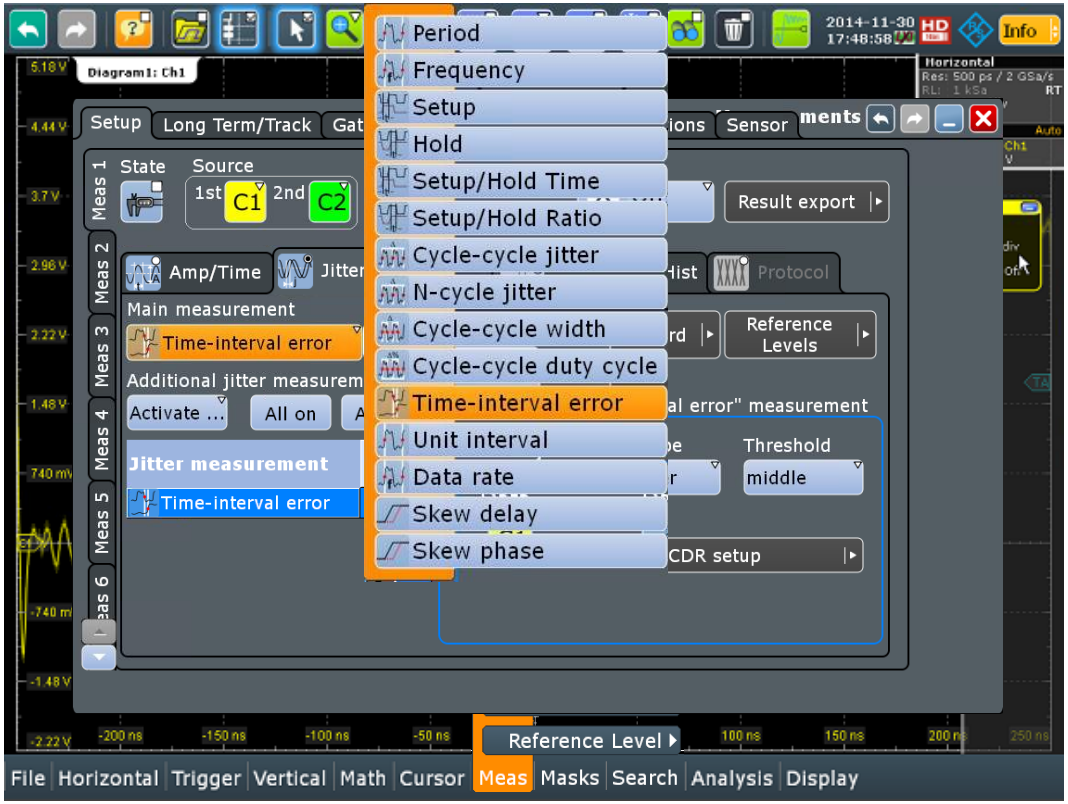
Analysis Tool for Clock & Eye

- **Statistics**
  - Cumulative measurement result to show mean, peaks & Standard Deviation of the result
- **Persistence**
  - Simple way to emulate phosphorous screen to measure spread of crossing points
- **Histogram**
  - Graphical representation of distribution of data. Supports to investigate jitter, noise & PDF of measurement value or waveform crossing
- **Track**
  - Track curve shows the measured results over time for acquired waveforms, revealing trend of changes with respect to time
- **Spectrum**
  - Display waveform in frequency domain to enable viewing of waveform from another intuitive dimension
- **Eye Diagram**
  - Overlaying of multiple waveforms Unit Interval to reveal signal deviations from reference define from embedded (CDR) or external clock

Jitter Measurements

Setting up

- With K12, users can now access automatic measurement for jitter related parameters



Jitter Measurements

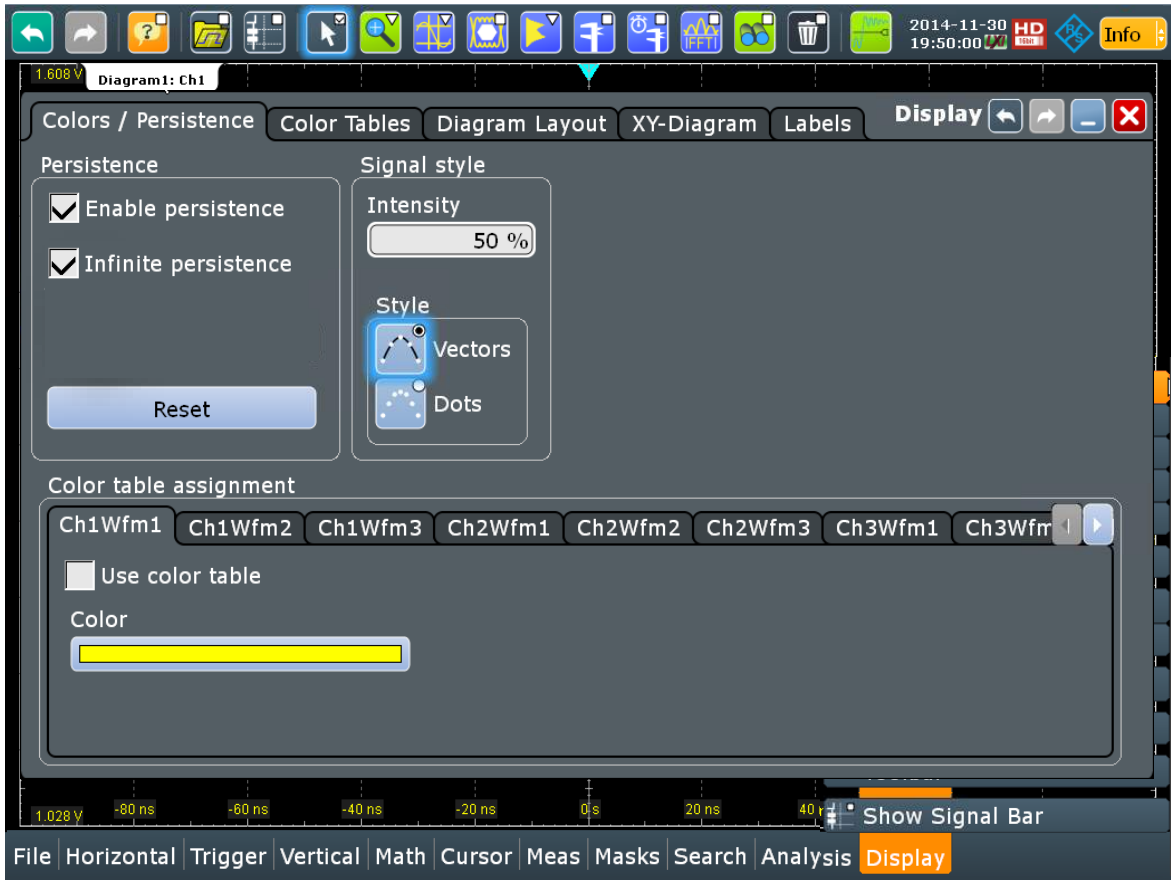
Statistics

- RTO statistics is a default feature

Persistence

Setting up

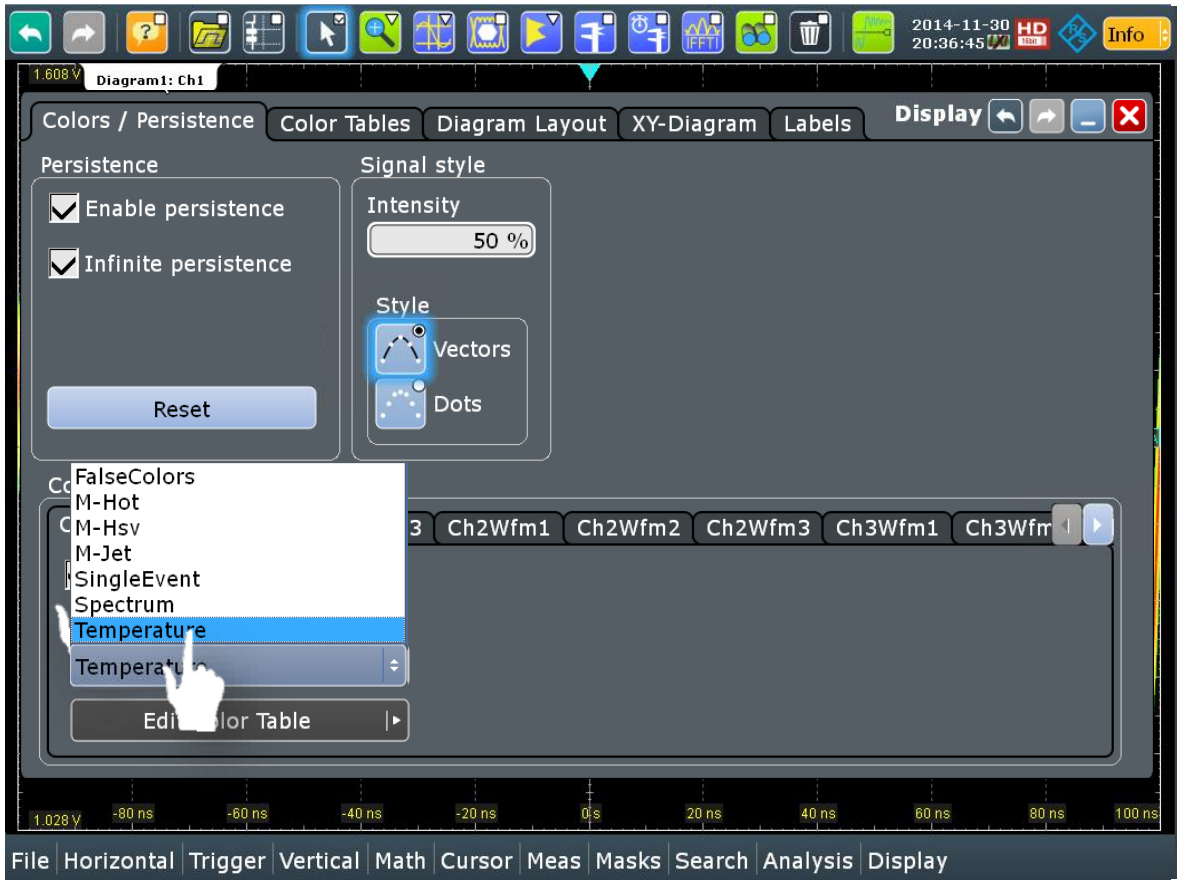
- Persistence is also a default feature on RTO



Persistence

Color Grade

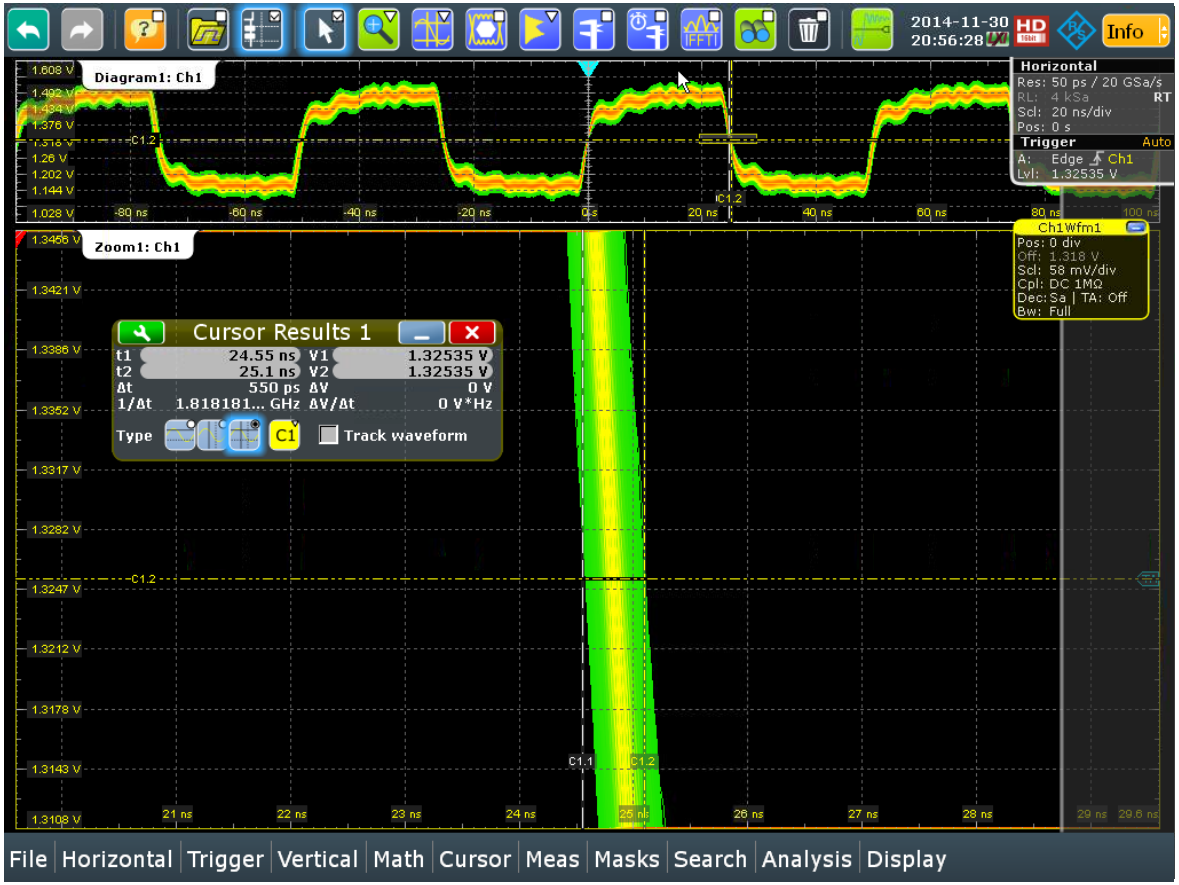
- For easier observation, user can change color grading



Persistence

Cursor

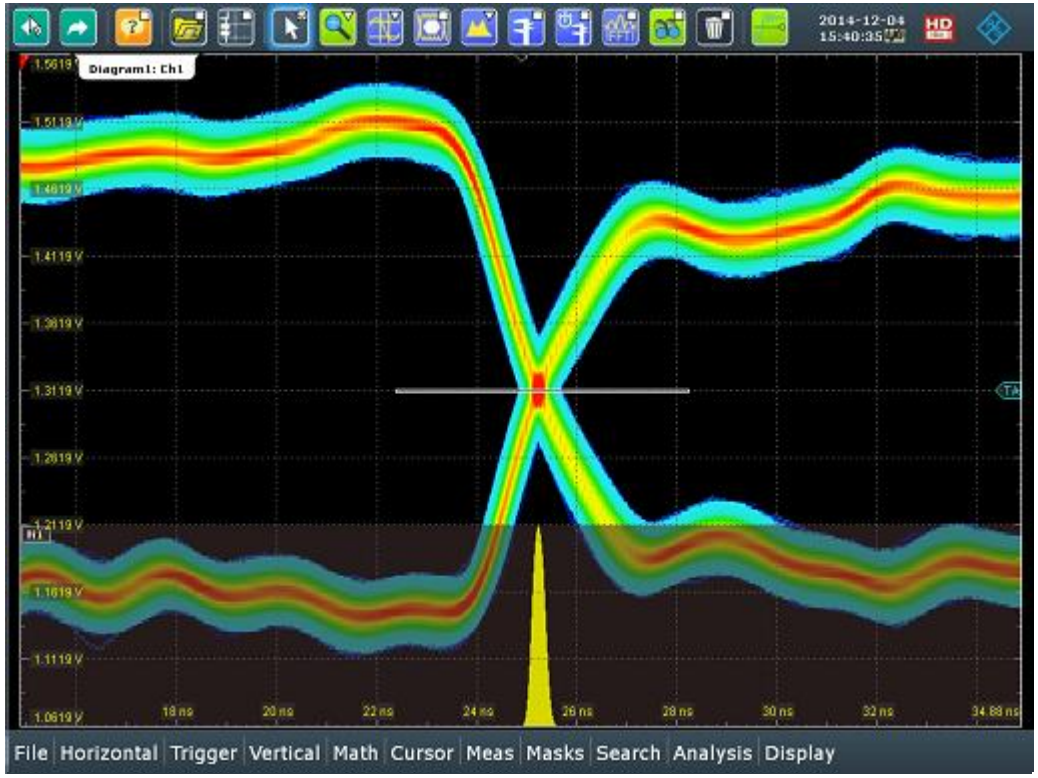
- Cursor can be placed on persistence waveforms signal edge



Histogram

Waveform

- Waveform histogram can show cumulative distribution of a signal jitter based on level crossing

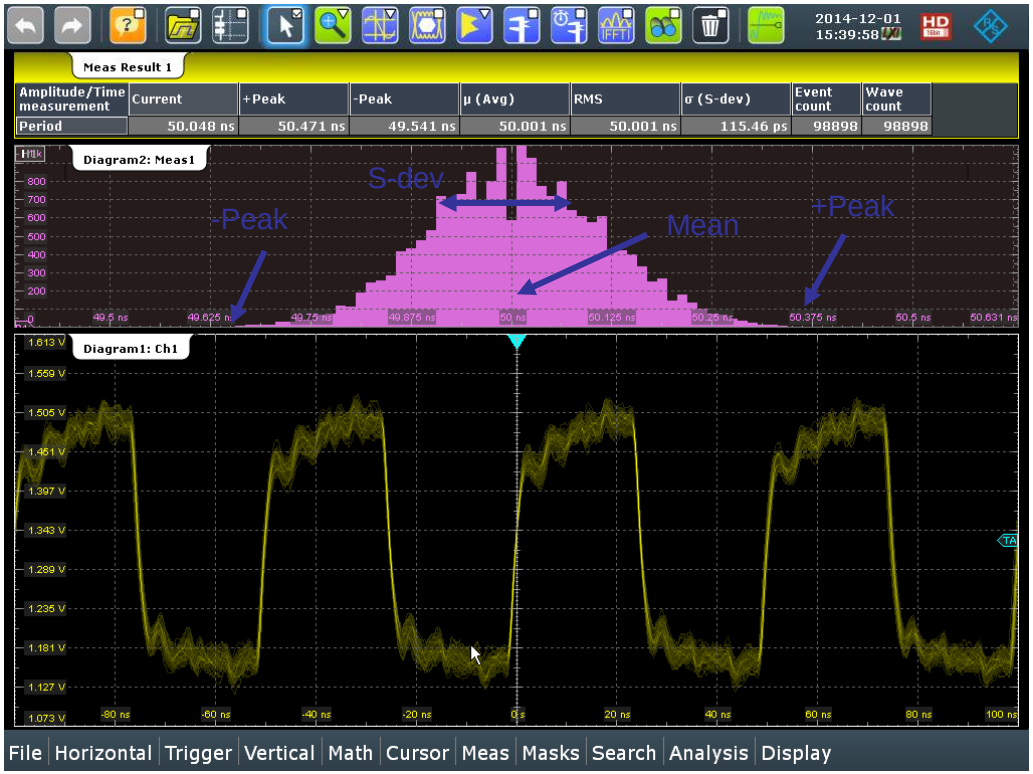


Histogram needs to be 1 pixel size around trigger value to see jitter distribution at the level

Histogram

Measurement

- Histogram can also be generated based on cumulative results of a measurements to allow user to see the statistic trend



Peaks for unbounded jitter depends on measurement interval. Waveform count is important to limit the effect of such peak to peak jitter spread

Track

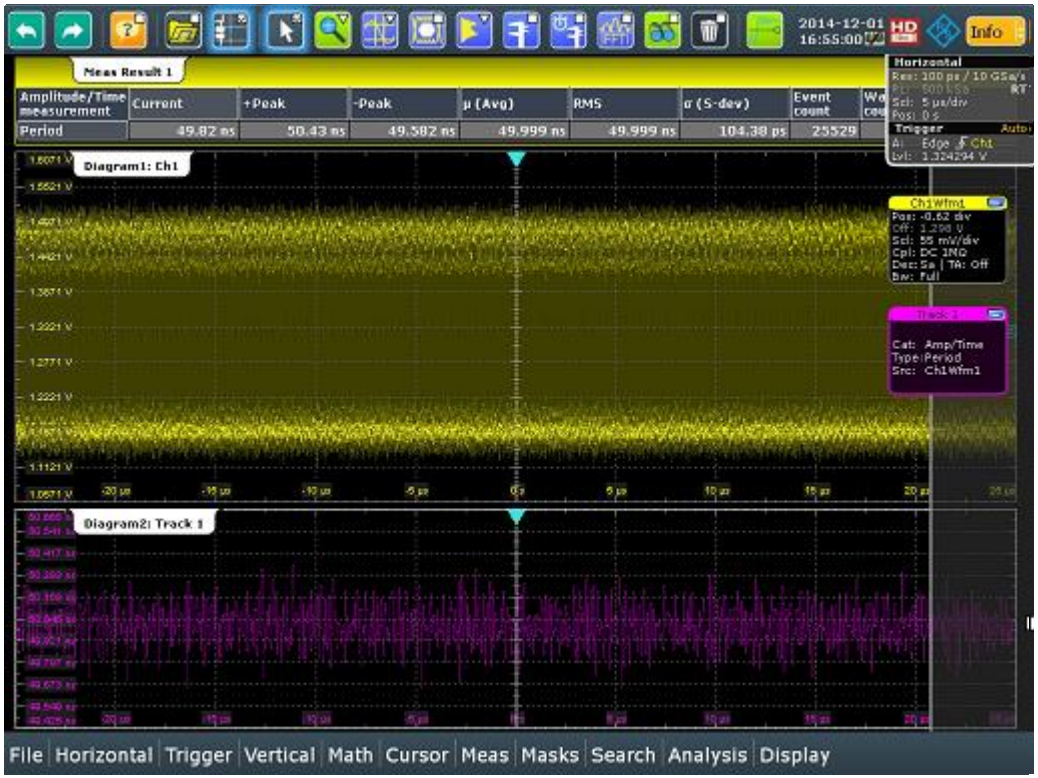
Setting Up

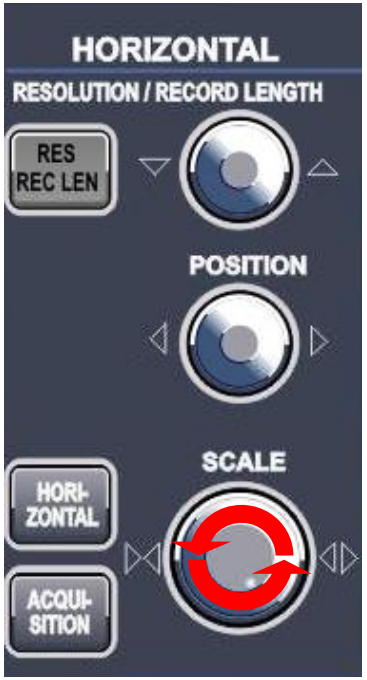
- K12 allows user to visualize multiple measured result in an acquisition as trace

Track

Configuring

- Track trace can be move & rescale based on user need

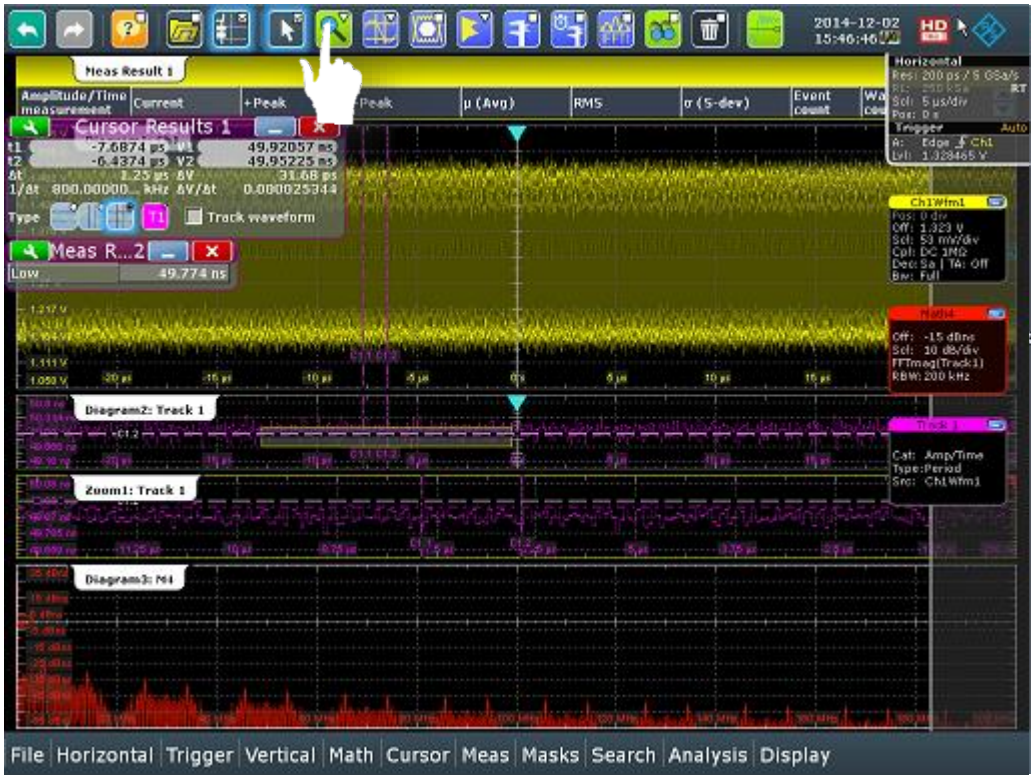




Track

Measurements

- Track can zoomed, measured via cursor or automatic measurements and even FFT



Zoom

Cursor

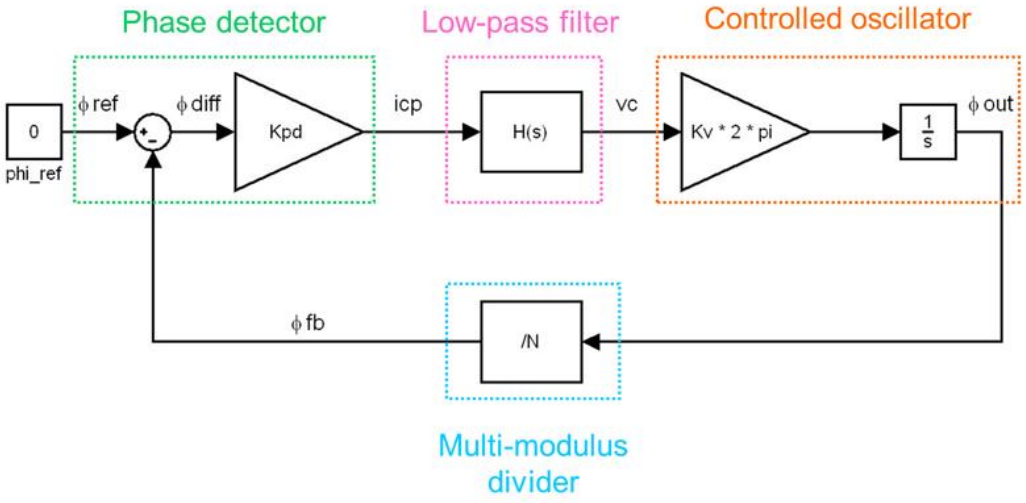
Measurement

FFT

Clock Data Recovery

CDR Concept

- To recover clock edges from data, a simple mechanism called the phase locked loop (PLL) is used
- PLL compares feedback signal with a reference using phase comparator and signals voltage controlled oscillator (VCO) to match up the phase. In the feedback loop, a divider is used so that reference does not have to be the exact frequency of output
- A filter is introduce between phase detector and VCO to control how PLL responds to changes, ie Lock range, lock time, settling time, damping, etc.



Clock Data Recovery

PLL Order & Damping

- 1st Order PLL is the most fundamental architecture and useful as a reference to understand complex higher order PLL. Some characteristics:
  - Medium jitter filtering towards high frequency
  - Medium jitter tolerance
  - Limited control

- 2nd Order PLL has added complexities to enabled it to:
  - Filter out high frequency component of incoming jitter
  - Jitter tolerance of 2nd order always is lower than 1UI
  - Damping ratio controls transient response of 2nd order PLL, it defines how fast PLL settle down and bandwidth of the PLL
  - Overdamping could cause ringing & overshoot while underdamping could cause slower response and more phase error

Clock Data Recovery

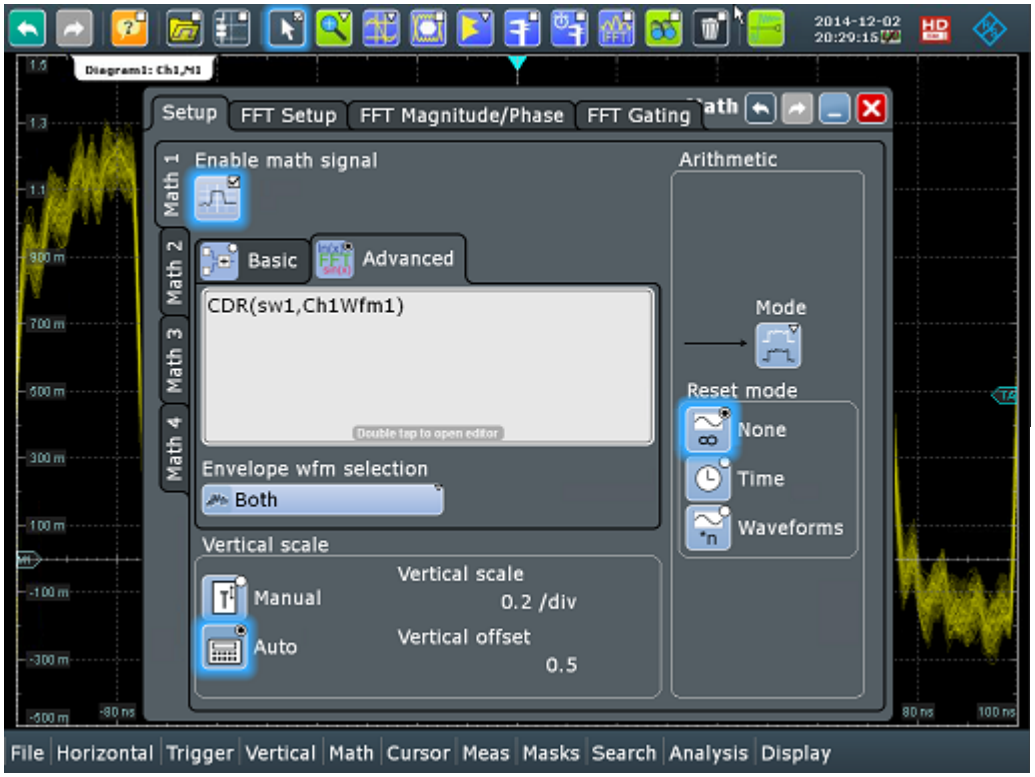
Software CDR

- SW CDR acquires enough edges from the acquisition to recreate a clock through calculation. It emulates receiver PLL via software

Clock Data Recovery

Displaying Software CDR

- Recovered Clock can be visualized using Math Trace
- Example uses a 40Mbps Data of alternating 1 and 0



Set Nominal Bit Rate and Data Edge

Use Estimate to get accurate bit rate

Go to Math and set to Advance Formula

Clear the previous Formula

Set the new formula to CDR with correct SW PLL source

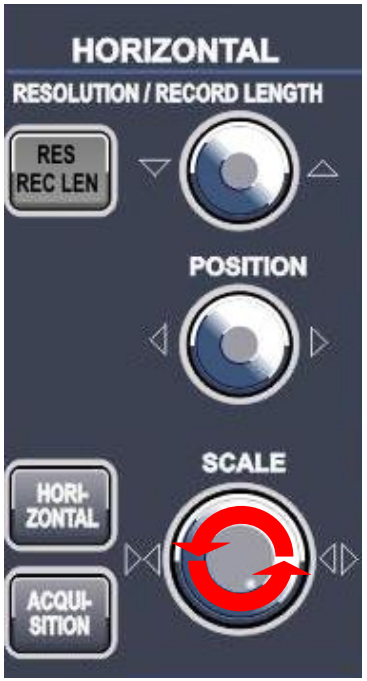
Fill the Formula with right Source and complete it

Enable the Math Function

Clock Data Recovery

Displaying Software CDR (2)

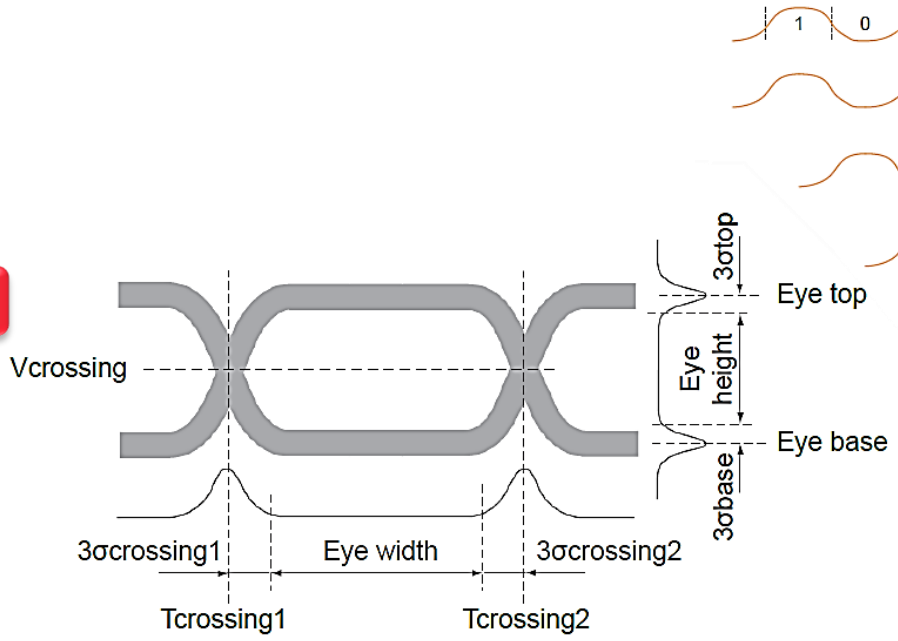
- SW CDR need enough edges to be able to synchronize the clock
- Zooming in we can observe the recovered clock edge

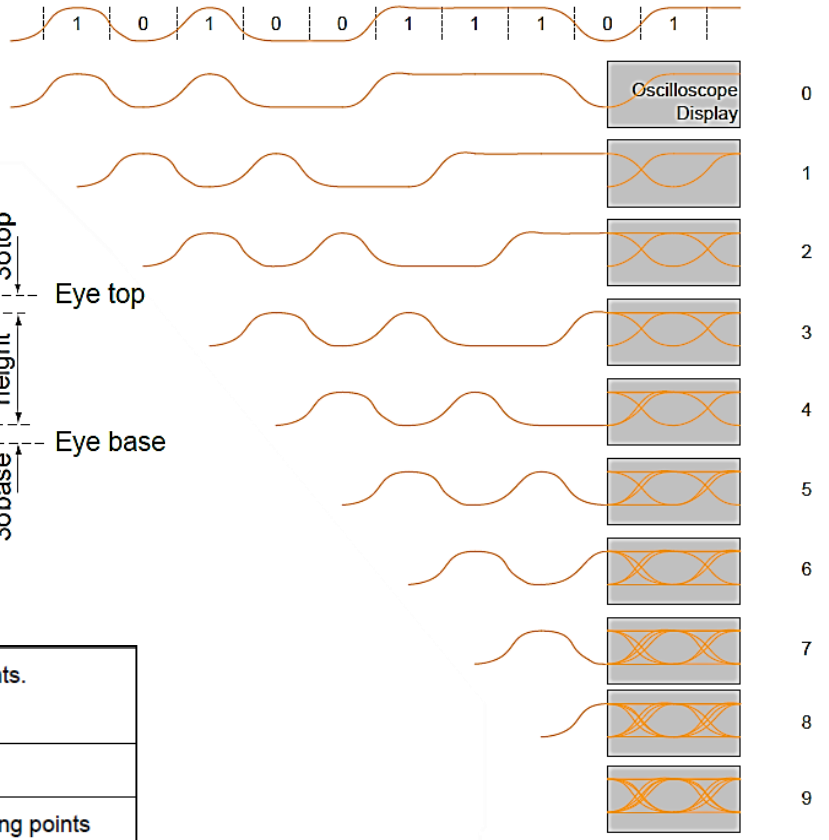


Eye Diagram

Overview

- Overlaying multiple UI is the quick and easy way to observe signal integrity issue, rise/fall time mismatch and even jitter



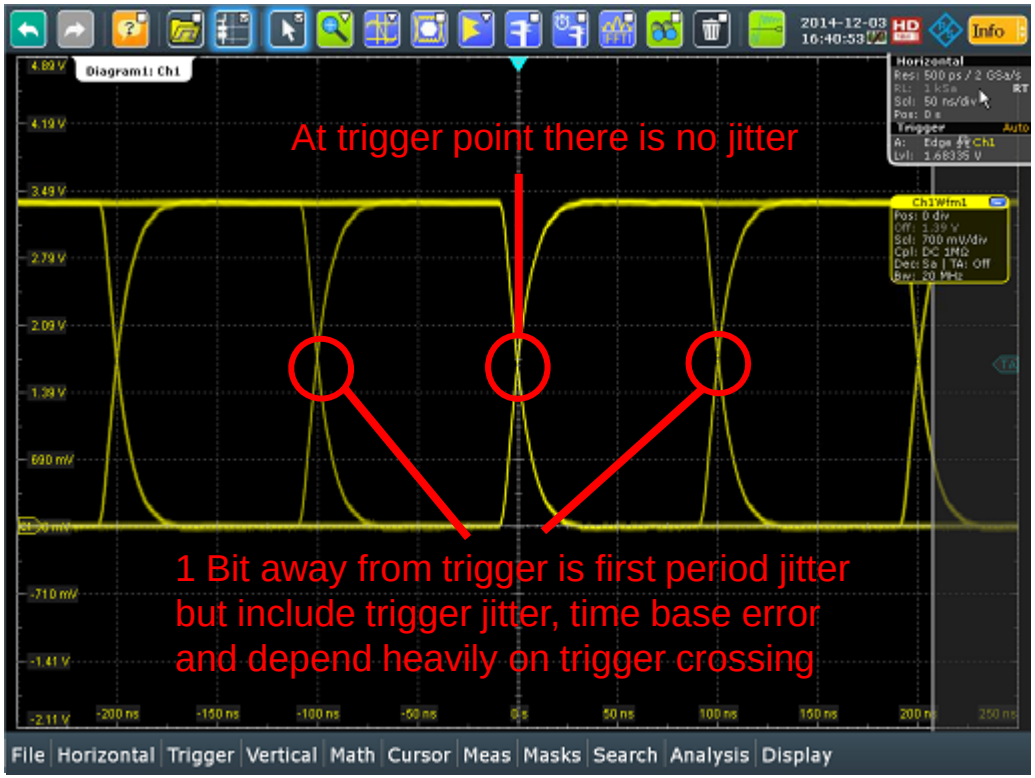


Jitter (peak to peak)	Average of the jitter for both crossing points. Jitter = (σcrossing1 + σcrossing2) / 2
Jitter (6*σ)	Jitter (6*σ) = Jitter * 6
Jitter (RMS)	Quadratic mean of the jitter at both crossing points

Eye Diagram

Configuring: Edge Trigger with Either Slope Method

- Simplest method of creating an Eye using edge trigger & persistence but limited in jitter measurement



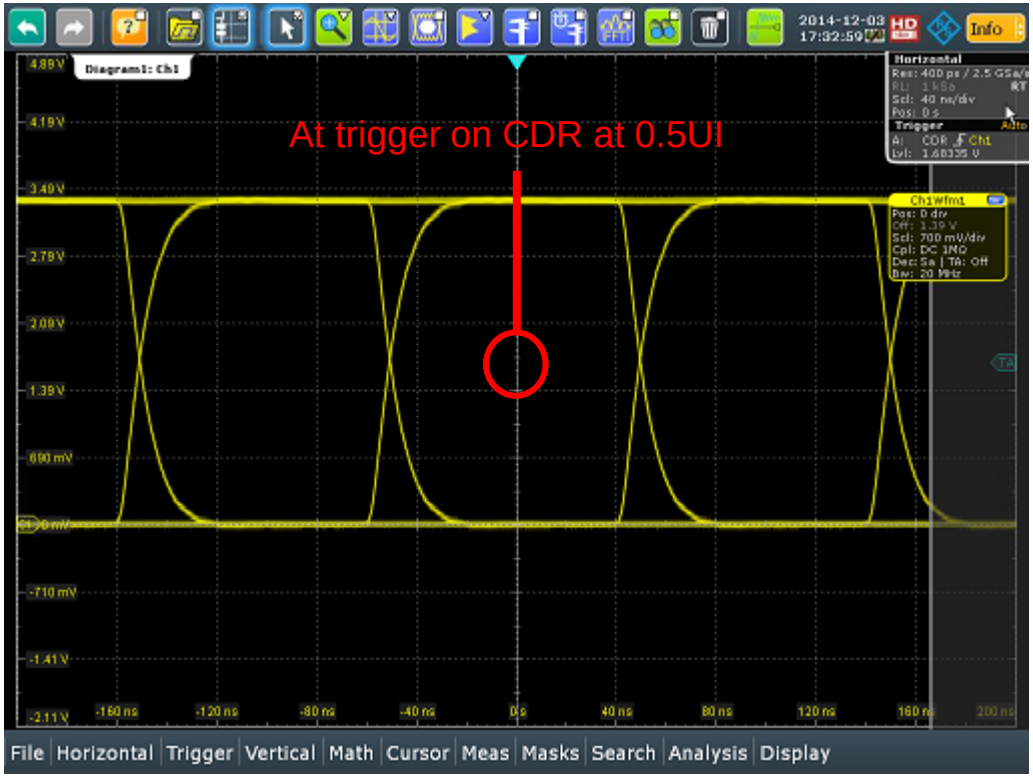
Not the best Eye Method because it is hard to determine if all transitions are overlap and jitter increase (time base error) as we move further away from trigger point.

Still this is quick and easy to allow observable signal issues and basic jitter profile.

Eye Diagram

Configuring: CDR Method

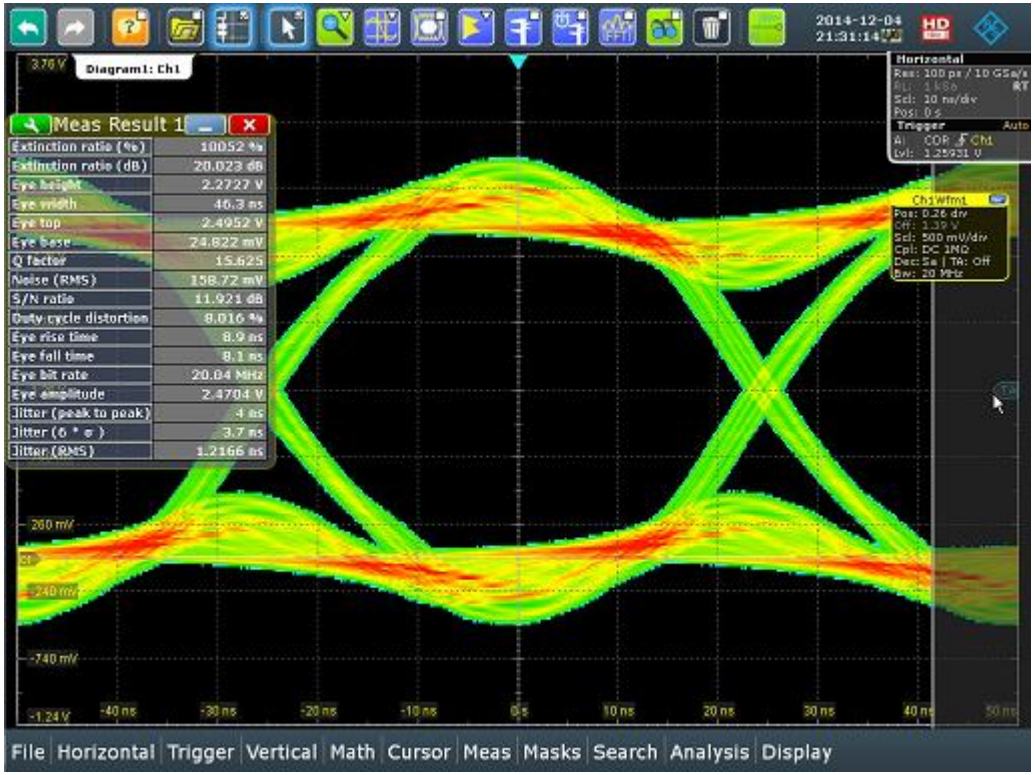
- Triggering on recovered clock emulate receiver characteristics and is best for eye & jitter measurement



Impact of time base accuracy is minimized. Every UI will experience similar jitter and higher confidence of transitions collection

Eye Diagram

- RTO Equipped with automated Eye measurements

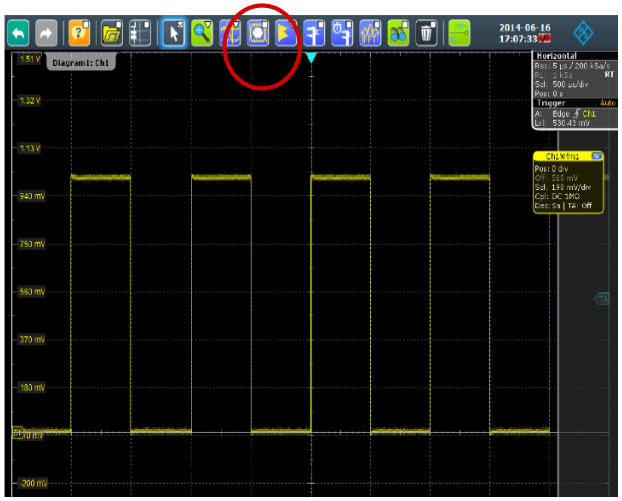


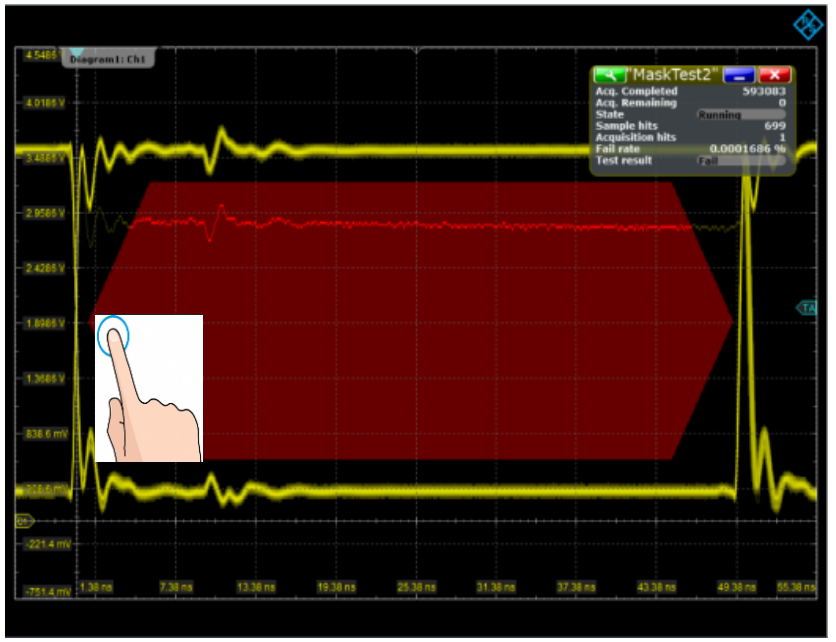
Eye related measurement can be done

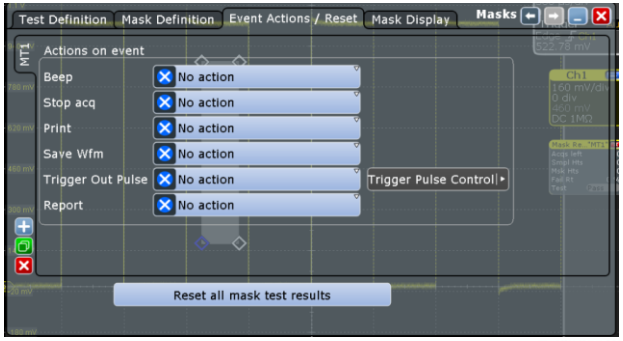
Measurements in “Real Time”

R&S®RTx Features: Easy MASK

- **Mask: settings in only seconds**
  - Easy and quick configuration
  - High acquisition rate
  - Reliable results
  - Standard in the R&S®RTx
  - Seup condition when mask hit







R&S®RTx Features: History Mode

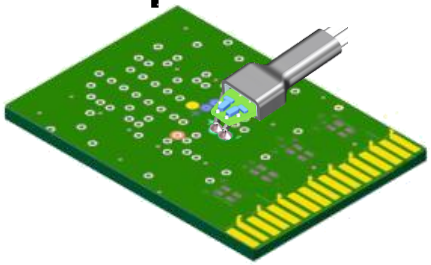
- always available
- Up to 250.000 acquisitions are stored
- Trigger event includes time stamp
- All waveforms can be replayed and analyzed

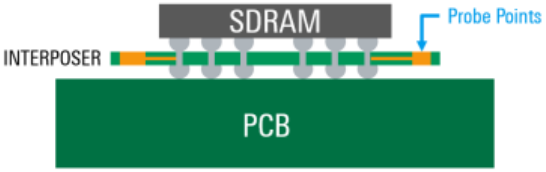
Analyze previous acquisitions - always available in history buffer

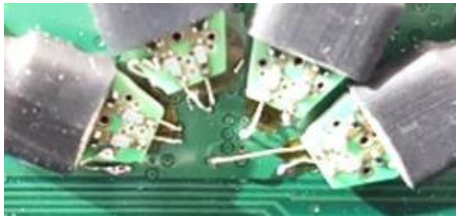
DDR4 Signal Integrity & Compliance Testing

Interposers

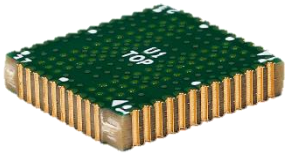
- **DDR JEDEC compliance focus on SDRAM chip and specifies measurement at package ball**
- **On single-sided DIMM or PCB, it is still possible to probe behind the package**
- **For design without access to back of PCB, interposer is the best option**

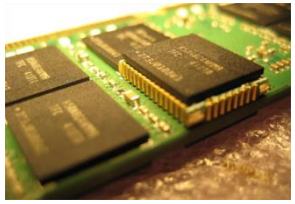






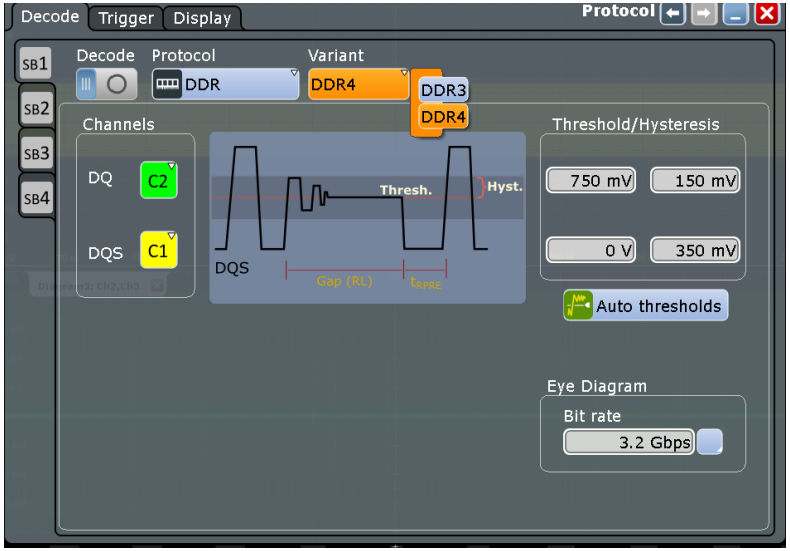
Edge-type from Nexus





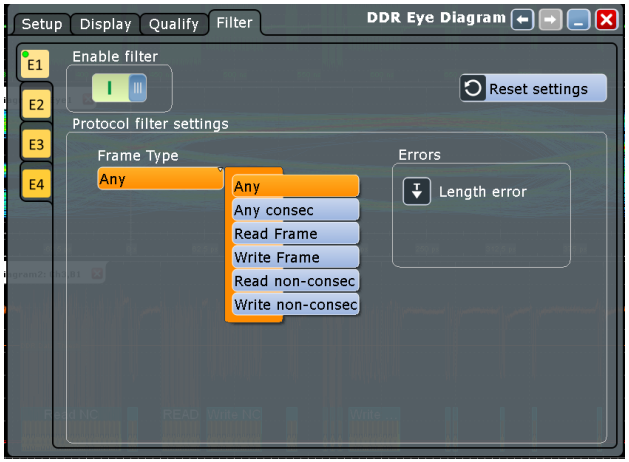
READ / WRITE Separation

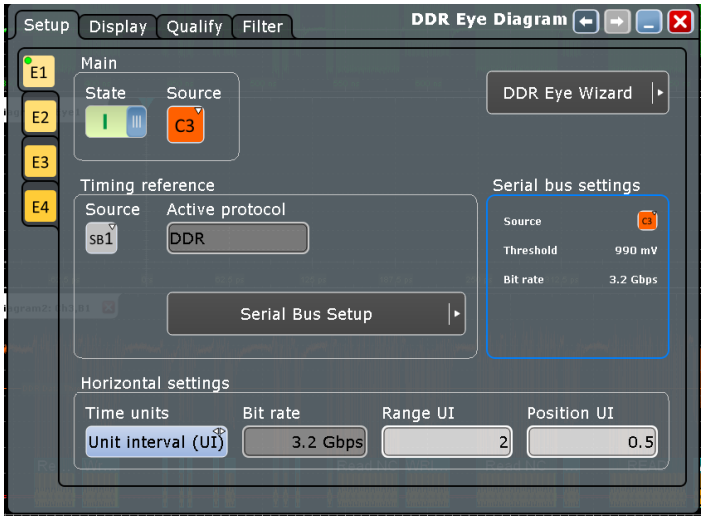
- R&S offers most stable R/W separation based on only DQ and DQS signal
- Additional information is with ChipSelect signal for in depth debugging available
- Reliable R/W separation is key for data eye analysis



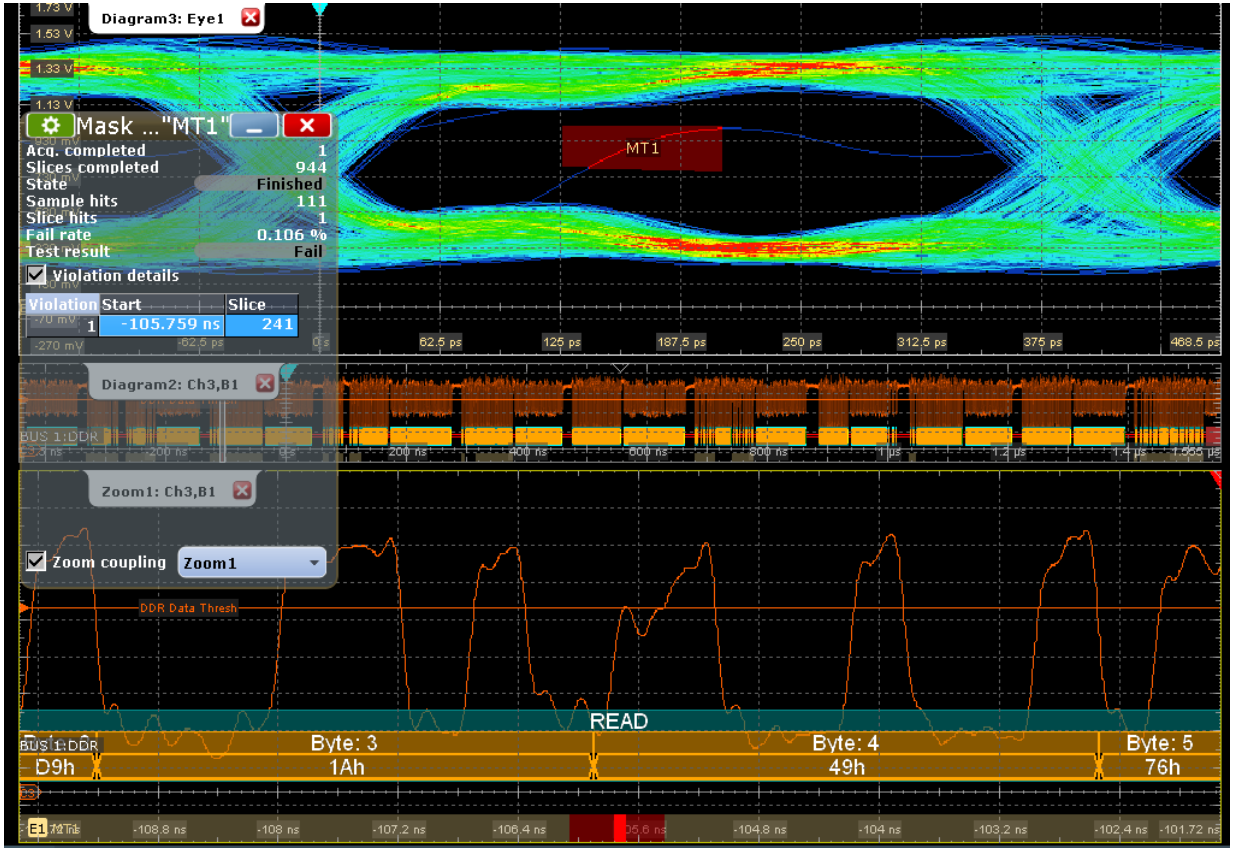
DDR4 Signal Integrity &Compliance Testing
DDR data eye

- **Data Eye display is the most important tool for Signal Integrity analysis!**
- **R&S implementation is very powerful and provides most insides**
  - Use w/r decoding as timing reference
  - Read / Write filter
  - Mask test
  - Zoom coupling on mask violations





DDR data eye



Zoom coupling of mask violations

Thank You