REDESIGN WITH SIC – AN EMI COMPLIANCE RAPID PROTOTYPING APPROACH

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ROHDE&SCHWARZ
Make ideas real

OBJECTIVES

- Insight of Today‘s Power Electronic designs challenges
- What is EMC all about
- EMI with in the relation to product development cycle
- Performance levels and instrumentation
- EMI Debugging with an oscilloscope and discuss limitations to consider
- Deeper look on two specific fields of EMI debugging with an oscilloscope
- Design tips and simplicity of redesign with SiC
- Tool Demo to extend oscilloscope capability
- Results of the re-design
- Conclusion

THE CHALLENGES IN TODAY'S POWER ELECTRONIC DESIGN

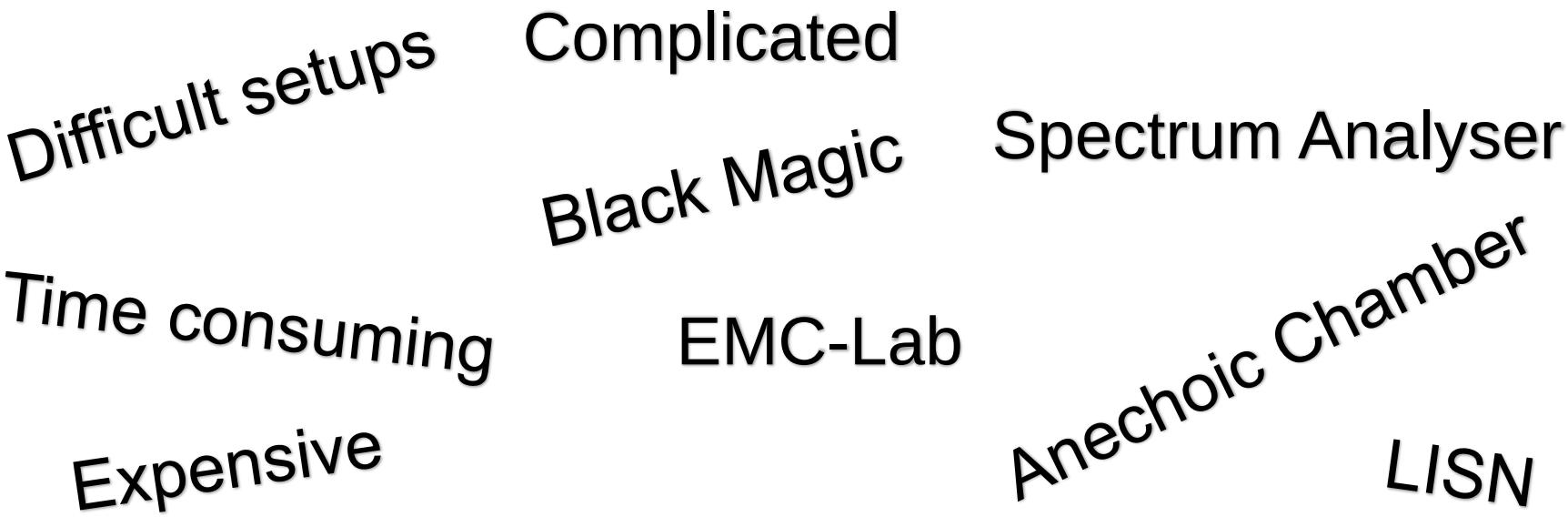
Trend for Power Electronic Design

- ► Usage of Faster Switching Devices like SiC to obtain higher efficiency
- ► SiC enables designing a smaller form factor (Higher power density)
- ► No increasing cost
- ► Reliability of power designs

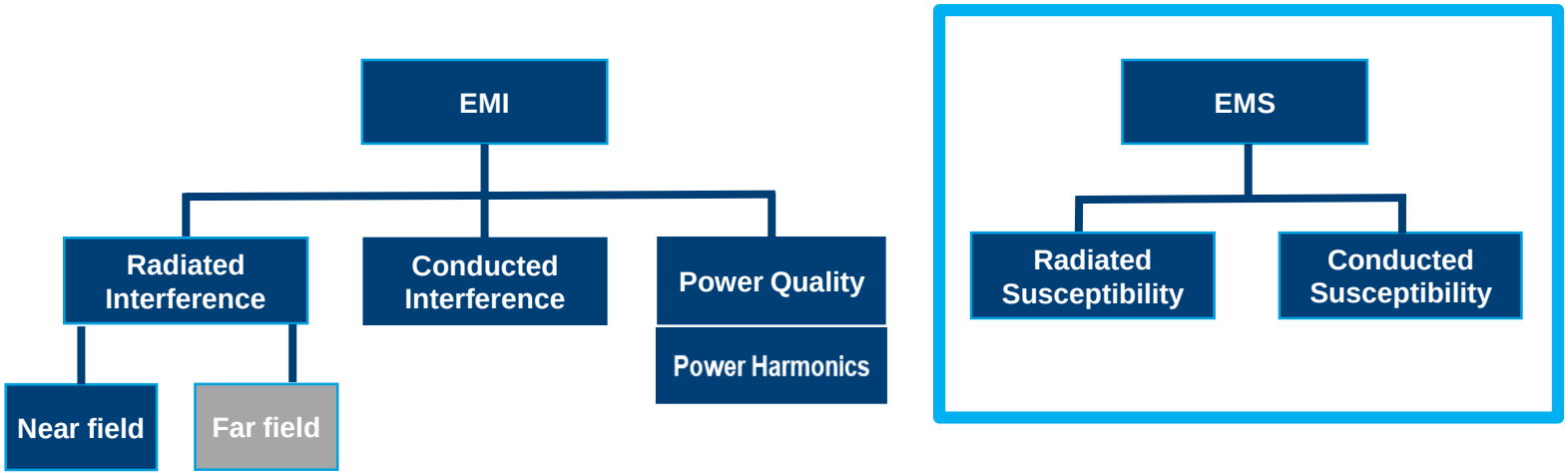
More EMI issues

- ► Higher speed of power semiconductor may introduces more EMI issues
- ► Bad PCB Layout (stacking) causing worse EMI

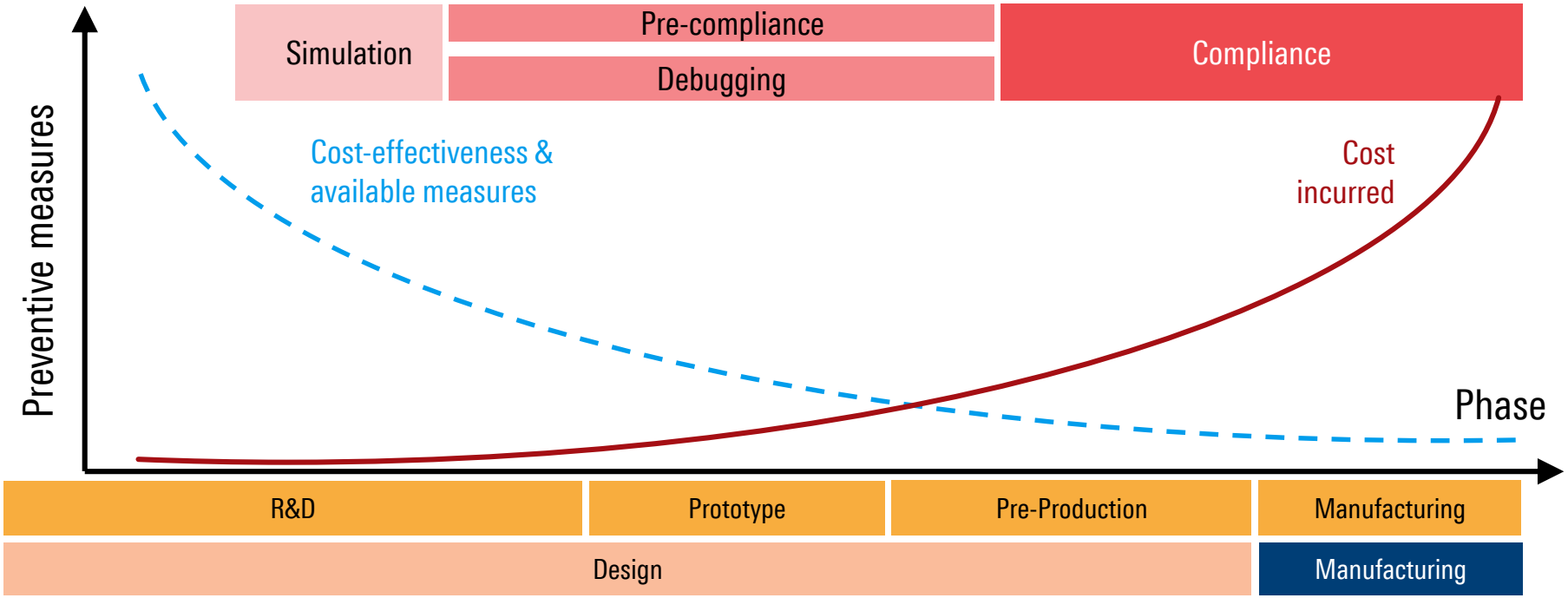
ELECTROMAGNETIC COMPATIBILITY (EMC)
WHAT COMES TO YOUR MIND WHEN THINKING ABOUT EMC?



WHAT IS EMC?


EMI
Radiated Interference
Conducted Interference
Power Quality
Power Harmonics
Near field
Far field
EMS
Radiated Susceptibility
Conducted Susceptibility

EMI MEASUREMENTS IN DIFFERENT DESIGN PHASES



PREVENTION IS BETTER THAN CURE

Similar to medical check-up for preventive health care, we diagnose early on circuit to avoid future issues

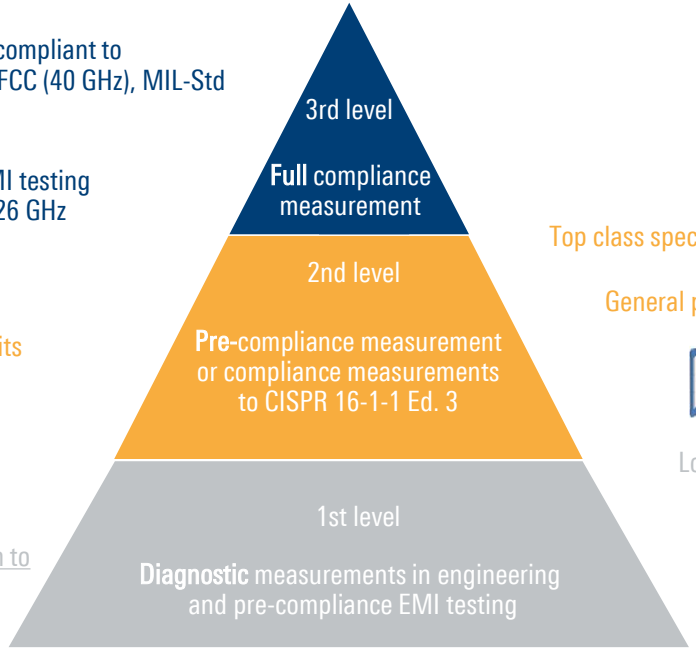
PERFORMANCE LEVELS OF INSTRUMENTATION
SELECTING THE RIGHT TOOL

ESW 
EMI receivers compliant to
CISPR 16-1-1, FCC (40 GHz), MIL-Std

ESR 
Compliance EMI testing
CISPR 16-1-1, 26 GHz

ESRP 
EMI testing
referring to limits

ESL 
Diagnostic
measurements
without relation to
limits



Receivers

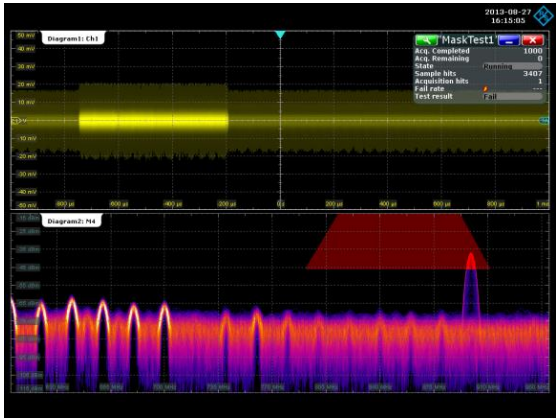
Top class spectrum analyzers 
FSW

General purpose spectrum analyzers
FSV
FSVR

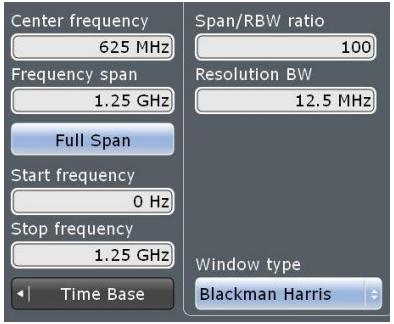

Low cost spectrum analyzers, oscilloscopes


Scopes & Spectrum Analyzer

EMI DEBUGGING WITH OSCILLOSCOPES



- Available on every R&D engineers desk
  - Easy debugging of EMI problems in R&D
  - Improvements can easily be tested
- Oscilloscopes show both time and frequency domain
  - Correlation between unwanted spectral emission and time-domain signal parameters easily possible
  - Time-domain trigger has advantages for capturing intermittent signals
- Today's oscilloscopes provide excellent sensitivity and usability
  - 1 mV/Div corresponds to DANL ~0dBuV
  - Direct input of frequencies and resolution bandwidth



EMI DEBUGGING WITH OSCILLOSCOPES

Near-Field Probes

Debugging in the near field after failed test in the far field (compliance test)

Artificial Mains Network

Debugging on power lines

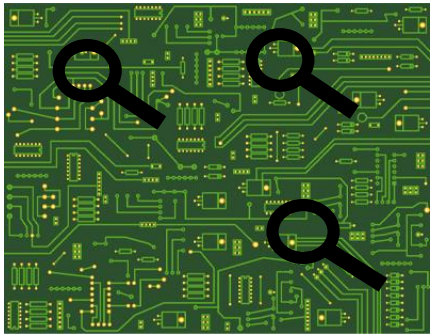
IN R&D

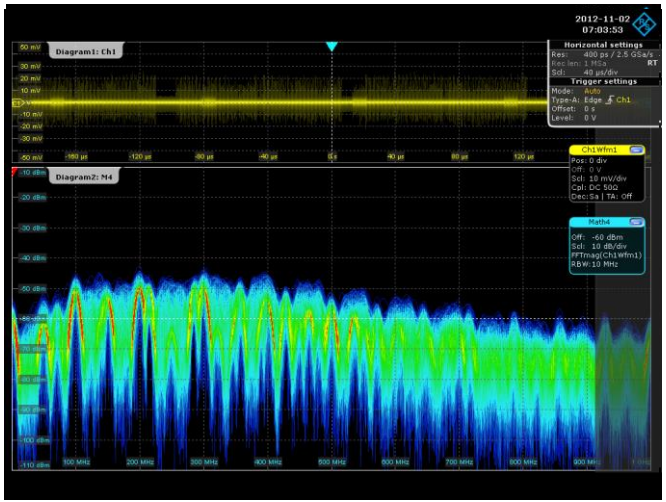
LOCATING EMI WITH A NEAR FIELD PROBE
WIDE SPAN SCANNING

Wide Span scan – fundamental of interfering signals are usually lower than 1 GHz

Identify abnormal spike or behaviour and its location while moving the probe around

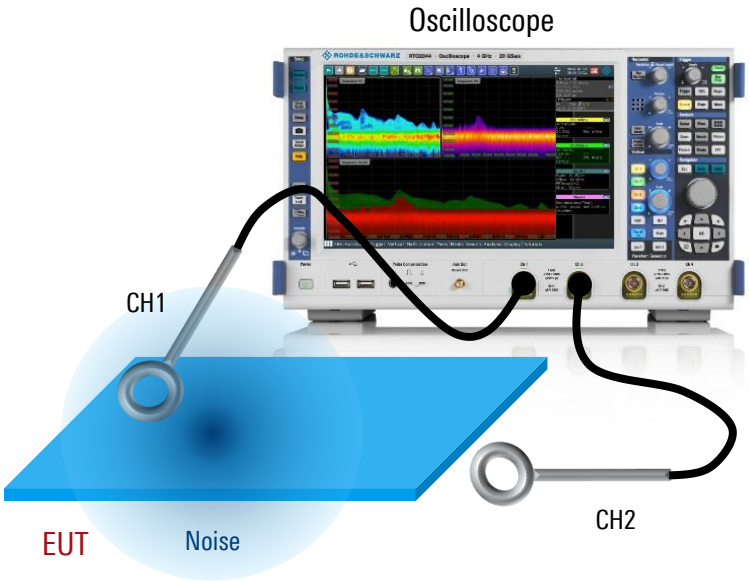
Narrow down to smaller span and RBW, change to smaller probe for better analysis

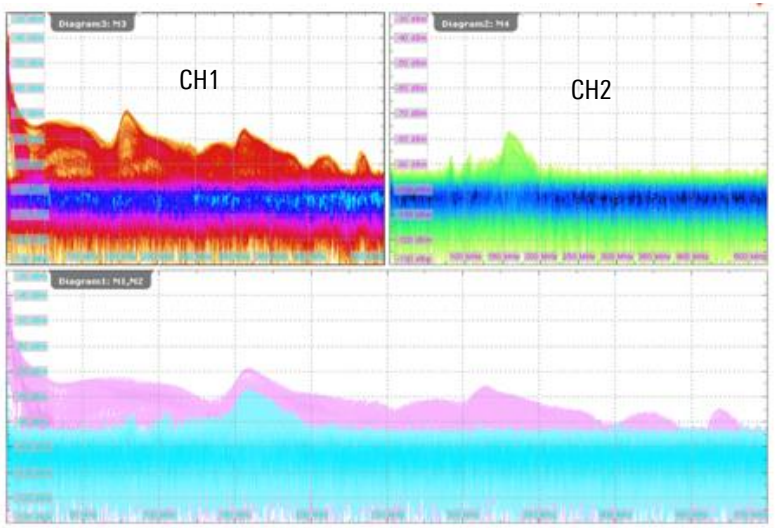




LOCATING EMI
REFERENCE POINT

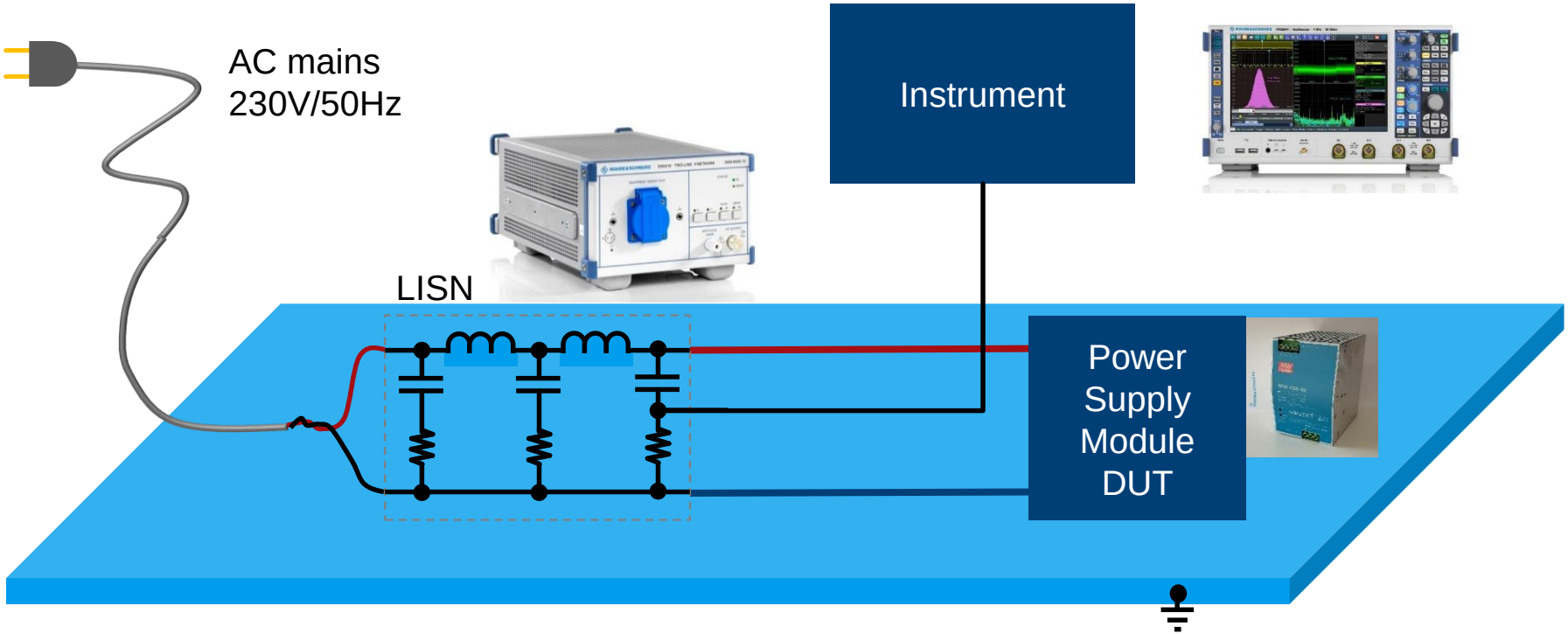
- Using one channel on scope as a static reference point to help locating noise source
- Closer to emission, probe will detect stronger signal presence





Multiple Channel FFT will be needed

EMI CONDUCTED EMISSIONS SETUP



DUT AND STRATEGY

125x86x129 mm

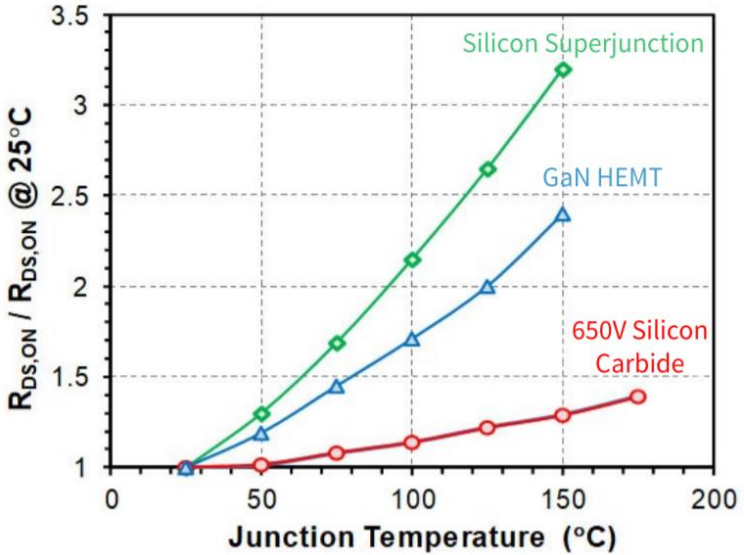
Courtesy: Mean Well

- Single phase industrial class product – SMPS
  - SMPS is the source emissions
- Replace SiC MOSFET with Si-MOSFET
  - Maintain the routing of layout and constraints of design/selection of other components

650V SIC MOSFET FEATURES

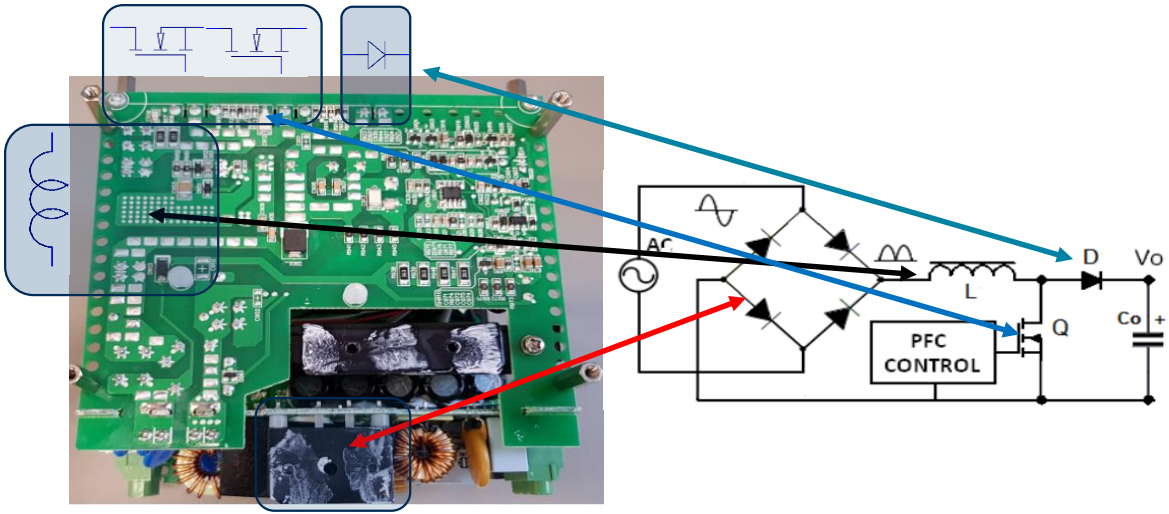
► Easy to use, now at 650V class, suitable for the wide power spectrum and applications.

Part Number	V_{DS}	$I_{D\ MAX\ (25°C)}$	$R_{DS(on)\ (25°C)}$
C3M0015065 D/K	650 V	120 A	15 mΩ
C3M0025065 D/K	**650 V**	**69 A**	**25 mΩ**
C3M0045065 D/K	**650 V**	**50 A**	**45 mΩ**
C3M0060065 D/J/K	650 V	36 A	60 mΩ
C3M0120065 D/J/K	**650 V**	**20 A**	**120 mΩ**



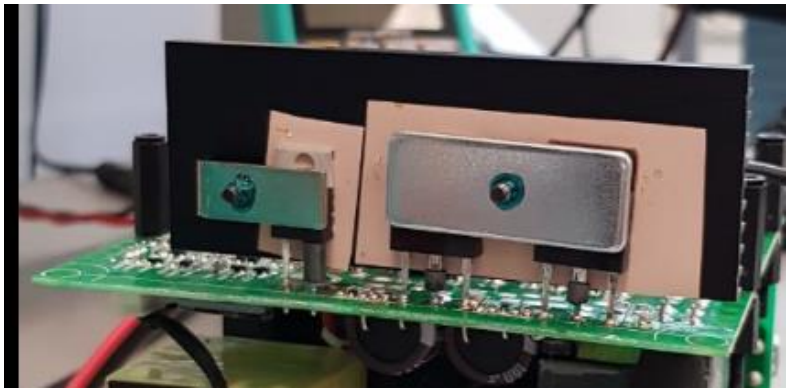
SMPS – CULPRIT; ELECTROMAGNETIC EMISSION

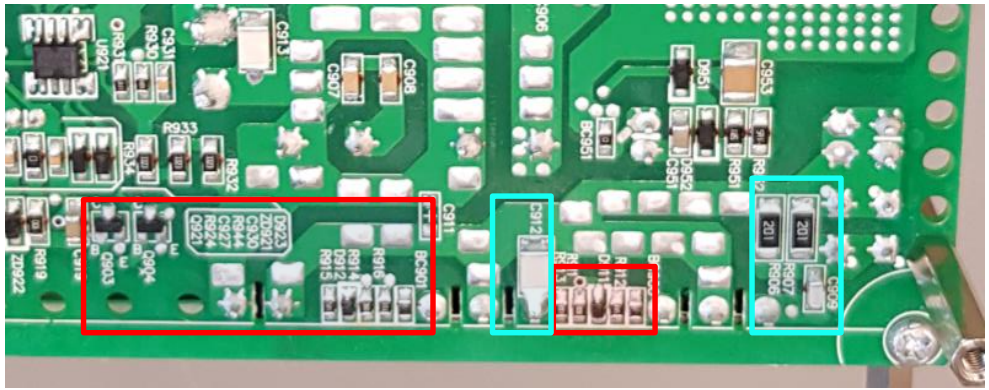
- Universal single phase input voltage, 480W
- Two layers PCB
- Diode rectifier PFC with paralleled Si MOS (85kHz), 1 SiC Diode + HB LLC



SMPS – CULPRIT; ELECTROMAGNETIC EMISSION

- Gate driver: Totem pole BJTs, 0/15V, turn-off diode, ferrite in series with Rg
- C + RC snubber
- Ferrite in PFC MOSFET, SiC boost diode and output capacitors.





Note: not the actual TIM and heatsink

REDESIGN AND TIPS WITH TOOLS

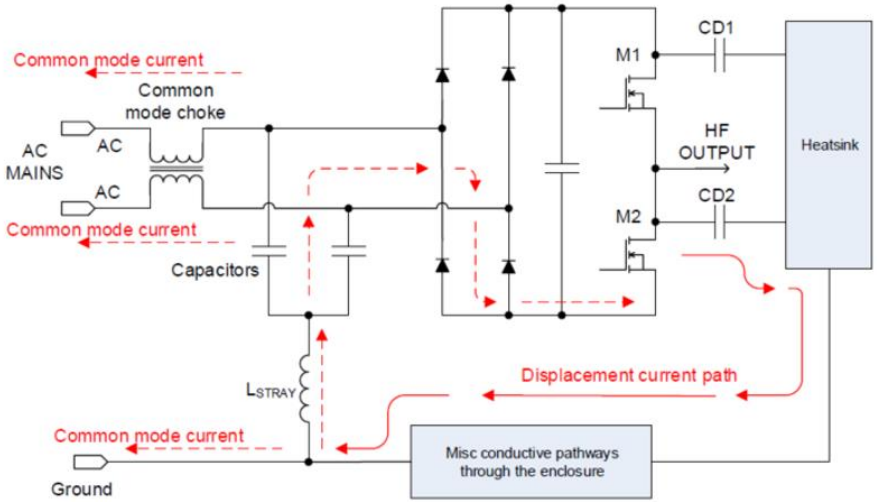
- What to do with Radiated Emissions?
  - Common design rules, SiC is not different than any other fast switching devices!
  - Keep the antenna effect small with layout; especially the power loop.
  - Decoupling, ferrite, snubber, etc.
- Indicative near field measurement with Si DIN rail PSU as reference
  - Multi channel FFT, side by side comparison with the SiC solution

REDESIGN AND TIPS WITH TOOLS

- What to do with Conducted Emissions?
  - LSIN to measure.
- Power-line filter; DM and CM, is often obvious the solution.
- Is there better alternative?

REDESIGN: ORIGIN OF CM NOISE

- Dv/dt cause a displacement current to flow
  - Parasitic capacitive coupling to ground
  - Through transformer interwinding capacitance
  - Through thermal management as shown here



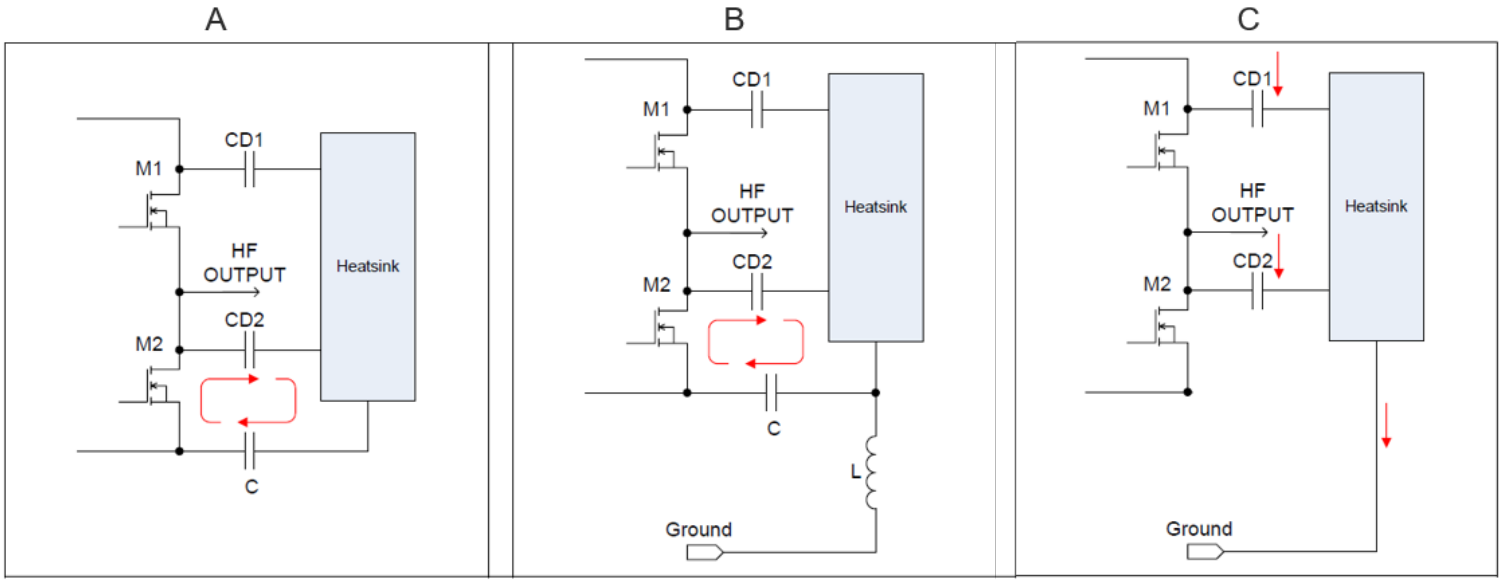
REDESIGN: TYPICAL APPROACH TO SOLVE CM

- Reduce switching speed by increase Rg thus reduce dv/dt,
  - Simple, BUT increases switching losses, ruin one of the key advantages; faster switching.

- More filtering
  - BUT this make the BOM more costly and the volume/weight of product to go up, which ruin another advantages of design with SiC.

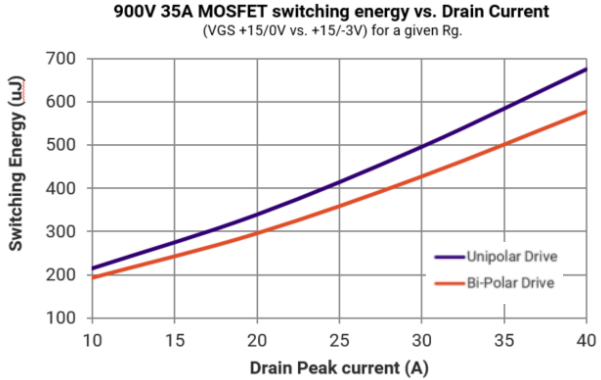
REDESIGN: PROPOSED APPROACH TO REDUCE CM

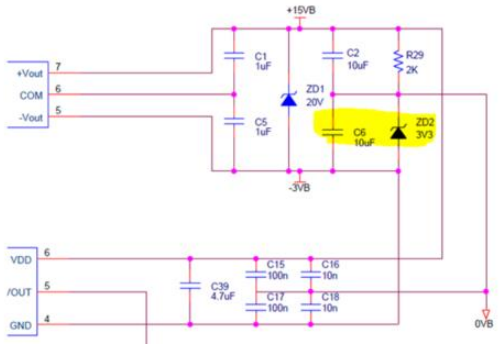
- Solve the problem at its root

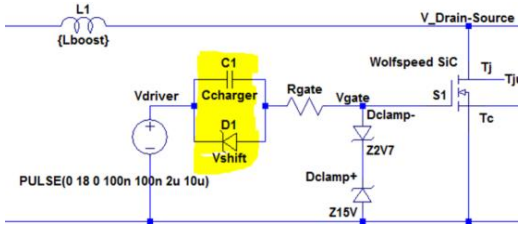


IMPLEMENTATION TIPS WITH SIC

Wolfspeed SiC MOSFETs are Enhancement-mode = Normally Off and can safely turned off with 0V, however with negative turn-off voltage the switching energy can be reduced and thus more efficient switching, furthermore it also increases the margin against parasitic turn-on and make the switching stage more robust in noisy environment.

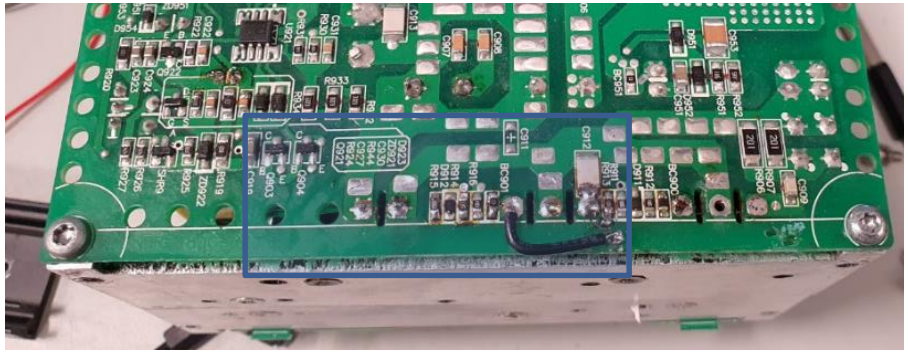






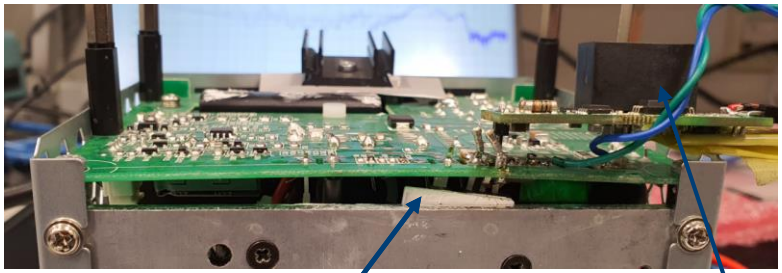
IMPLEMENTATION TIPS AND OVERVIEW

- Use internal gate driver as TO-247-3 and drive the device with 0/15V
  - Gate loop inductance should be reduced as much as possible
  - Can add ~1nF across gate-source if near field measurement show anything from here
  - General good layout design can reduce a lot emission
    - Removed gate ferrite bead because the gate waveform looks ok
    - Removed ferrite bead on the drain, because don’t see the need.



IMPLEMENTATION TIPS OVERVIEW

- Use external gate driver and driver as TO-247-4
  - SGD15SG00D2 can take existing gate PWM signal as input (level might adjust)
    - Will output -3/15V
- SGD15SG00D2 need aux.12V, if not accessible from the design/prototype, use a battery and connect the negative to reference point to include interference.

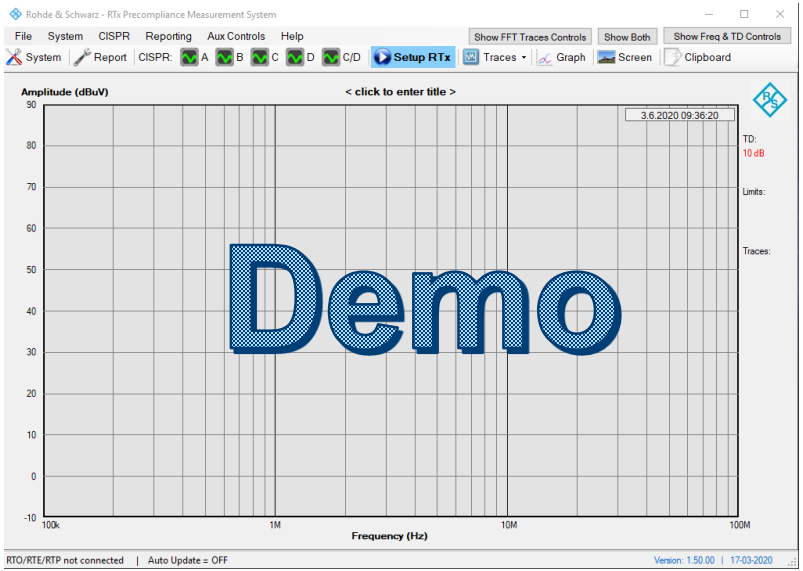


AOS 218 247A Fischer Elektronik:
3mm AL2O3, 25 W/m·K

CGD15SG00D2

PRE-COMPLIANCE MEASUREMENT SYSTEM TOOL

FREE“R&S RTxPre-Compliance Software” adds fast pre-compliance functionality



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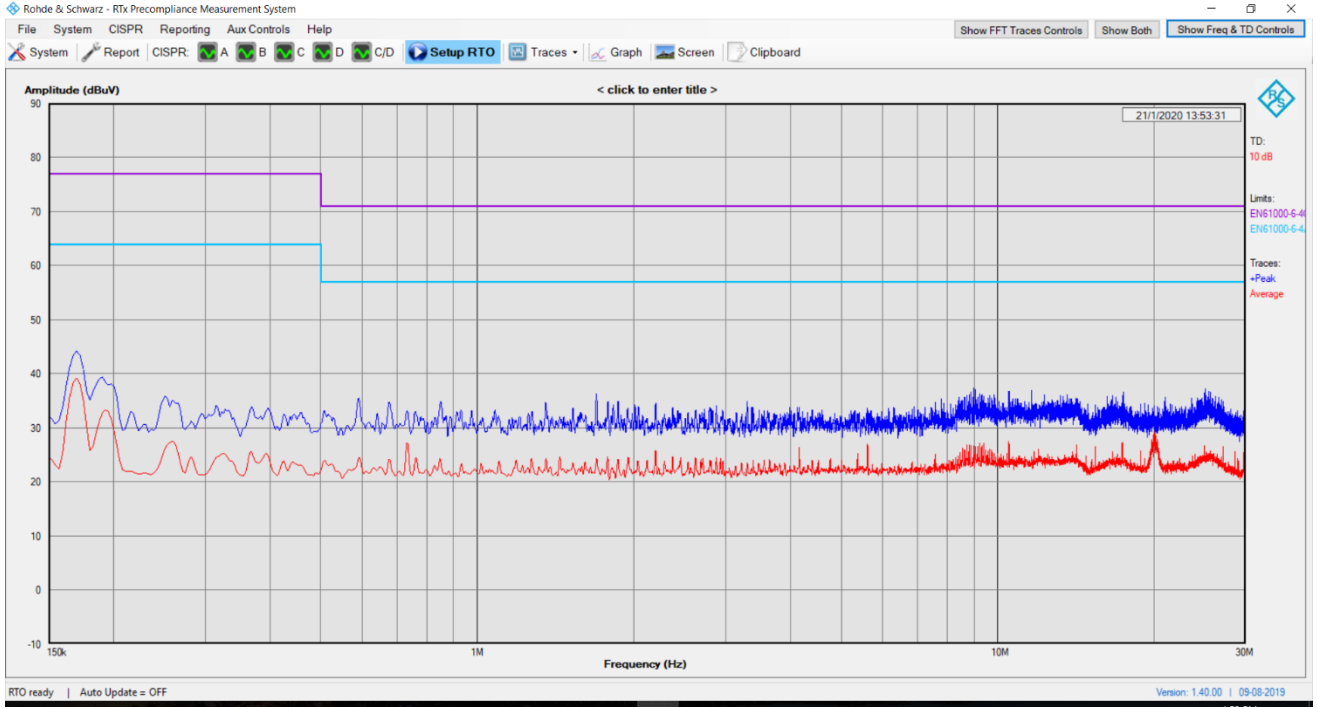
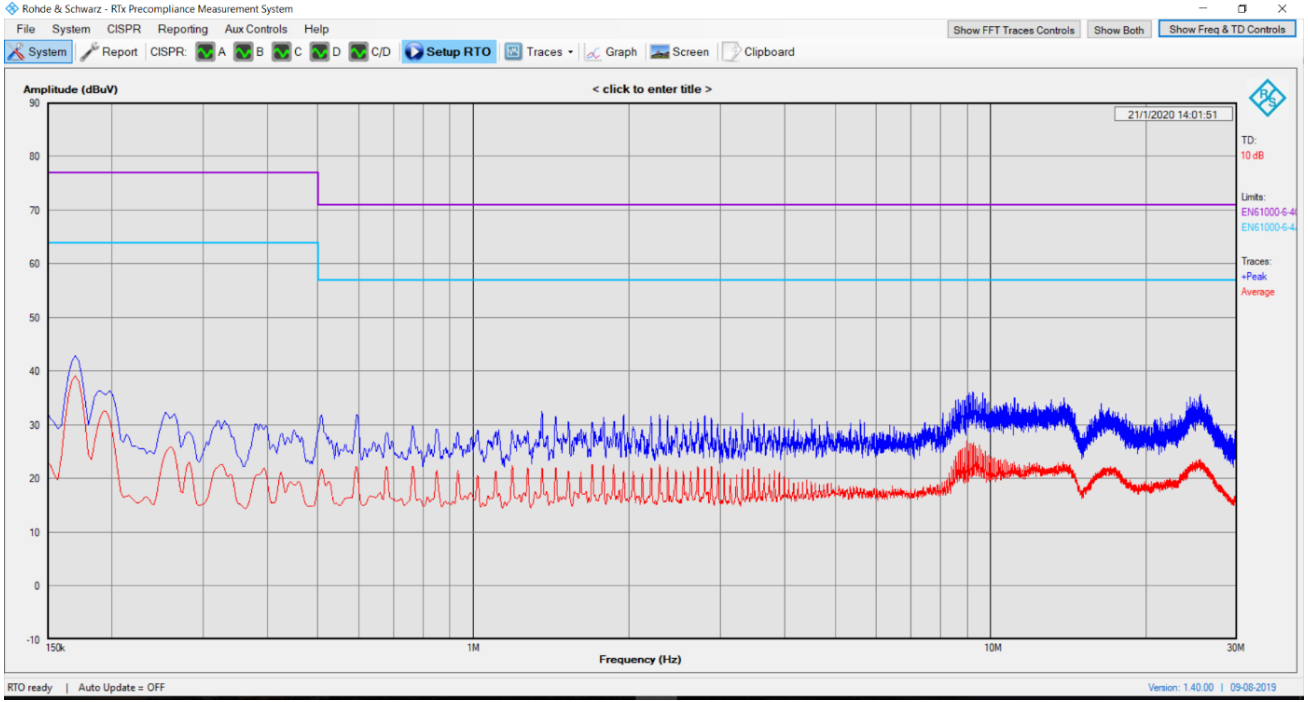
RESULT OF REDESIGN – EXISTING SI MOSFET SOLUTION

- Well below class B limits, no more than 35dBµV at high end of spectrum.



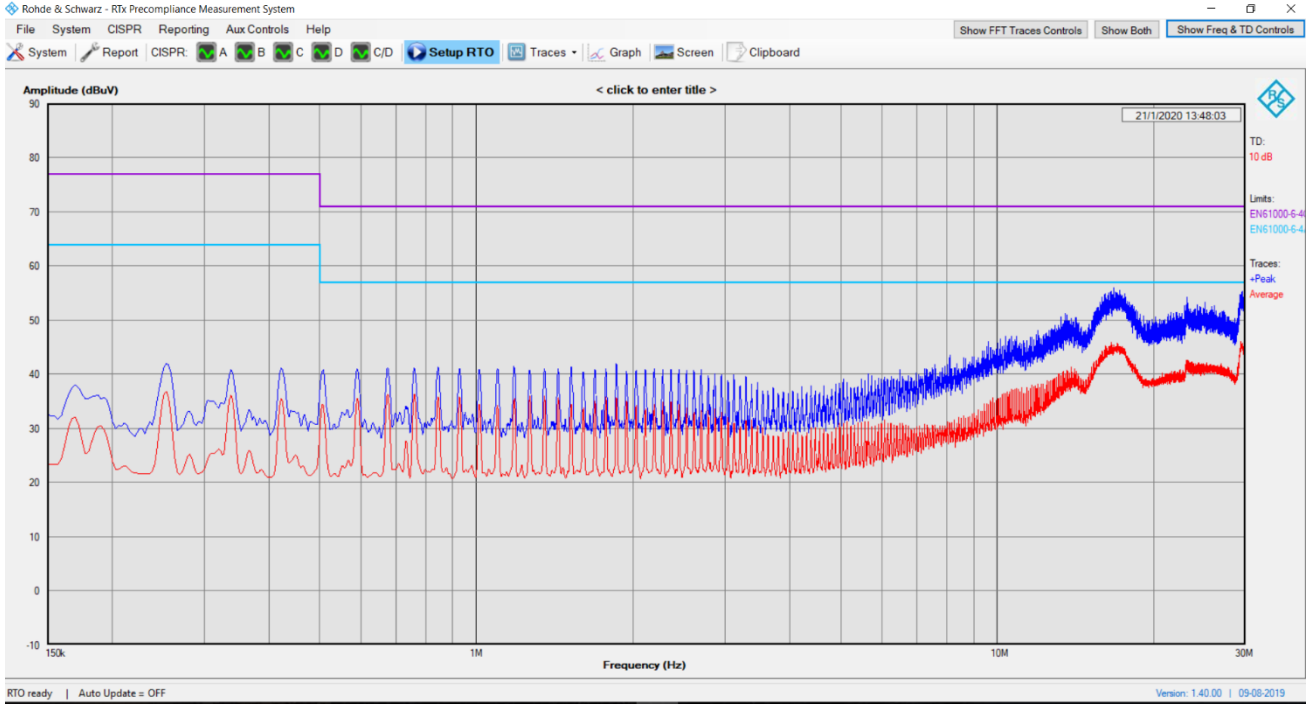
RESULT OF REDESIGN – SIC MOSFET AS TO-247-3

- Well below the limits, Pre-compliance software indicate similar level as Si solution.



RESULT OF REDESIGN – SIC MOSFET AS TO-247-4

- Still below the limits with more than 10dBuV margin, no further fine tuning.

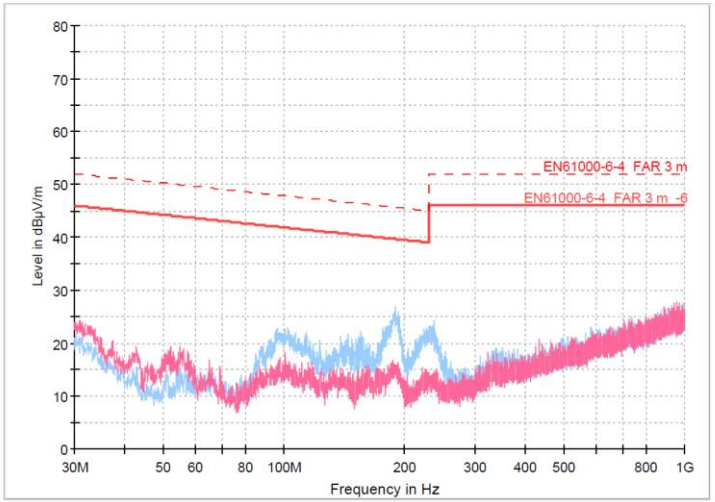


RESULT FROM COMPLIANCE TEST – RADIATED EMISSIONS

- Just like Si MOSFET solution, well below the limit. Also for 1-6GHz scanning.

Editor:	Ramm, GF-QP2
Date of Test:	2020-01-20
Operation Mode:	Ohmsche Last mit 4,8 Ohm, Volllast mit 500Watt, 110Volt AC
Comment:	Feststellung Unterschied mit Silicium und Silicium Carbit (EMV Unterschied). 2 te Messung nur mit Silicium, 110V

Full Spectrum



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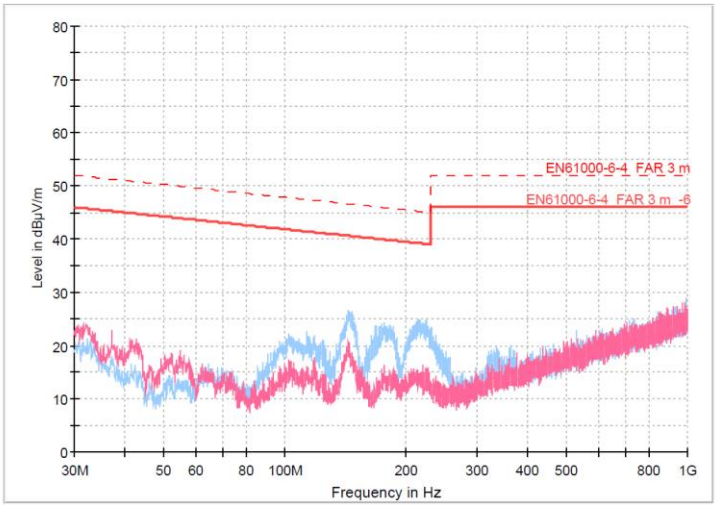
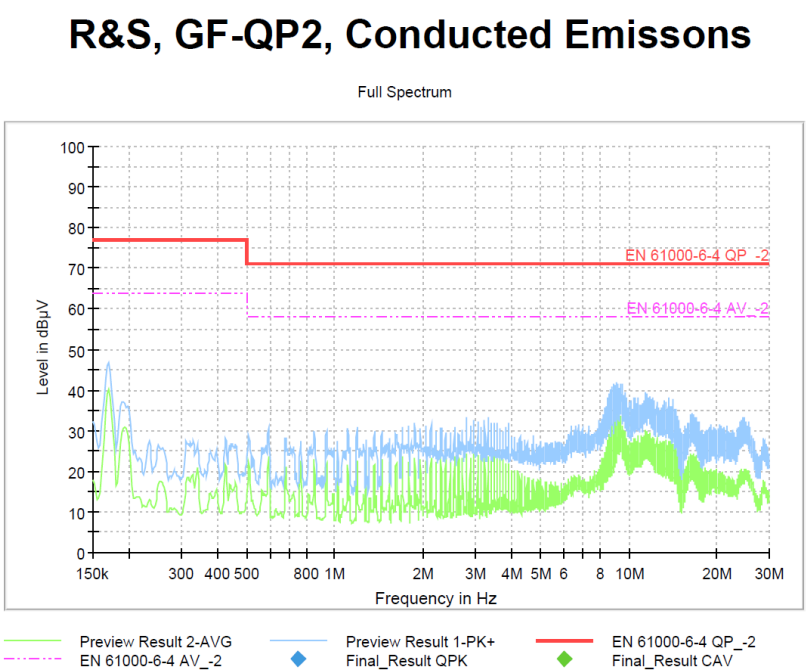


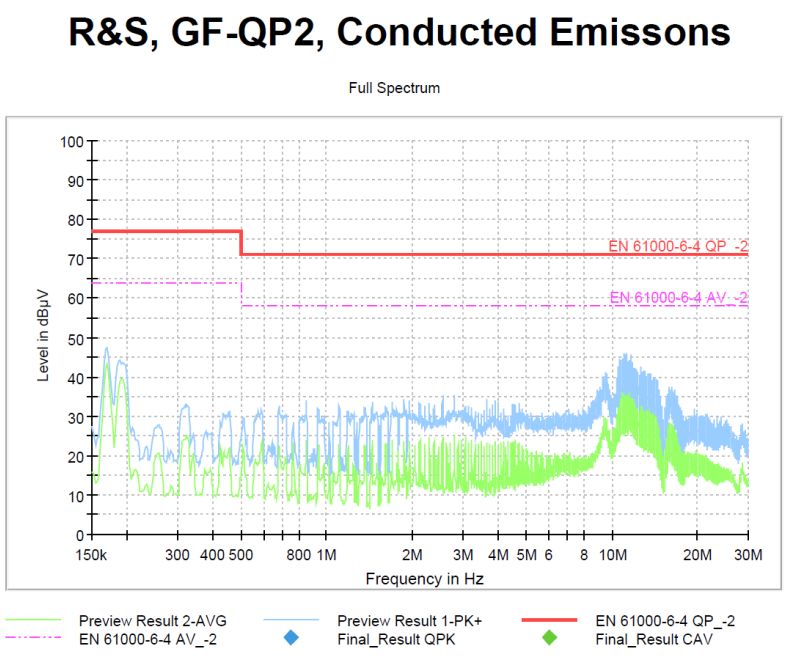
RESULT FROM COMPLIANCE TEST – CONDUCTED EMISSIONS

- As predicted by the pre-compliance tools, SiC MOSFET is not more noisy.

07_EN61000-6-4_CE_L1_Si 110V 2020-01-20 1

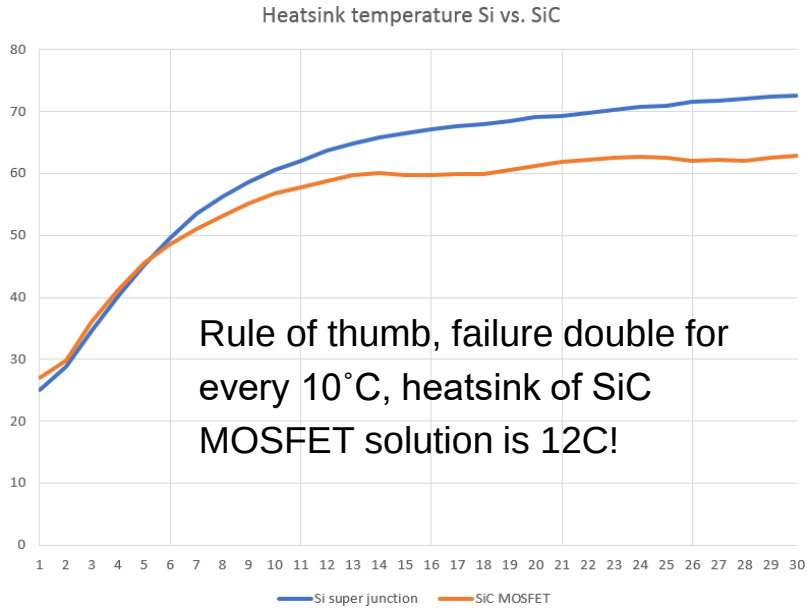


03_EN61000-6-4_CE_L1_Si-Car 110V 2020-01-20 1

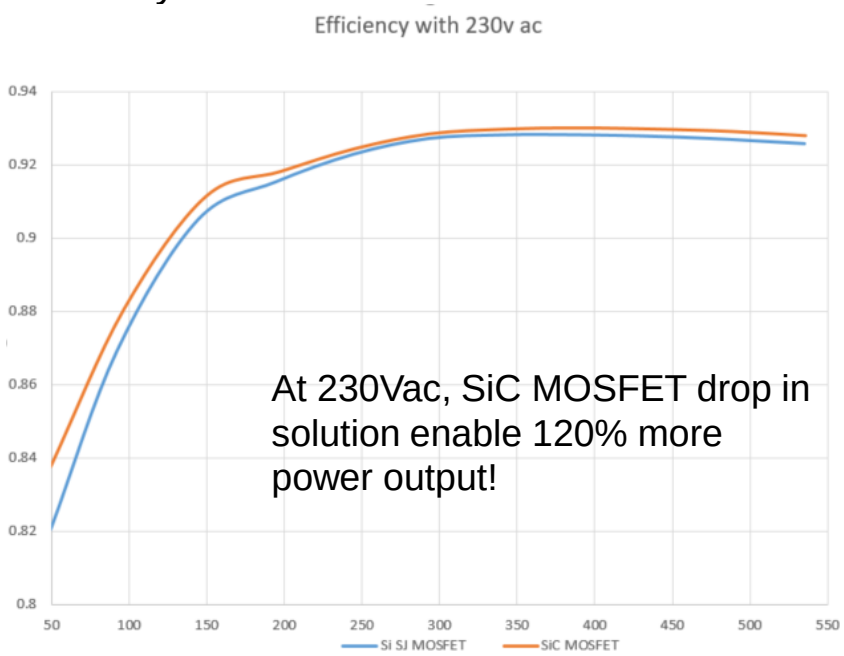


RESULT OF REDESIGN – OBJECTIVES OF USING SIC

- Why design with SiC? Reliability, efficiency, power density!



Rule of thumb, failure double for every 10˚C, heatsink of SiC MOSFET solution is 12C!



At 230Vac, SiC MOSFET drop in solution enable 120% more power output!

CONCLUSION

- With the right implementation and strategy, SiC is NOT more challenge to pass compliance certification test than Si.
- Suitable measurement tools like an oscilloscope in combination with accessories and additional software are a tremendous help to identify problems and save cost and time.

THANK YOU!

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