Webinar

MIPI D-PHY 2.1/2.5 COMPLIANCE TESTING WITH RTP OSCILLOSCOPE

Guido Schulze, Product Manager, Oscilloscopes
Alessandro Cappelletti, Application Expert, Oscilloscopes

ROHDE&SCHWARZ

Make ideas real

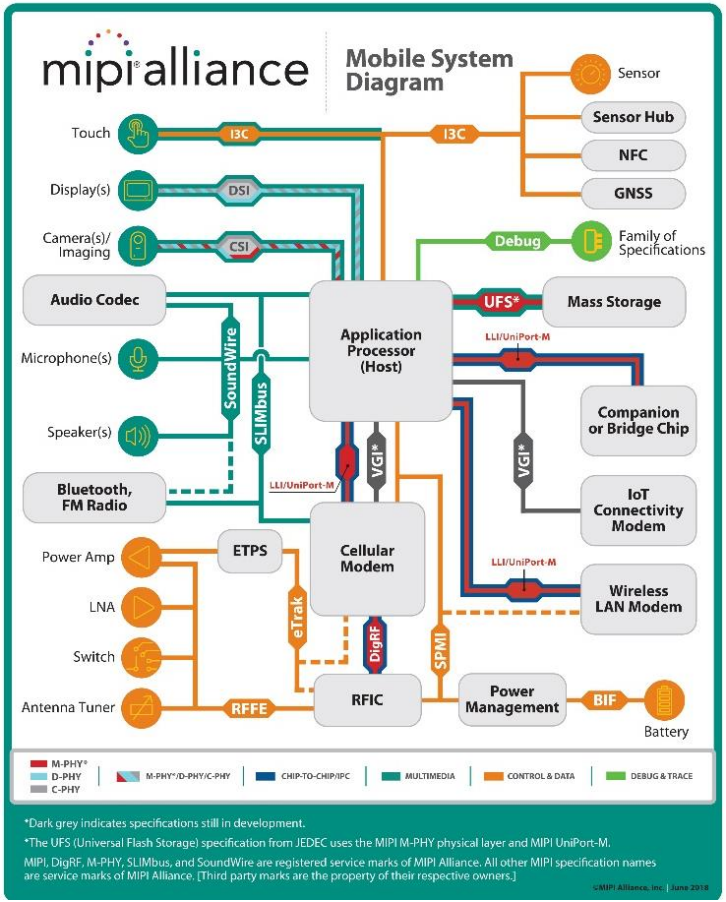
OUTLINE

- MIPI D-PHY Insights
- Compliance Testing
- Live Demonstration
- Summary

MIPI D-PHY INSIGHTS

WHAT IS MIPI D-PHY

- Physical layer defined by MIPI Alliance
- Especially for mobile applications
- Primarily for camera and display
- Highspeed data interface
- Expands to other industries

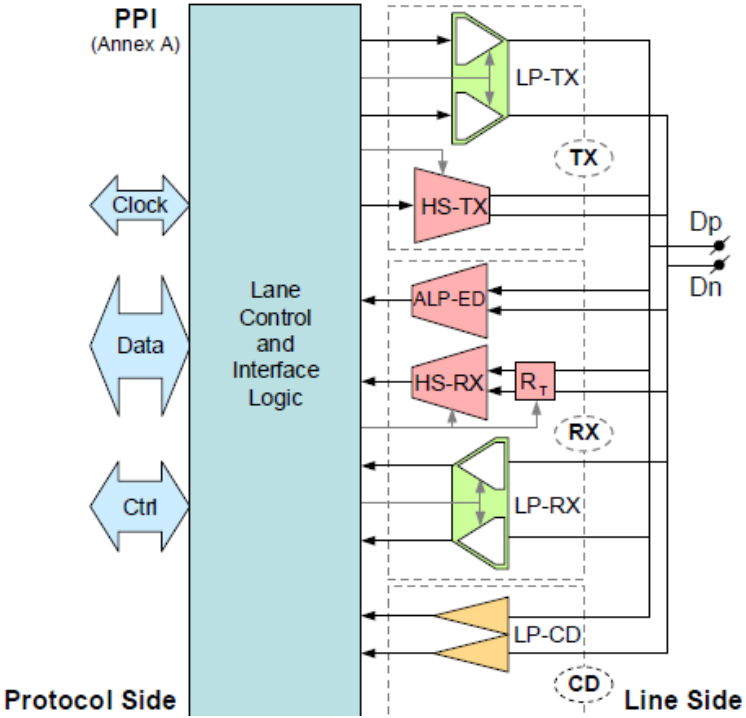


Source: MIPI Alliance

MARKET TRENDS

- Mobile/ Consumer:
  - Continued display & camera innovation on smartphones
- Automotive:
  - Lidar, Radar, etc. for autonomous drive
- Industrial:
  - Higher resolution

MIPI D-PHY SIGNALS

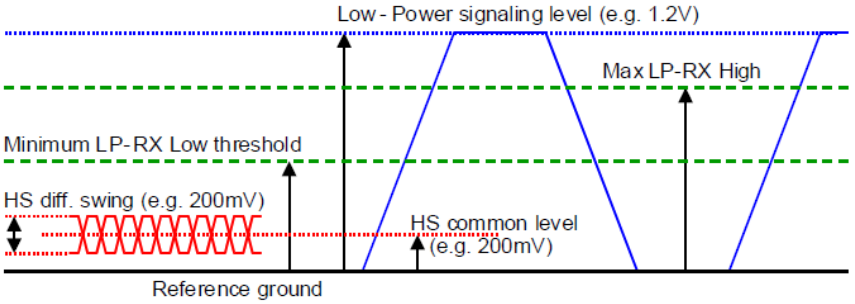


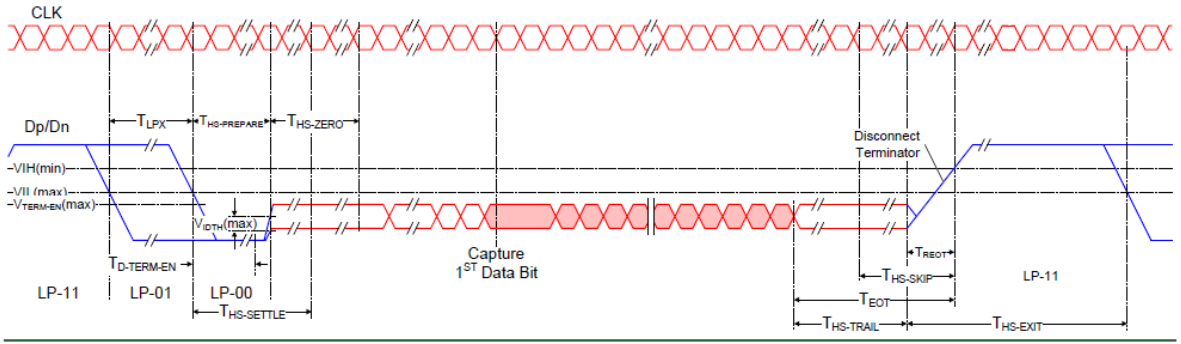
- Source-Synchronous: one or more data lanes (uni- or bidirectional) and 1 clock (master to slave)
- High-speed signalling for fast data traffic (differential signalling)
  - 80 to 1500 Mbps per lane without deskew calibration.
  - Up to 2500 Mbps per lane with deskew calibration.
  - Up to 4500 Mbps per lane with equalization.
- Low-Power signalling for control purposes (single-ended) or low speed communication (differential)

Source: MIPI Alliance

MIPI D-PHY SIGNALS

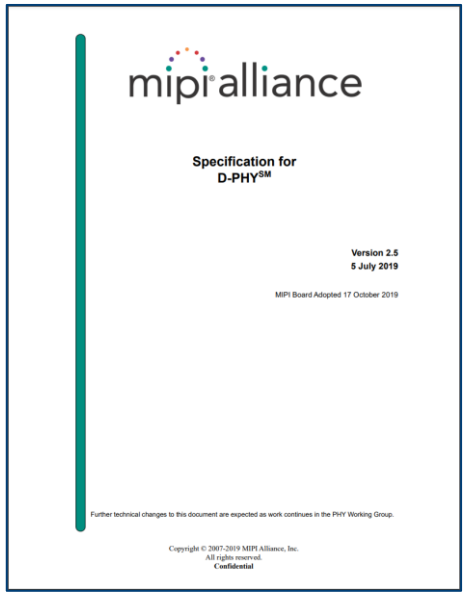
- High-speed mode:
  - LVDS
- Low-Power mode:
  - 2x single-ended
- Alternate Low-Power (ALP) mode:
  - low voltage levels of HS
  - unterminated

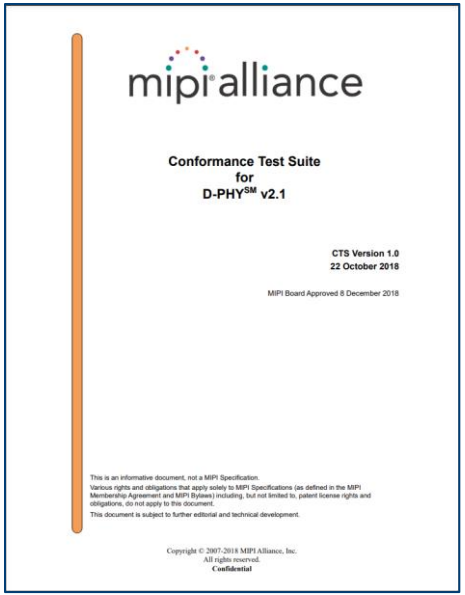




Source: MIPI Alliance

SPECIFICATIONS BEHIND





Specification	Date	Diff	Specification Status	Test Materials
D-PHY℠ v3.0	21-Jul-2021	Diff	Recommended	—
D-PHY℠ v2.5	17-Oct-2019	Diff	Superseded	—
D-PHY℠ v2.1	28-Mar-2017	Diff	Superseded	CTS
D-PHY℠ v2.0	08-Mar-2016	Diff	Superseded	—
D-PHY℠ v1.2	10-Sep-2014	Diff	Superseded	CTS
D-PHY℠ v1.1	16-Dec-2011	Diff	Superseded	CTS
D-PHY℠ v1.0	22-Sep-2009	—	Superseded	CTS

Source: MIPI Alliance

EVOLUTION OF THE STANDARD

D-PHY Feature Roadmap

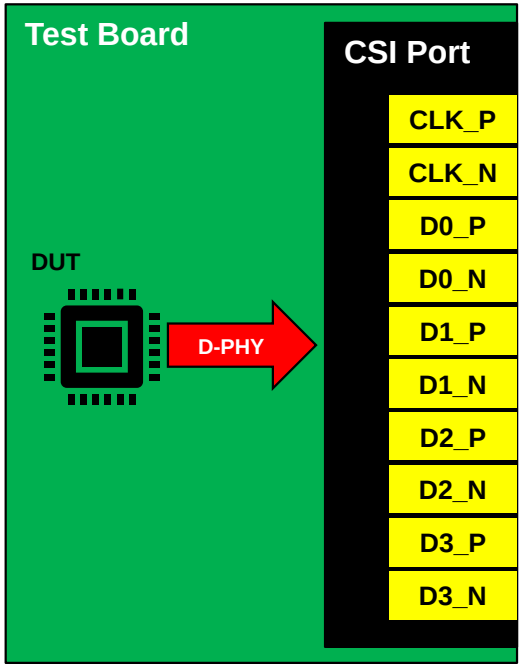
Category	Feature	v1.0	v1.1	v1.2	v2.0	v2.1	v2.5	v3.0
	Board Adoption	4Q 09	4Q 11	3Q 14	1Q 16	1Q 17	3Q 19	3Q 21
Symbol Rate (Gbps/Lane)	Standard Channel	1	1.5	2.5	4.5	4.5	4.5	9
	Short Channel					6.5	6.5	11
Increased Symbol Rate	Basic De-emphasis				✓	✓	✓	✓
	Calibration			✓	✓	✓	✓	✓
	Additional UI Jitter (RCLK jitter) specs		✓	✓	✓	✓	✓	✓
	Rx Equalization							✓
Power Reduction	Unterminated Mode				✓	✓	✓	✓
	Reduced Amplitude "LVLP" Mode option					✓	✓	✓
LP Mode	Alternate Low-Power Mode						✓	✓
Enhanced Function	16-bit/32-bit PPI				✓	✓	✓	✓
	Optical Interconnect				✓	✓	✓	✓
	HS Reverse Mode	✓	✓	✓	✓	✓	✓	✓
	PHY Generated/Detected Packet Delimiter					✓	✓	✓
	Fast Lane Turnaround						✓	✓
	4m channel support, for IoT use cases				✓	✓	✓	✓
Protocol Specs	MIPI CSI-2®			v1.2/ v1.3		v2.0	v3.0	v4.0
	MIPI DSI-2℠	-	-	v1.1/ v1.0	v2.0	-	-	-

MIPI.ORG/DEVCON MOBILE & BEYOND 11

Source: MIPI DevCon Sep. 2022

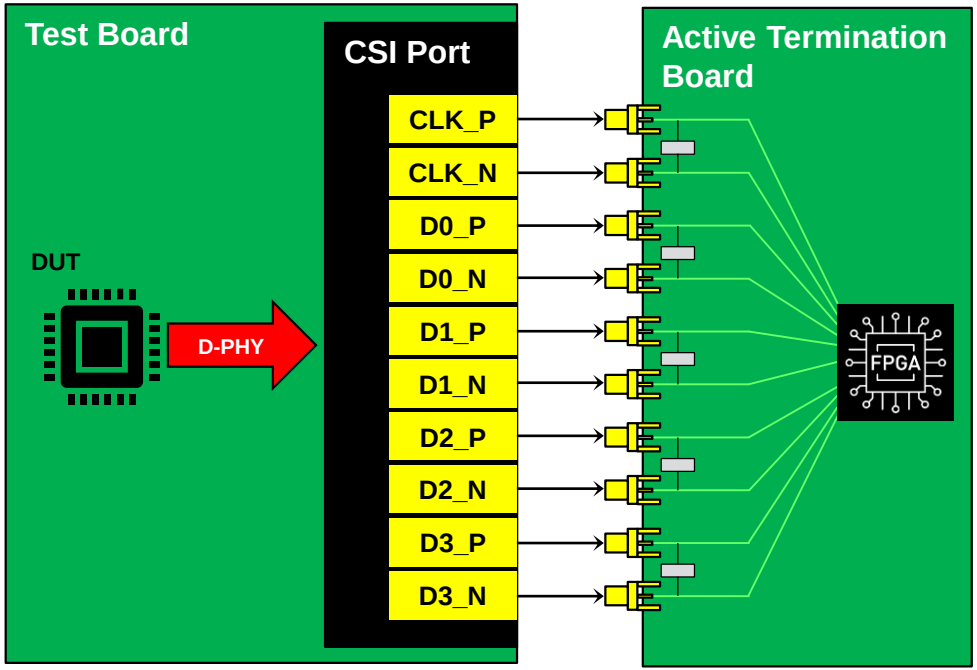
COMPLIANCE TESTING

COMPLIANCE TESTS
TYPICAL SETUP



1 Clock Lane
Up to 4 Data Lanes

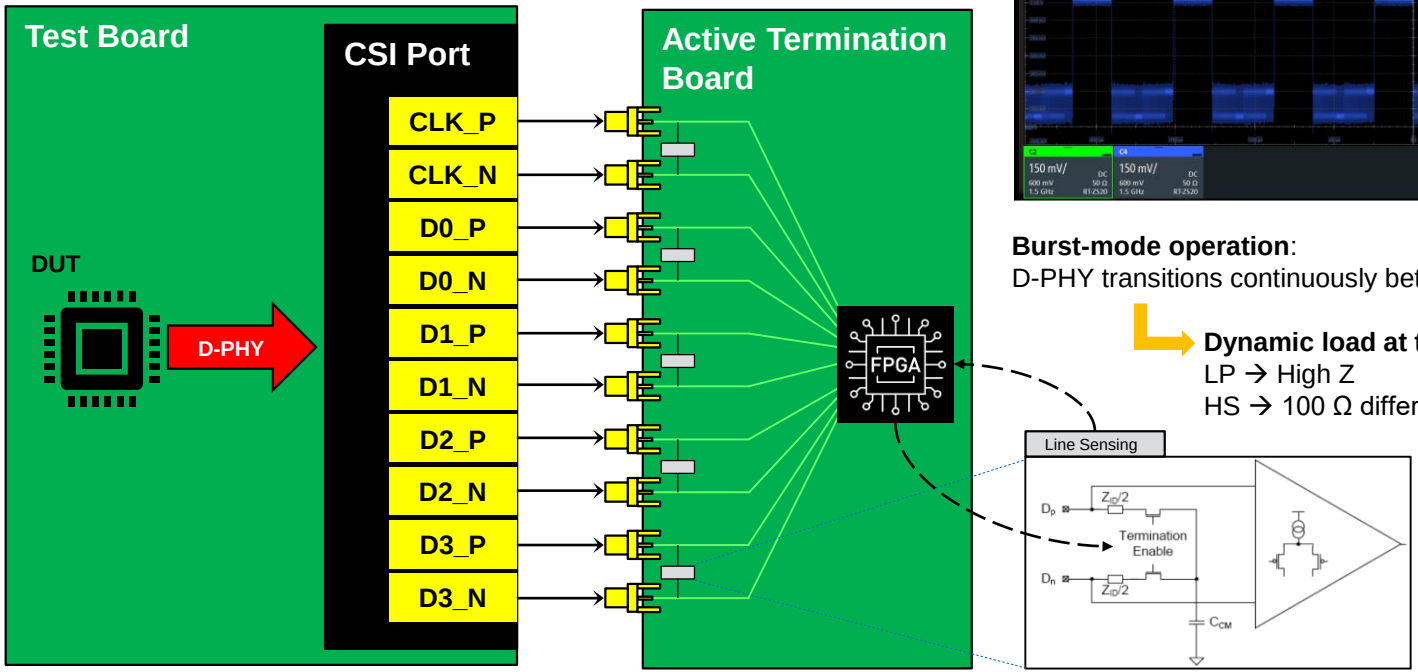
COMPLIANCE TESTS
TYPICAL SETUP



Burst-mode operation:
D-PHY transitions continuously between LP and HS

Dynamic load at the receiver:
LP → High Z
HS → 100 Ω differential, AC-coupled to ground

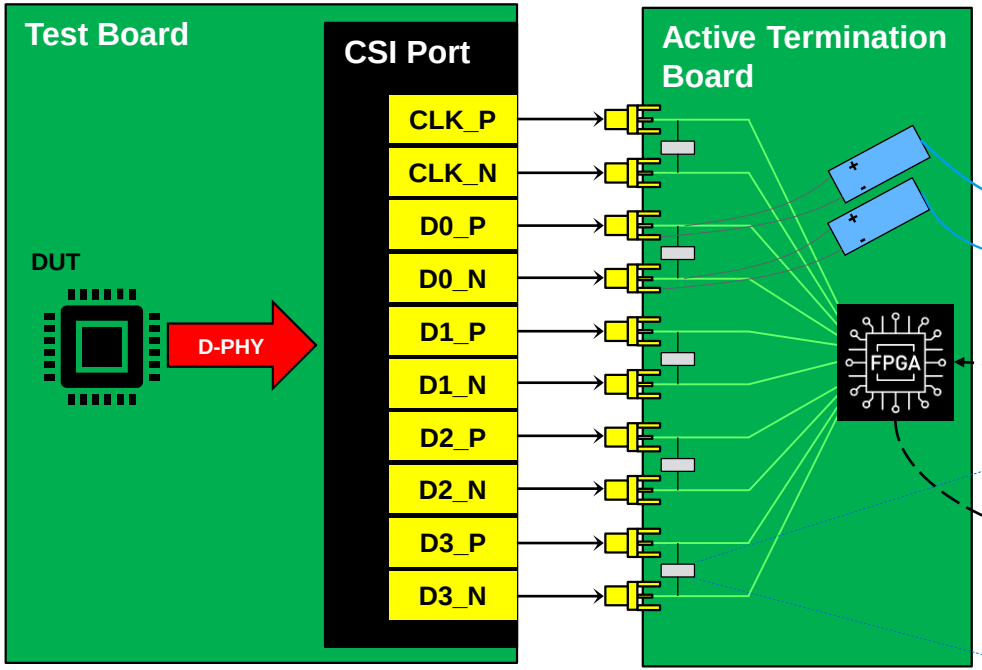
COMPLIANCE TESTS
TYPICAL SETUP

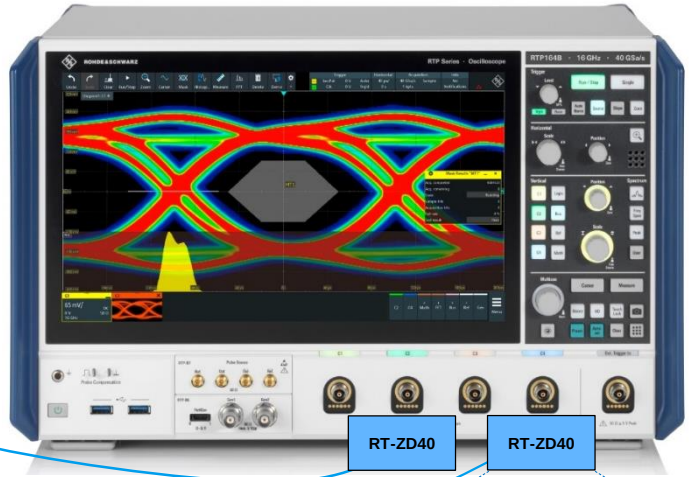


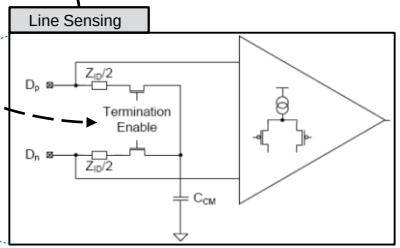
Burst-mode operation:
D-PHY transitions continuously between LP and HS

Dynamic load at the receiver:
LP → High Z
HS → 100 Ω differential, AC-coupled to ground

COMPLIANCE TESTS
TYPICAL SETUP







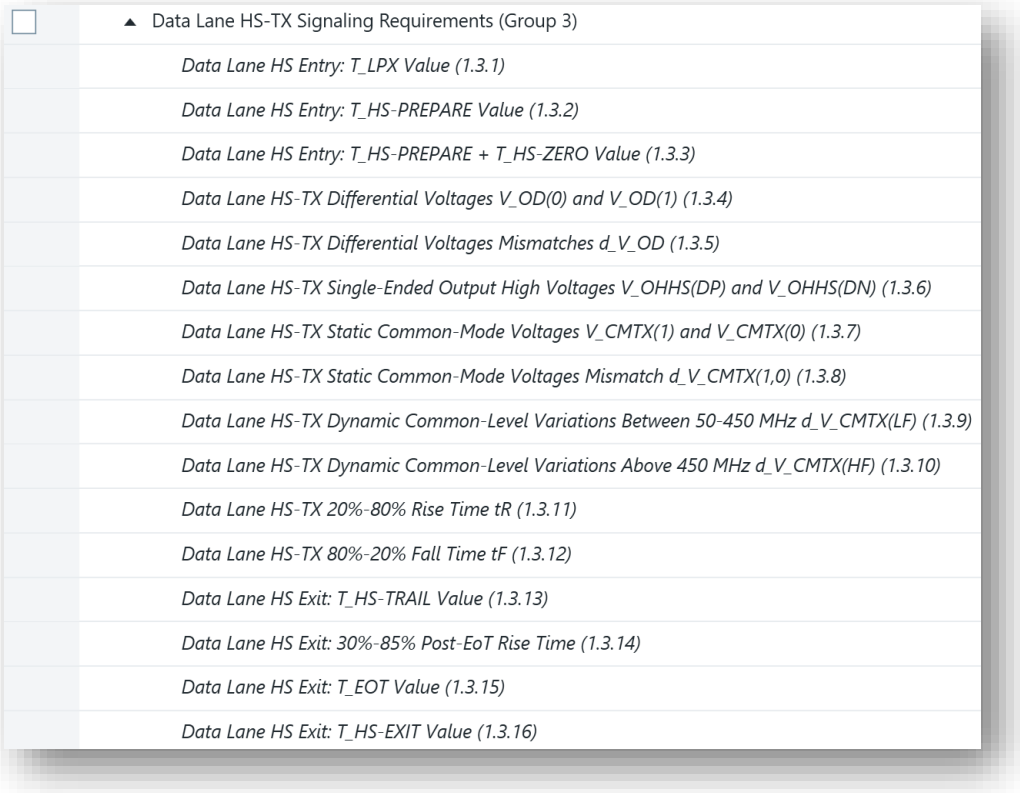
COMPLIANCE TESTS
TEST CASES

► CTS v2.1 describes 6 test groups

- Group 1 (1.1.x) verifies various requirements specific to Data Lane LP-TX signaling.
- Group 2 (1.2.x) verifies various requirements specific to Clock Lane LP-TX signaling.
- Group 3 (1.3.x) verifies various requirements specific to Data Lane HS-TX signaling.
- Group 4 (1.4.x) verifies various requirements specific to Clock Lane HS-TX signaling.
- Group 5 (1.5.x) verifies various requirements specific to HS-TX Clock-to-Data-Lane timing.
- Group 6 (1.6.x) verifies various requirements specific to Initialization, ULPS, and BTA behavior.

COMPLIANCE TESTS
TEST CASES

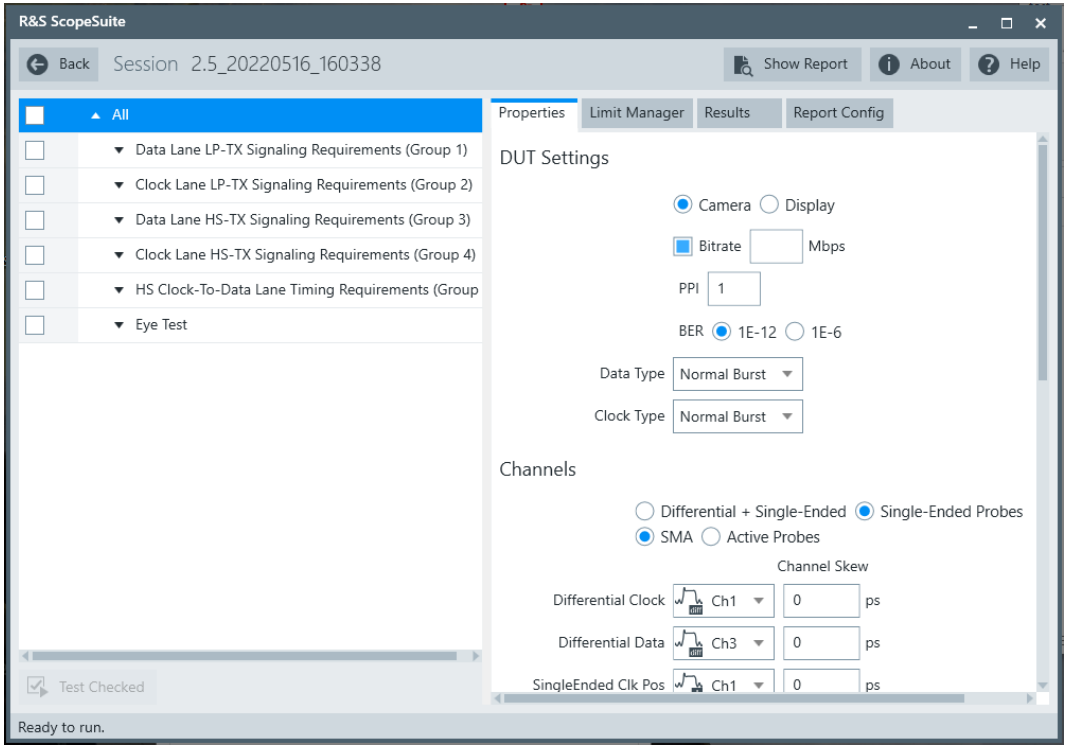
- Example of Group 3 test cases:
  - timing and voltage tests



ROHDE & SCHWARZ TEST SOLUTION

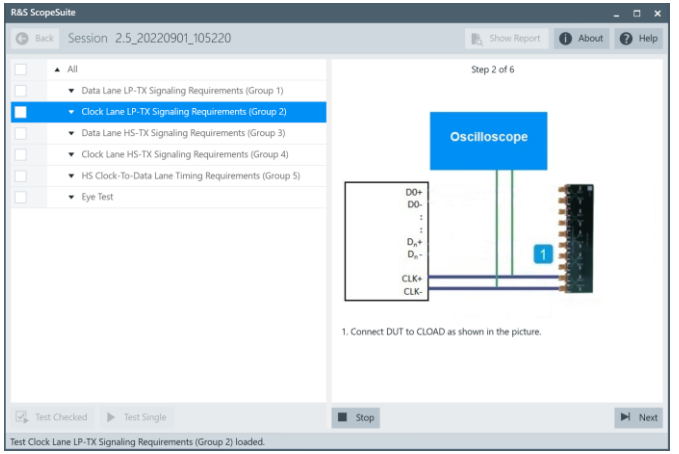
MIPI D-PHY COMPLIANCE

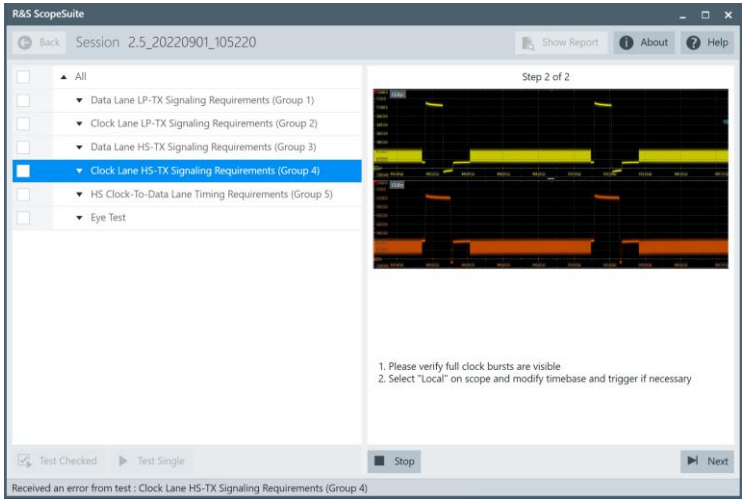
- **Options:**
  - RTP-K26: V.1.2
  - RTP-K27: V.2.1/2.5
- **Functions:**
  - Guided Tx compliance tests
  - Data & Clock lane test for LP and HS mode
  - Detailed Report
- **Advantages:**
  - Support of latest standard
  - Support of Eye Test



R&S TEST SOLUTION GUIDED STEPS

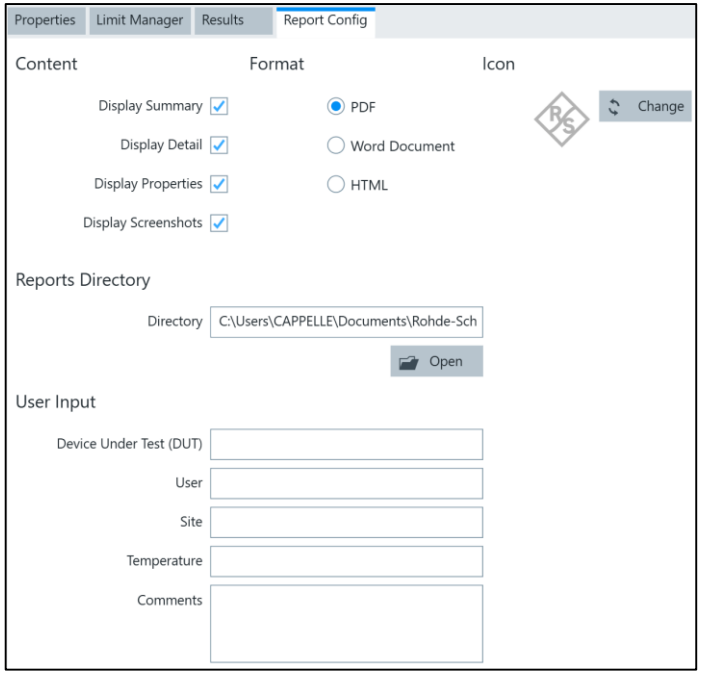
- The R&S ScopeSuite guides the user with supporting illustrations step-by-step

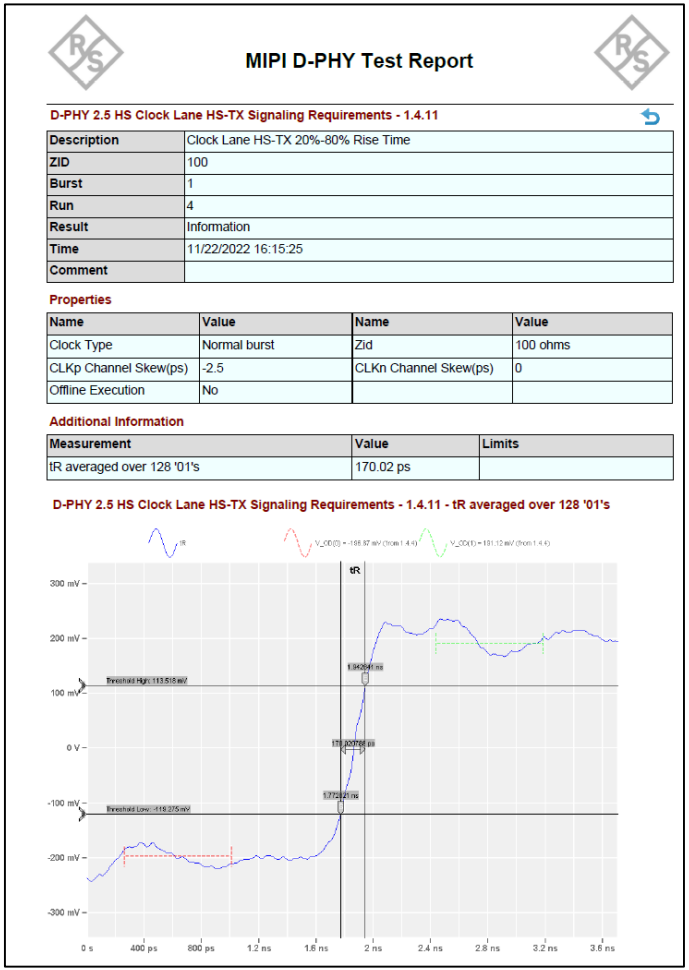




R&S TEST SOLUTION
DETAILED REPORT

- Configurable Report in selectable format





MIPI D-PHY Test Report

D-PHY 2.5 HS Clock Lane HS-TX Signaling Requirements - 1.4.11

Description	Clock Lane HS-TX 20%-80% Rise Time
ZID	100
Burst	1
Run	4
Result	Information
Time	11/22/2022 16:15:25
Comment	

Properties

Name	Value	Name	Value
Clock Type	Normal burst	Zid	100 ohms
CLKp Channel Skew(ps)	-2.5	CLKn Channel Skew(ps)	0
Offline Execution	No		

Additional Information

Measurement	Value	Limits
tR averaged over 128 '01's	170.02 ps	

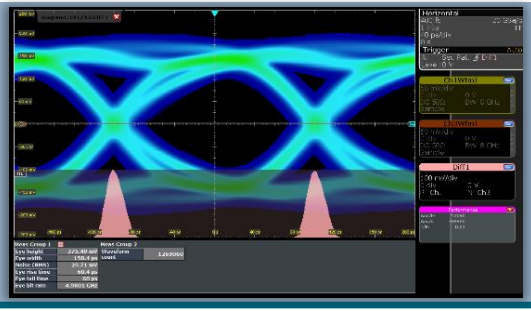
D-PHY 2.5 HS Clock Lane HS-TX Signaling Requirements - 1.4.11 - tR averaged over 128 '01's

SIGNAL INTEGRITY DEBUGGING

R&S RTP OSCILLOSCOPE: Unique Analysis Functions

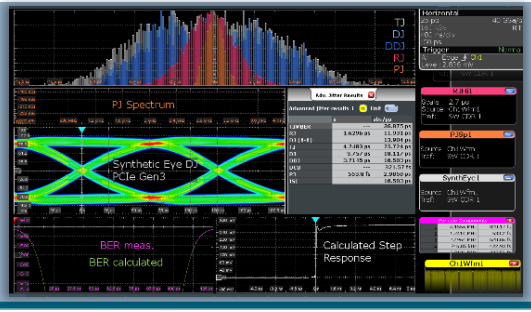
Fastest Eye Diagram Analysis

- CDR based triggering
- Real-time deembedding
- Real-time differential math
- Real-time analysis (histogram, mask)



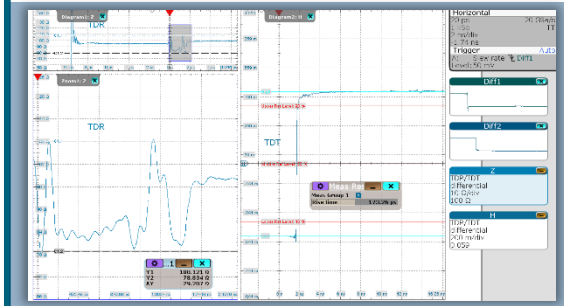
Most detailed Jitter & Noise Decomposition

- Histograms for all components
- Track and Spectrum views
- Eye diagram, BER bathtub
- Step/Frequency response



Most versatile TDR/TDT Analysis

- 16 GHz differential Pulse Source
- TDR / TDT Analysis SW
- Guided calibration & measurement
- PacketMicro Probe



R&S TEST SOLUTIONS
ADDITIONAL MIPI OPTIONS

- **Compliance**
  - RTP-K28: MIPI C-PHY

- **Triggering and Decoding**
  - RTO/P-K40: MIPI RFFE
  - RTO/P-K42: MIPI D-PHY based DSI and CSI-2
  - RTO/P-K44: MIPI M-PHY physical layer and UniPro protocol layer

LIVE DEMONSTRATION

SUMMARY

TYPICAL CONFIGURATION: MIPI D-PHY REV 2.1/2.5

#	Type	Description
1x	RTP134	13 GHz High-performance oscilloscope
2x	RT-ZM130	13 GHz Modular probe (HS mode)
2x	RT-ZMA10	Solder-in probe tips
2x	RT-ZD40	4.5 GHz differential probe (LS mode)
1x	RTP-K27	MIPI D-PHY 2.1/2.5 compliance test option
1x	RTP-K136	8 Gbps Advanced Eye analysis option (for Clock delta UI, Clock Jitter)
1x	RTP-K140	8 Gbps Serial Pattern Trigger (for Clock and Data Eye)
Optional – Signal Integrity Debugging		
1x	RTP-SIBNDL	Signal Integrity Bundle (incl. Deemb., 16 Gbps serial pattern trigger w/ HW-CDR, etc.)
1x	RTP-K134	Jitter & Noise decomposition option
Test Fixtures		
1x	UNH-IOL-DPHY-RTB	Active Termination Board (order from https://license.unh.edu/products/iol/mipitestfixtures)
1x	CLOAD	MIPI D-PHY Capacitive Load Fixture

SUMMARY

- MIPI D-PHY is highspeed interface for displays, cameras, etc.
- Emerging applications in automotive, industrial, etc.
- R&S test solutions:
  - Automated compliance test
  - Signal integrity debugging
  - Triggering and decoding
- R&S RTP oscilloscope – most flexible & compact test solution

Find out more
www.rohde-schwarz.com

Thank you!

ROHDE&SCHWARZ
Make ideas real