ROHDE&SCHWARZ

以Double Pulse Tester協助寬能隙半導體於電源轉換器功率級的設計及驗證

Using Double Pulse Tester to Assist in the Design and Verification of Wide Bandgap-Based Power Stage for Converter/Inverter

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Outline

- Introduction
- Key Components
- DPT in Power Switch Applications
- DPT in Power Stage Design and Verifications
- DPT Demo

Objectives

Traditional applications of the DPT

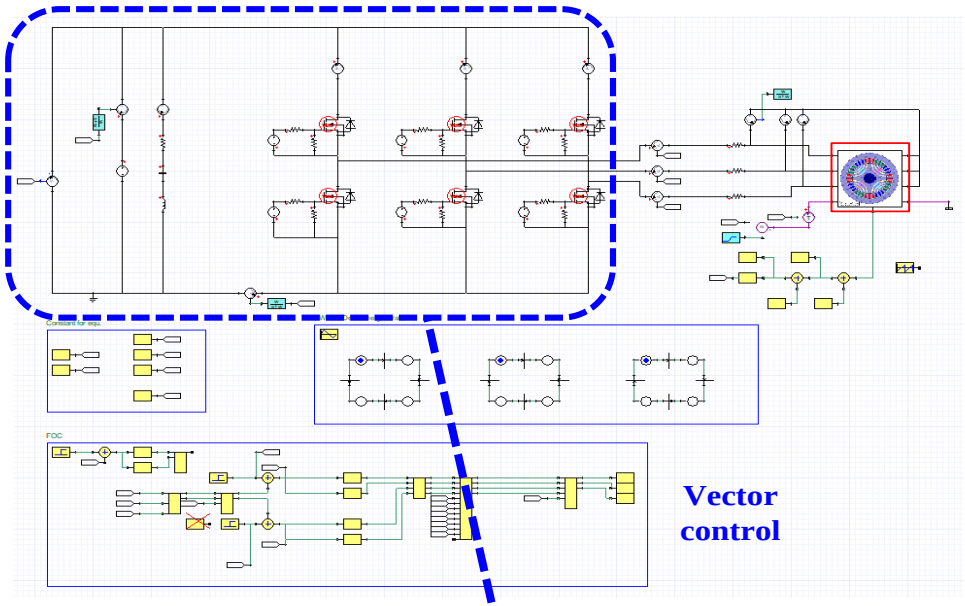
- Measure key parameters the power switch
- Measure voltage stress and loss for the power switch
- Investigate reverse characteristics for parasitic diode or diode
- Verify gate driver for the power switch

DPT applications for power stage design

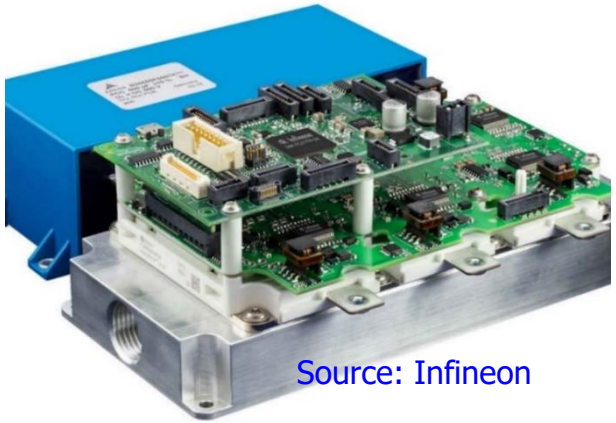
- Measure stray inductance(s) of the main power flow path
- Measure the influence of stray inductance(s) on the turn-off voltage spike of power switch
- Investigate the current sharing phenomena among paralleled power switches
- Verify the Spice model of the power switch
- Investigate magnetic flux saturation of the transformer/choke

Power Stage Design for Converter/Inverter

☐ Efficiency estimation and thermal design

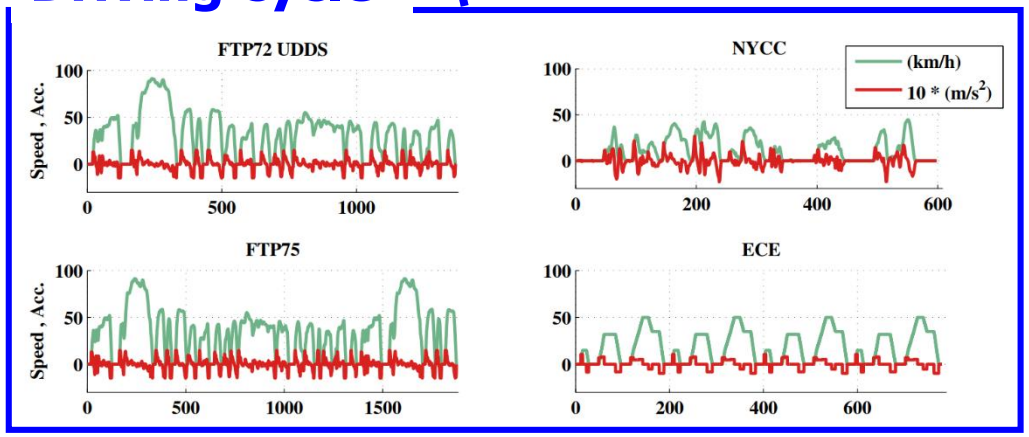


Estimate losses of power stage under required driving cycle and output power by Spice model using co-simulation for thermal design



Source: Infineon

Driving cycle



Virtual design

Power Stage Design for Converter/Inverter

☐ Key issues and tools for the power stage design

- ✓ Q3D: extract the parasitic parameters
- ✓ Spice model: characteristics analysis of power switch
- ✓ Twin Builder/circuit simulation S/W: operation of the power stage (stress/current sharing) and losses estimation for thermal design

Simulation Tools

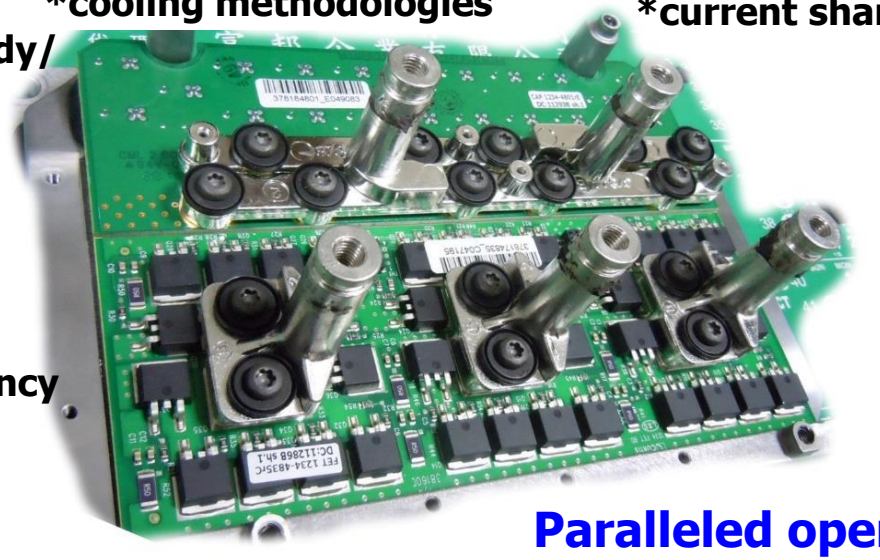
- ✓ Double pulse test: verify the simulation results

Verification

Power switch
*stress analysis
*characteristics of steady/ transient state
*losses

Thermal design
*losses estimation
*cooling methodologies

Busbar design
*stray inductance
*current sharing among capacitors



Power connection bar
*current density distribution
*loss

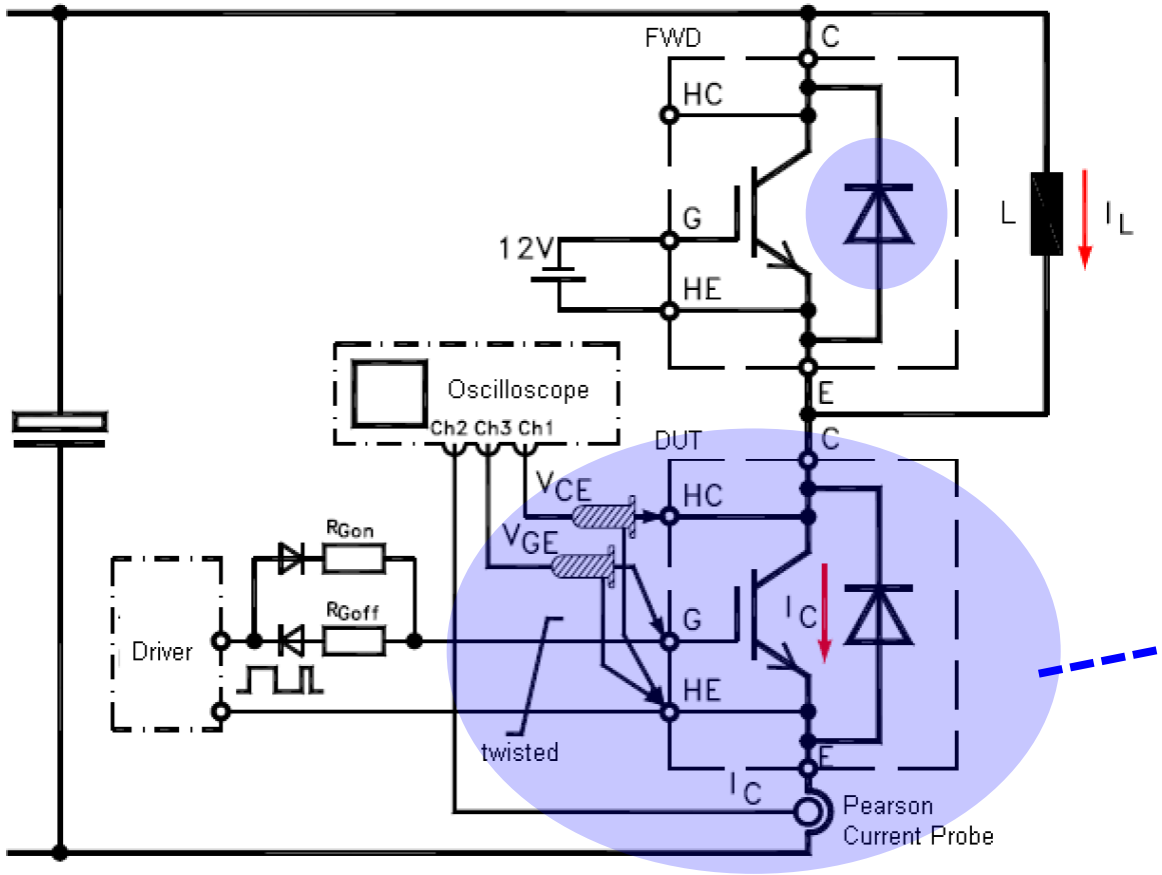
DC link capacitor
*impedance vs. frequency
*estimate losses

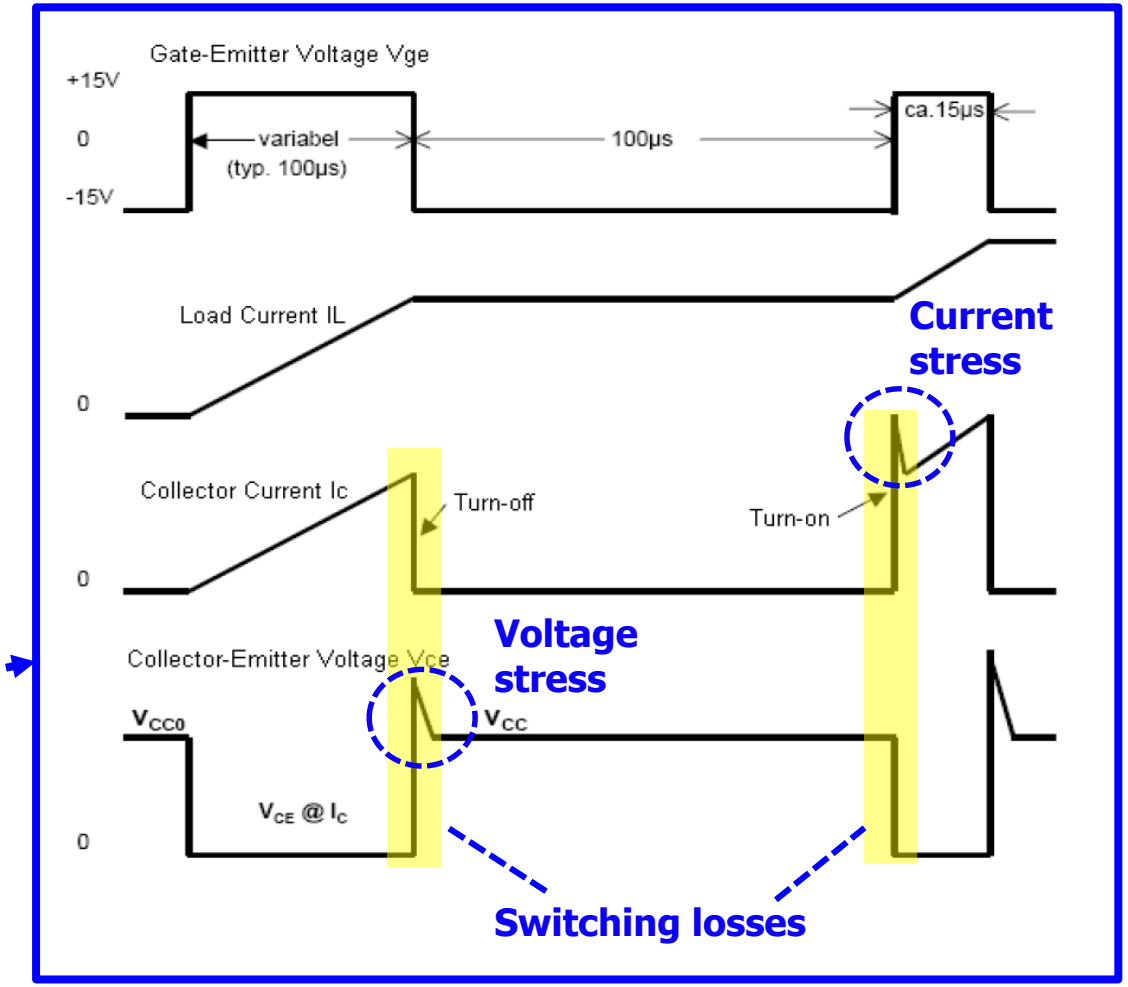
Paralleled operation of power switches
current sharing at steady and transient state

EMI/SI(Signal integrity)?

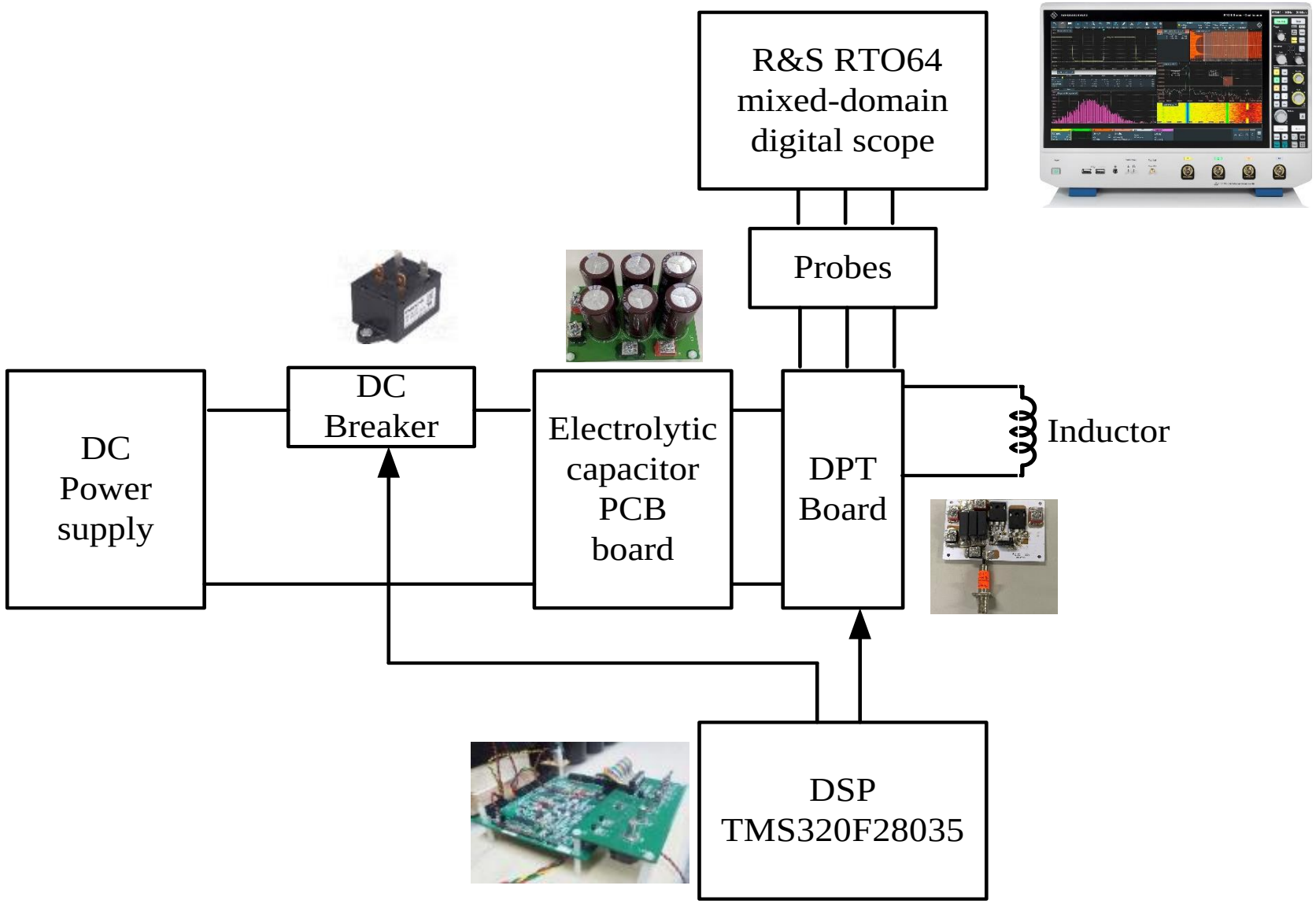
Fundamental of the DPT

☐ Equivalent circuit and test pattern

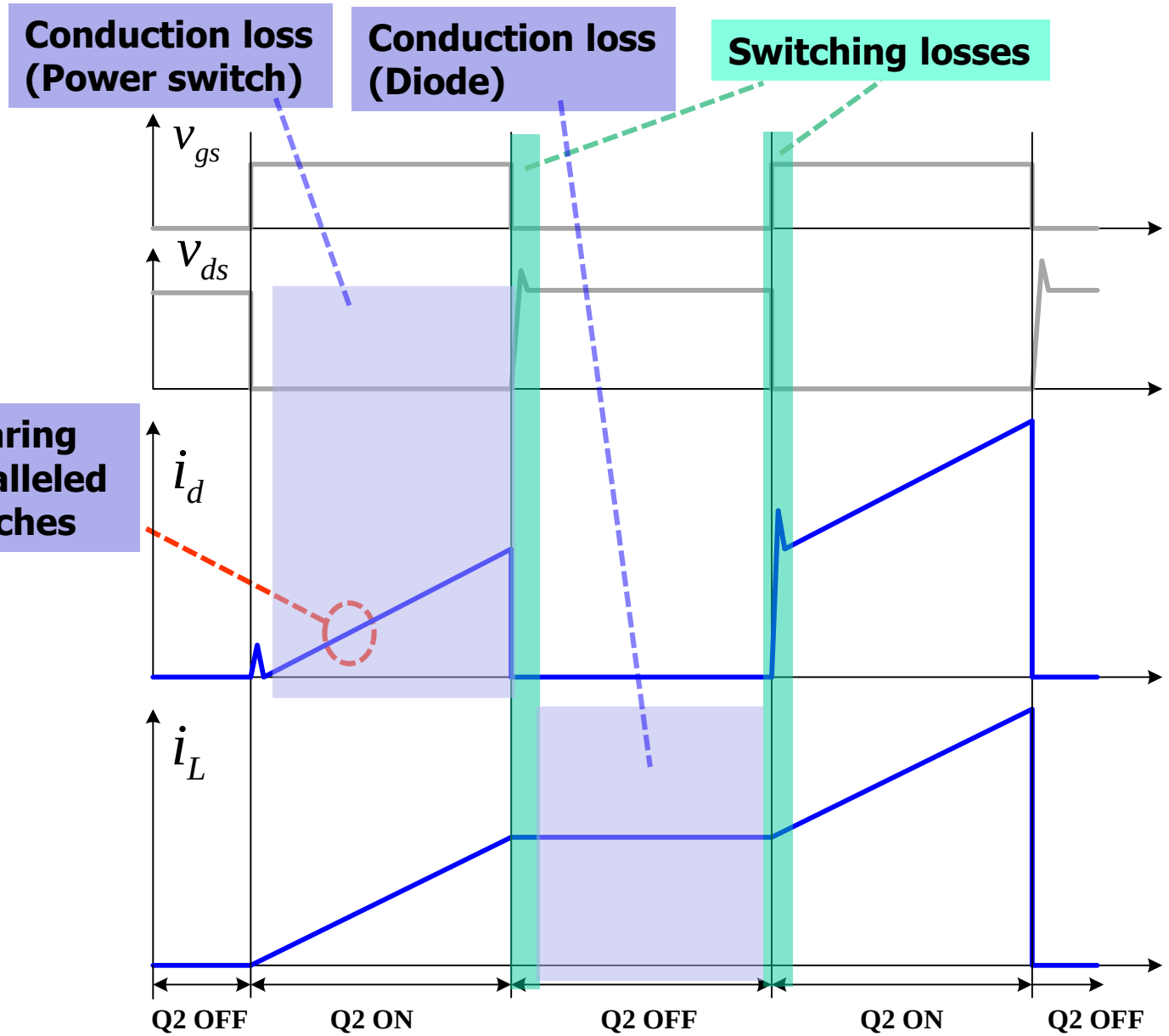




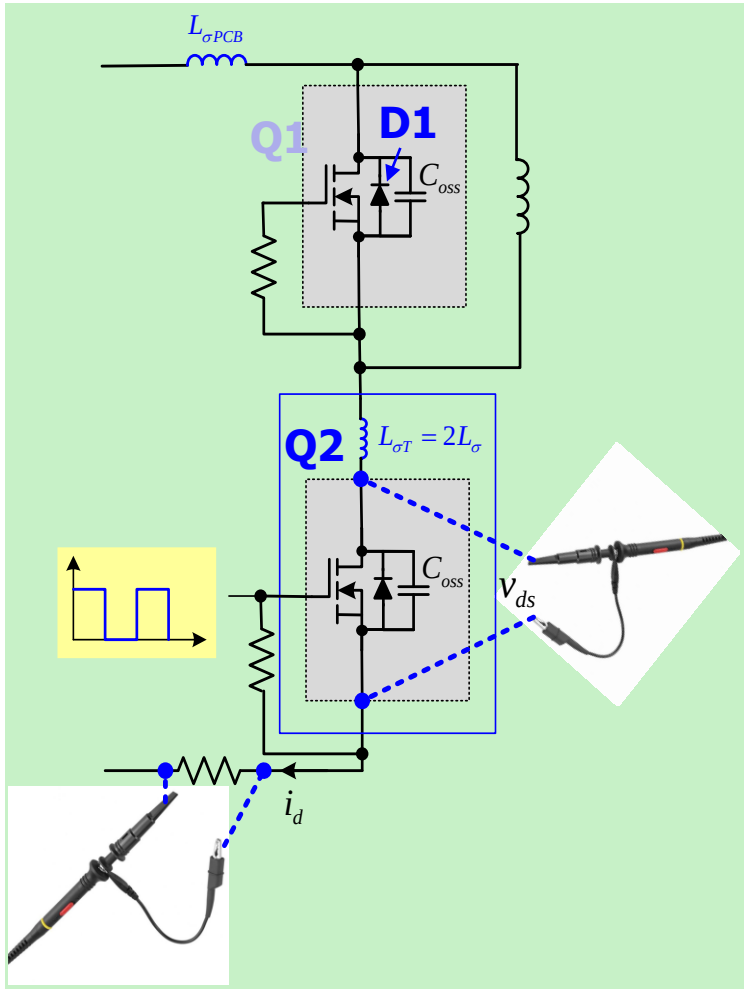
Double Pulse Tester – Function Block



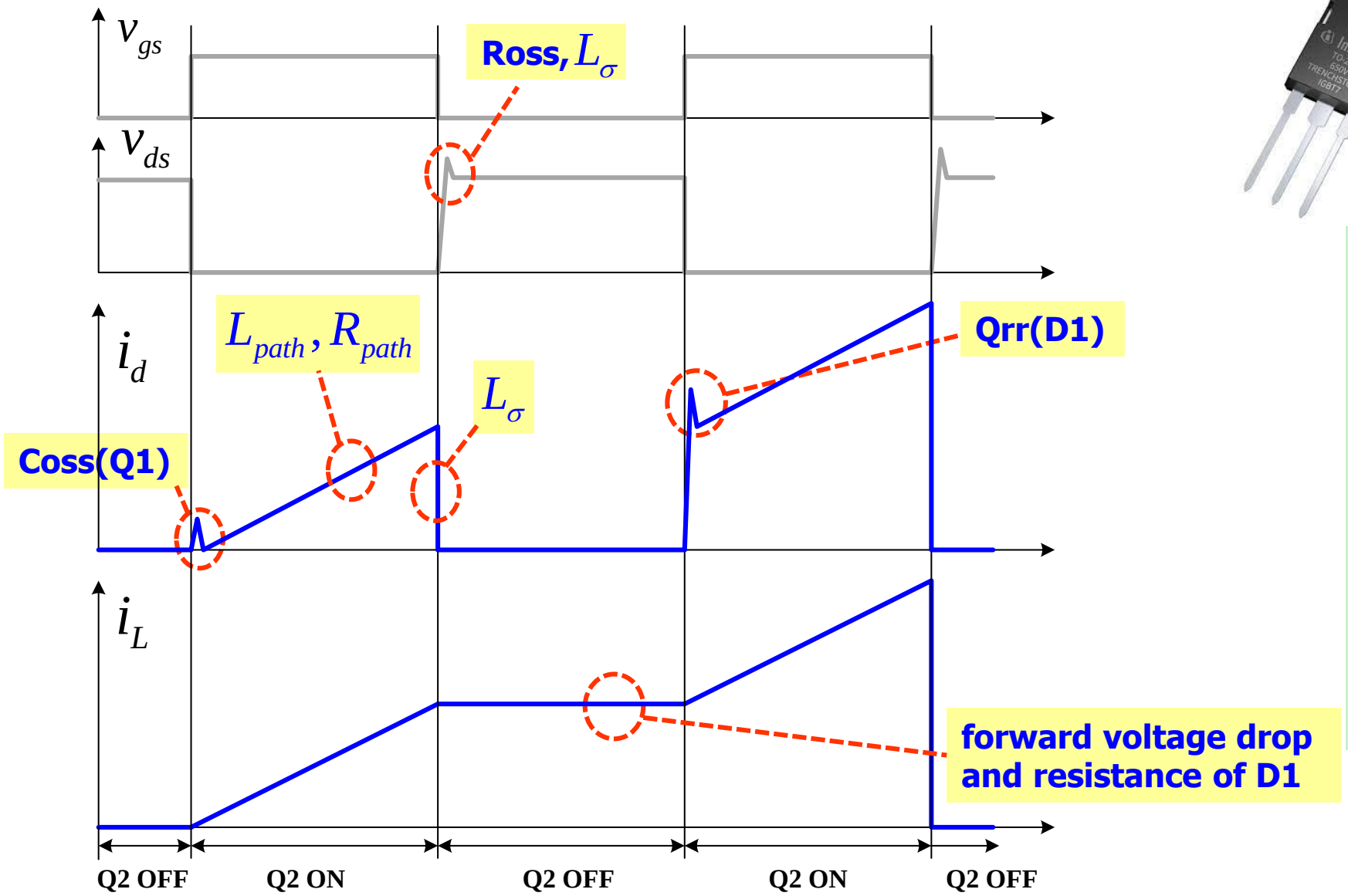
DPT Test Items

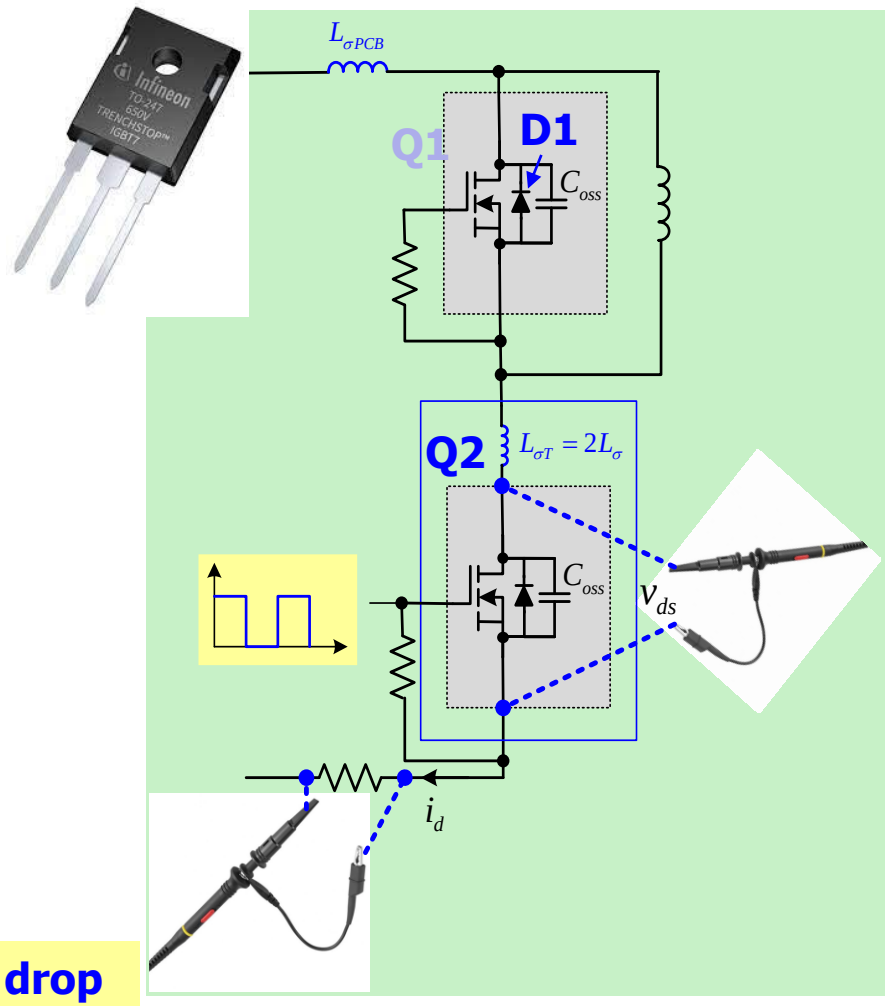


Current sharing among paralleled power switches



DPT Test Items





Double Pulse Tester Equipment

☐ Dynamic power device analyzer/double pulse tester

Static

Output characteristics On-resistance Threshold voltage Transconductance
Junction, input, output and reverse transfer capacitance Breakdown voltage Gate charge

Dynamic

Turn-on characteristics Turn-off characteristics Dynamic on-resistance
Dynamic current and voltage Switching characteristics
Reverse recovery Gate charge Derived output characteristics

Ruggedness testing(at high voltages and high temperatures)

Short-circuit conduction time Short-circuit energy Avalanche energy

DPT Parameters

Group	Parameters	Description	Associated Standards
Turn-On Characteristics	$t_{d(on)}$, t_r, t_{on}, $e_{(on)}$, dv/dt, di/dt	Characterizes how quickly the transistor can turn on, the maximum di/dt and dv/dt, and the resulting energy loss. Contributes to switching loss characteristic.	FET – IEC 60747-9 IGBT - 60747-8
Turn-Off Characteristics	$t_{d(off)}$, t_f, t_{off}, $e_{(off)}$, dv/dt, di/dt	Characterizes how quickly the transistor can turn off, the maximum di/dt and dv/dt, and the resulting energy loss. Contributes to switching loss characteristic.	FET – IEC 60747-9 IGBT - 60747-8
Switching Characteristics	I_d vs. t, $V_{ds,}$ vs. t, V_{gs} vs. t, I_g vs. t, Clamped V_{ds} vs. t, e vs. t, I_d vs V_{ds} (switching locus)	These time-based parameters are waveforms retrieved directly from the oscilloscope. The I_d vs V_{ds} (switching locus) are derived from the waveforms.	
Reverse Recovery	t_{rr}, Q_{rr}, E_{rr}, I_{rr}, I_d vs. t	Characterization of reverse recovery of body diode in vertical FETs. Provides additional timing information regarding how quickly the transistor can switch between on and off.	IEC 60747-8
Gate Charge	V_g vs. Q_g, (Q_{gs}(th), Q_{gs}(pl), Q_{gd})	The voltage and the current of the gate are measured during a double pulse turn-on operation. The charge on the gate during different gate voltage transitions is characterized. This parameter is used to determine the driving loss of the transistor.	IEC 60747-8 IEC 60474-9
Derived Output Characteristics	I_d vs. V_g, I_d vs. V_d	Provides basic transfer characteristics for the semiconductor.	

Double Pulse Tester (Board Level)

☐ Littelfuse

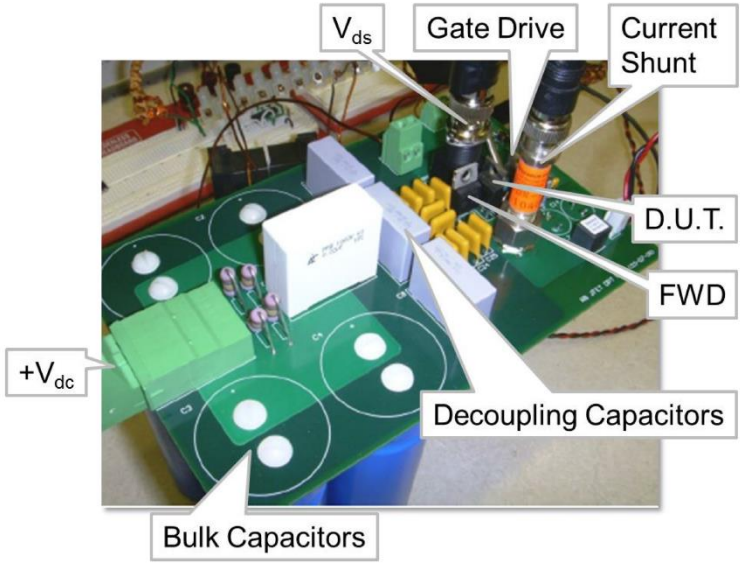
Electrical Specifications			
Parameter	Typical Value	Maximum Rating	Units
Input DC Link Voltage	800	1000	V
Input Control Voltage	12	13.2	V
Output Peak Current	-	100	A
Ambient Temperature	-	55	°C
Gate Driving Voltage	+20/-5	+22/-6	V

Source: Dynamic Characterization Platform-littelfuse

☐ Cree

Source: Evaluation Board for Cree's SiC MOSFET in a TO-247-4 Package

☐ VPEC



Source: High Temperature Characterization and Analysis of Silicon Carbide (SiC) Power Semiconductor Transistors

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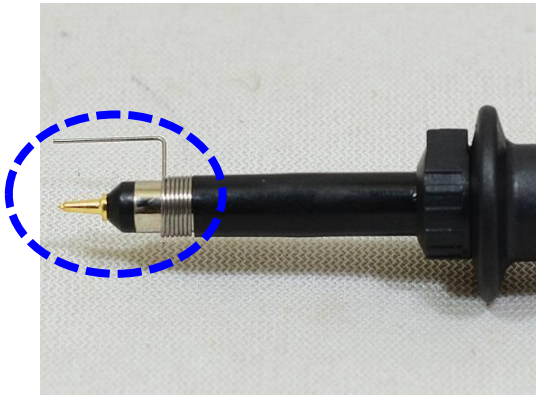
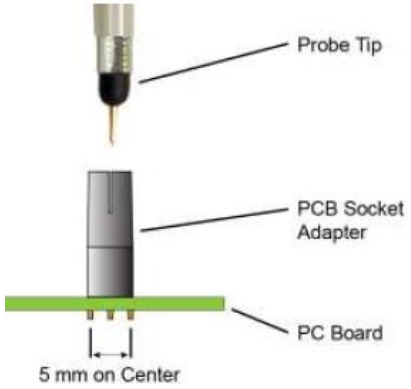
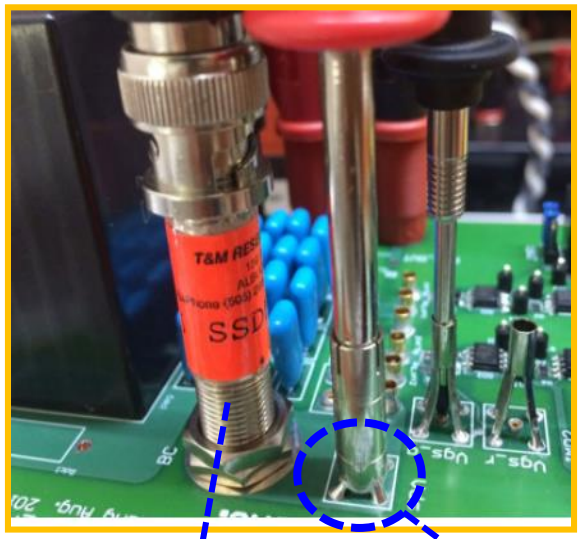
Double Pulse Tester – Sensors

☐ Short ground pin/probe tip adapter







Source: Dynamic Characterization Platform-littelfuse

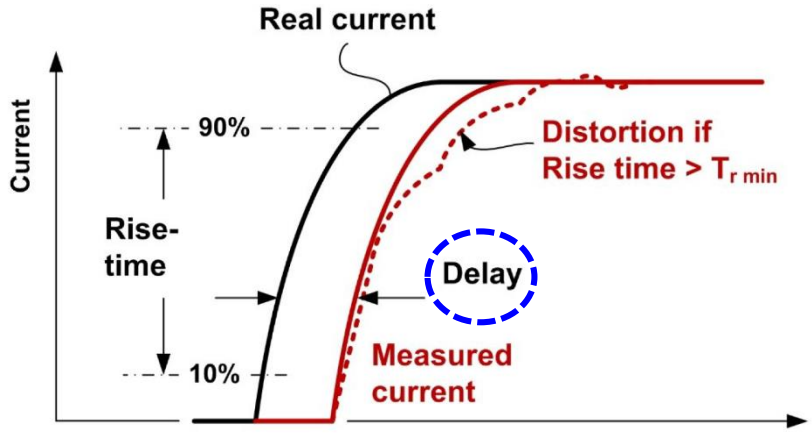
current sensor

Probe tip adapter for measuring voltage

☐ Fast response current sensor

	Current shunt resistor	Current transformer	Rogoski coil current probe
Pros	• Best accuracy • High bandwidth	• Isolated output	• Minimum insertion inductance • Isolated output • Smallest size
Cons	• Large size • Added loop inductance	• Large size • Added loop inductance • Lower bandwidth	• Low bandwidth • Not suitable for switching energy measurement
Best Use	• Eon/Eoff measurement	• Application where high bandwidth is not required	• High current measurement. e.g. Double pulse test
Equipment	**T&M research co-axial current shunt** • SDN-414-10 (0.1Ω, 2GHz bandwidth) • SSDN series for low insertion inductance  SDN series 	**Pearson 2877 current monitor** • 1V/A output • 200MHz/100A 	**PEM CWT Ultra Mini** • 9.2Hz-30MHz, 300A  

Source: Measurement Techniques for High-Speed GaN E-HEMTs-GaN Systems



Source: High Frequency Performance Delay, Rise-time and Peak di/dt

Double Pulse Tester – Current Sensor

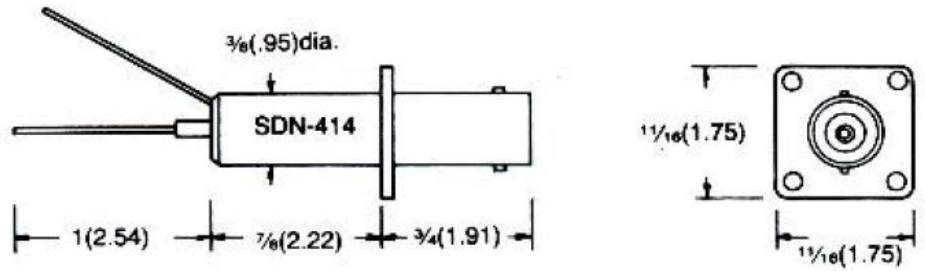
☐Current sensor – coaxial resistor

BW=1200MHz, rising time <=0.3ns, w/o delay and limited thermal capacity

SDN - 414 Series

SDN-414- 2 Watt Units - 1 5/8 Inch Case

Model	Resistance ohms	Bandpass MHz.	Risetime nsec.	Emax joules
SDN-414-01	0,01	400	1	6
SDN-414-025	0,025	1200	0,3	3
SDN-414-05	0,05	2000	0,18	2
SDN-414-10	0,1	2000	0,18	1



ORDERING INFORMATION

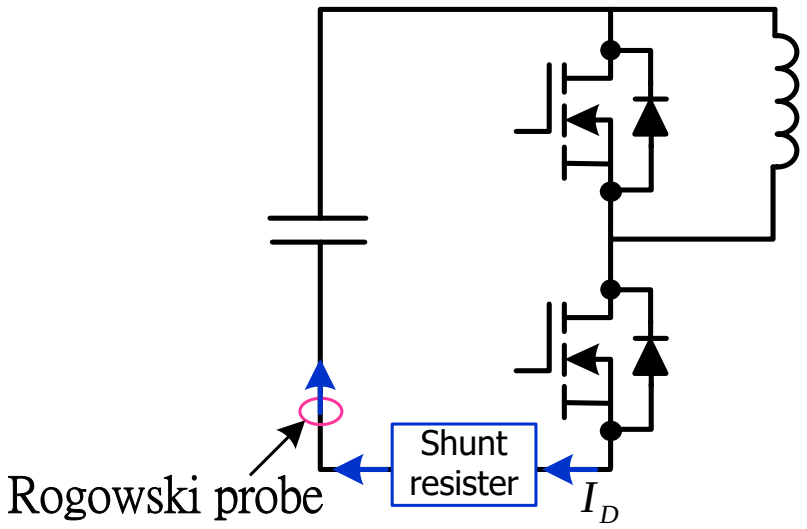
When ordering specify model number,wattage, and tolerance. Example: SDN-414-10, 2 watts, 4%.
Please specify type of load terminals: standard wire=SDN - flat low impedance strips = TTSDN

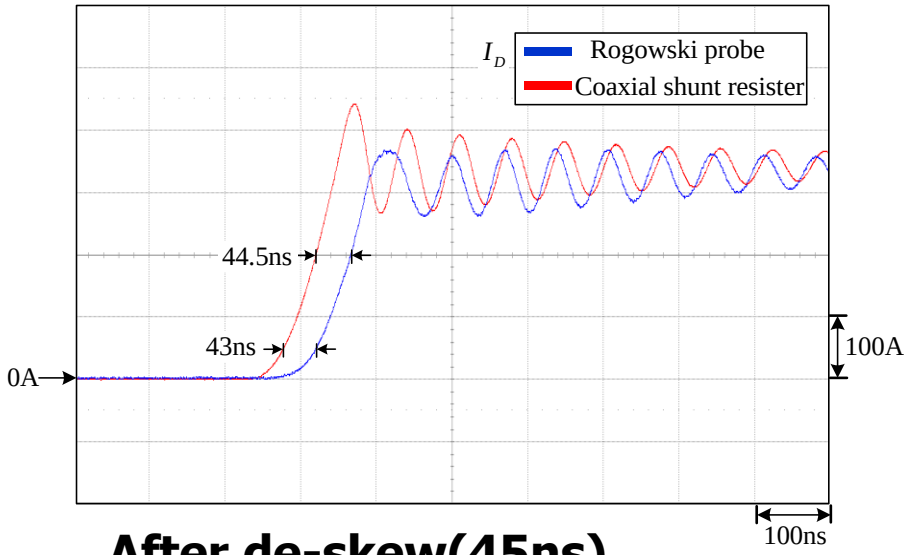
Source: Investigation of the inductor's parasitic capacitance in the high frequency switching of the high voltage cascode GaN HEMT

	Bandwidth	*Saturation*	*Linearity*	*Material Technology*
Rogowski	$0.1 \sim 100MHz$	No	Very good	simple
CT	$0.1Hz \sim 100MHz$	Yes	Fair	simple
Hall	$< 1MHz$	Yes	Poor	complicated
GMR	$DC \sim 5MHz$	Yes	Fair	Very complicated
GMI	$DC \sim 30GHz$	No	Fair	Very complicated
Shunt	$DC \sim 10MHz$	No	Very good	simple
Coaxial Shunt	$DC \sim 2GHz$	No	Very good	simple

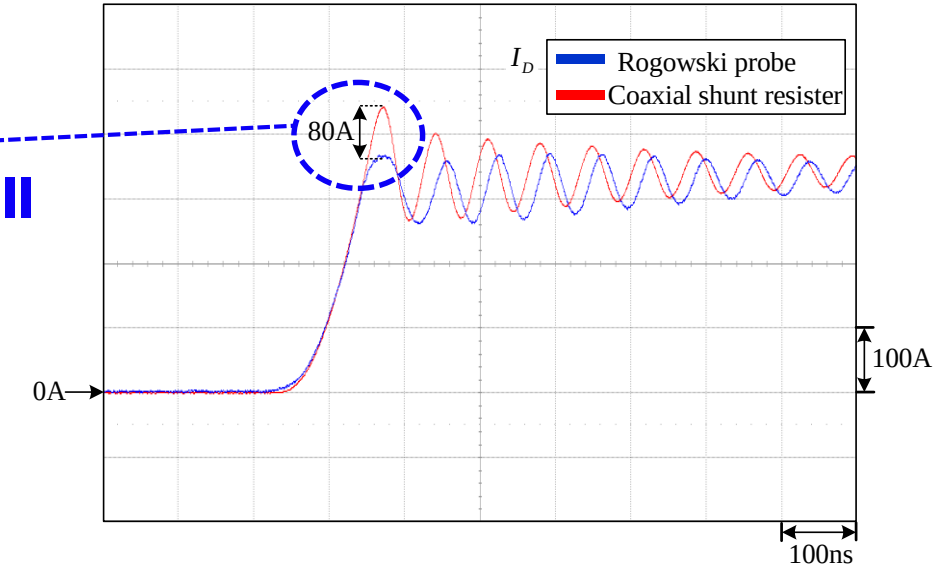
Double Pulse Tester – Current Sensor

- Calibration of the Rogowski probe by high BW coaxial shunt resistor and **higher current.**





After de-skew(45ns)

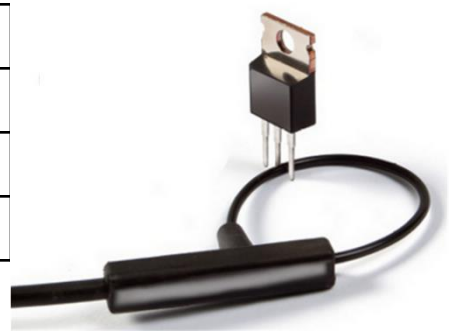


The distorted amplitude is still existed after de-skew, which will cause less accuracy in transient measured results.

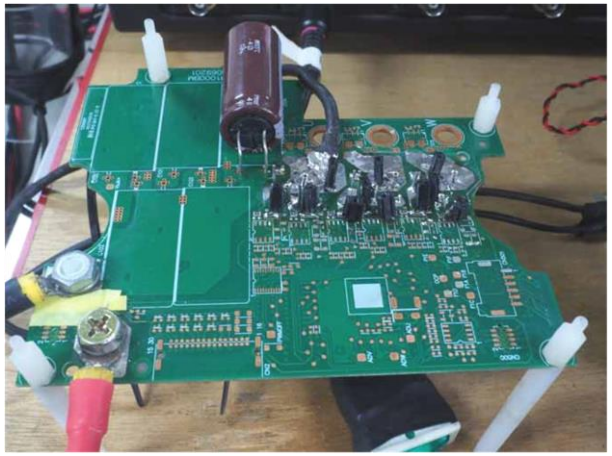
Double Pulse Tester – Current Sensor

☐ Calibration of the Rogowski probe by high BW coaxial shunt resistor

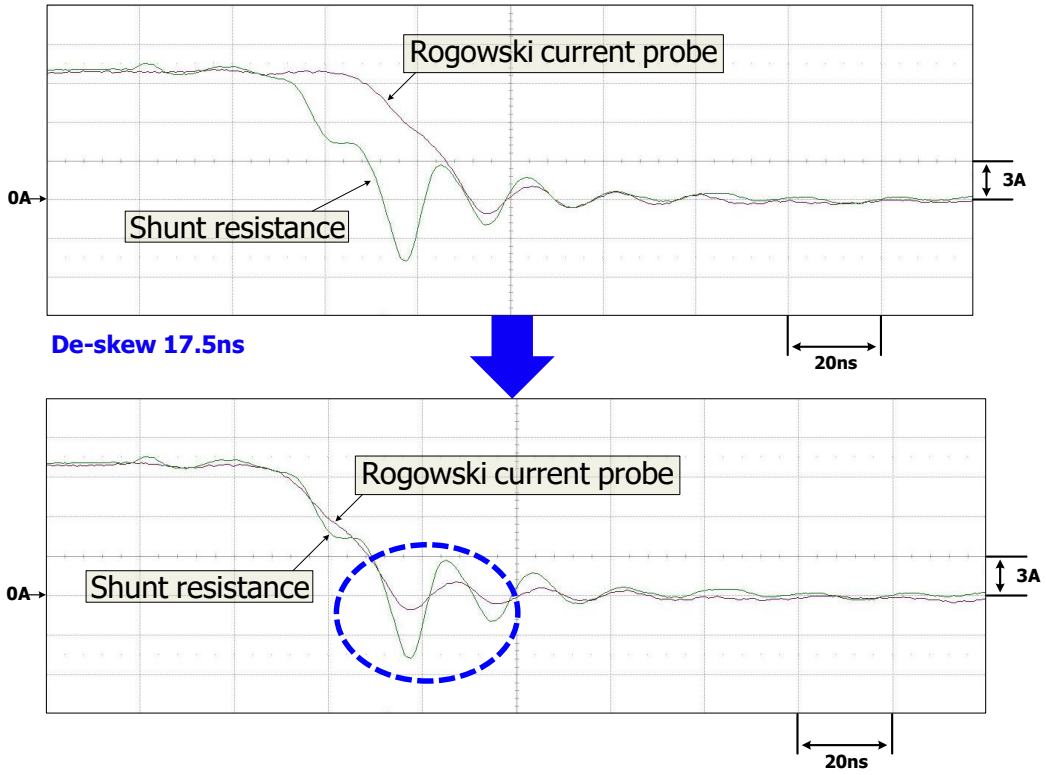
Specification	
Vdc	48V
Inductor	5.4μH
MOSFET	**IPP041N41N3(120V 120A)**



Part. No	Manufacturer	PEAK		Insulation voltage (kV)	BW -3dB(MHz)
		Current (kA)	di/dt (kA/us)		
CP9012S	Cybertek	0.12	8	1	30



The de-skew time in both rising and falling time are near the same!



Double Pulse Tester – Voltage Probe

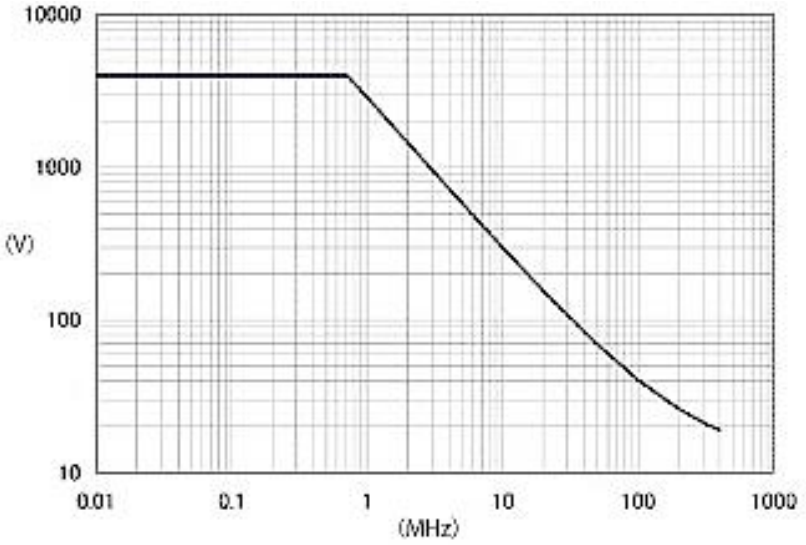
☐ Measurement equipment – high voltage probe

GaN probe

P2000A GaN Probe	
Characteristic	**Rating**
System Bandwidth	700 MHz (-3 dB) typical
Attenuation Ratio (1)	100:1 ± 2 % at DC Connected to oscilloscope with an input impedance of 1 MΩ ± 1 %.
Absolute Maximum Voltage	< 1000V $_{RMS}$
Voltage Coefficient	0.00025 %/V %/V (typical)
Probe Rise Time	500 psec (10 % - 90 %) (typical)
Maximum Rated Input Voltage (2)	As defined in IEC 61010-031. Also see definitions in User Manual.
Measurement category I:	1000 V $_{RMS}$ 4000 V transient overvoltage
Measurement category II:	1000 V $_{RMS}$ CAT II
Input Resistance (System)	50 MΩ ± 1 %
Input Capacitance (System)	7 pF (typical)
Compensation Range	10 pF - 50 pF (typical)
Input Coupling of the Measuring Instrument	1 MΩ AC / DC
Weight (probe)	82g
Cable Length	1m
Probe Tip Diameter	5mm

item	SS-0170R	SS-0171R
Input enduring voltage *Derating curve reference	CATI6,000V(DC+AC peak) CATII1,000V (DC+AC peak)	CATI4,000V(DC+AC peak) CATII1,000V (DC+AC peak)
Frequency bandwidth	DC to 400 MHz(±2 d B) *Derating curve reference	
Attenuation ratio	100:1±3.0 % 以内	

Voltage vs. frequency de-rating curve

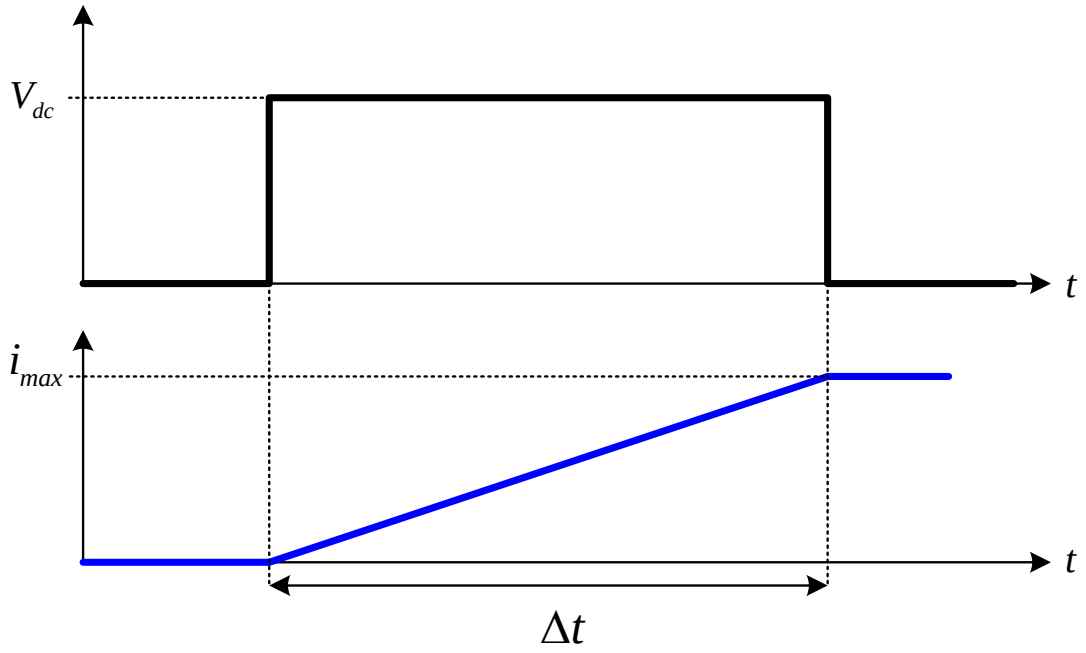


Ref. https://www.iti.iwatsu.co.jp/en/products/accessories/Voltage_probe5_e.html

Double Pulse Tester - Inductor

- Inductor – without magnetic core to provide linear characteristic

$$L = \frac{V_{dc}}{i_{max}} \Delta t$$



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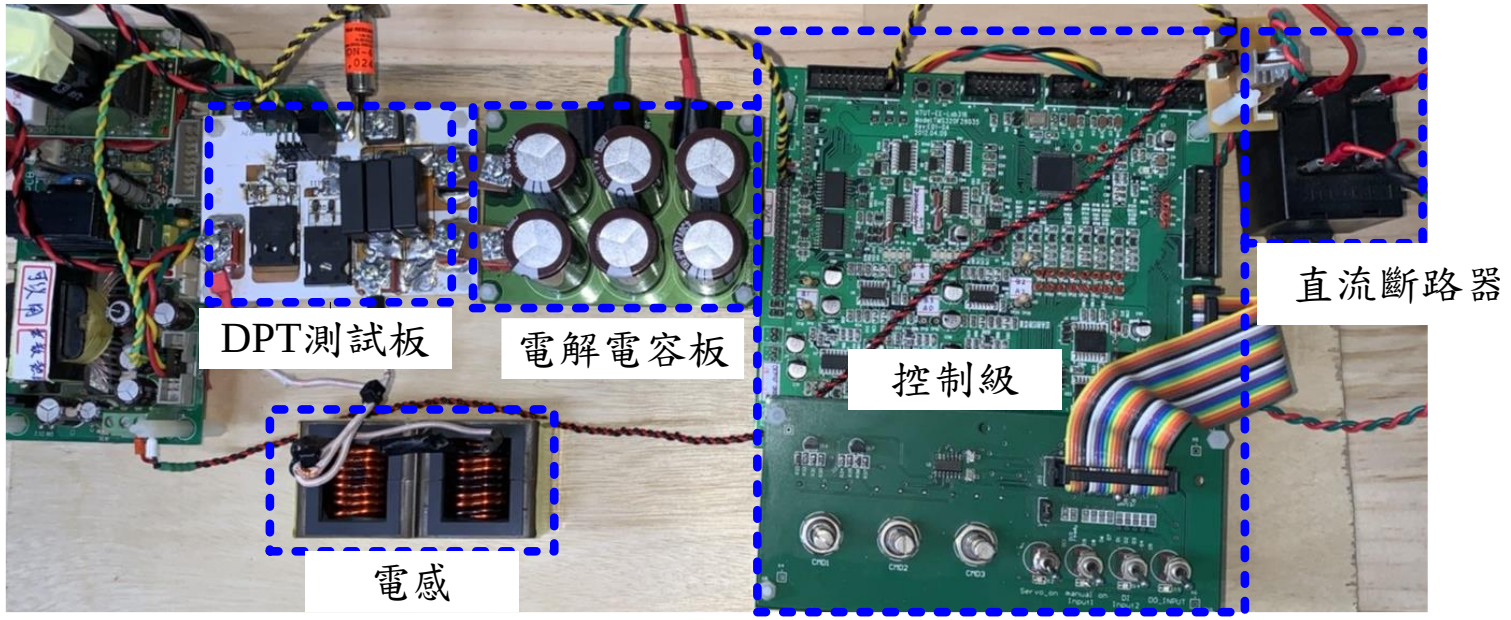
Double Pulse Tester – Test Plaform

Parameter	Specification
DC link voltage	300V
Inductor	70uH
Maximal current	40A
Gate driver UCC21520	Dual channels/ 4A source /6A sink
DUT	H1M065F050 and IKW75N60T



Compare Different Power Switches

☐ DUT- key parameters of the SiC MOSFET and IGBT

SiC MOSFET

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn On Delay Time	$t_{d(on)}$	V_{DS}=400V, V_{GS}=-4/+20V, I_D=20A, R_L=20Ω, $R_{G(ext)}$= 2.7 Ω		16		ns
Rise Time	t_r			17		
Turn Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			10		
C_{oss} Stored Energy	E_{oss}	V_{GS}=0V, V_{DS}=400V f =1MHz, V_{AC}=25mV		24		µJ
Turn-on Switching Energy	E_{on}	V_{DS}=400V, V_{GS}=0/20V, I_D=20A, $R_{G(ext)}$= 2.7 Ω		21*		
Turn-off Switching Energy	E_{off}			28*		
Internal Gate Resistance	$R_{G(int.)}$	f =1MHz, V_{AC}=25mV		1.2		Ω

*Based on the results of calculation, note that the energy loss caused by the reverse recovery of free-wheeling diode is not included in E_{on}.

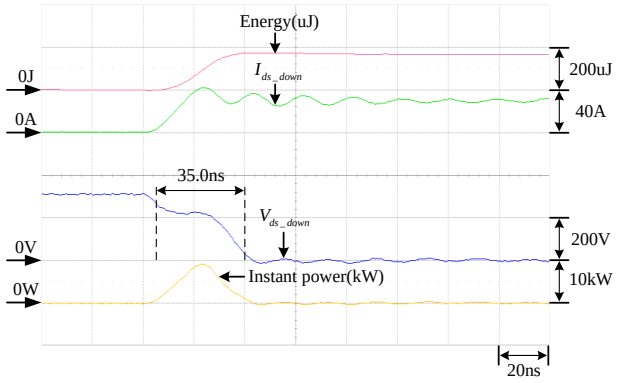
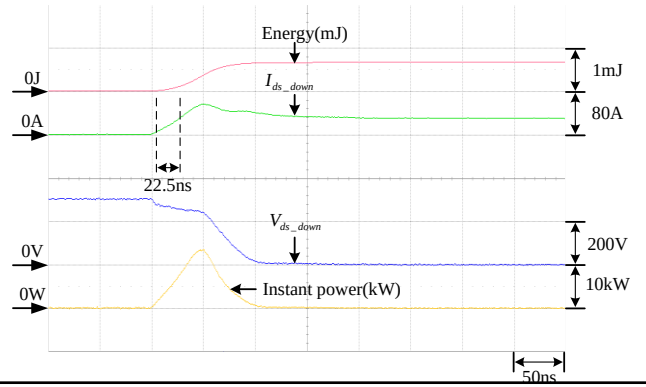
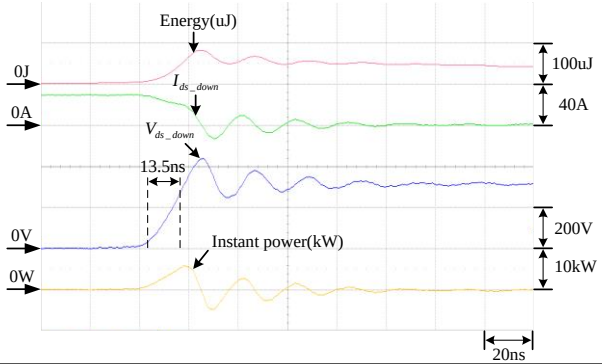
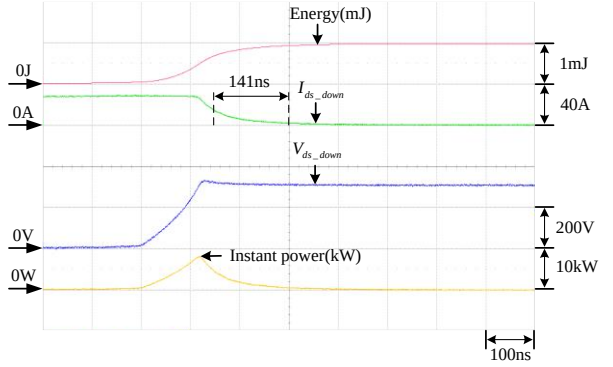
Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_{SD}=5A	3.0	V
Continuous Diode Forward Current	I_S	V_{GS}=-5V, T_C=25°C	36	A
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_{SD}=30A, V_{DS}=400V, di/dt=300A/µs	58	ns
Reverse Recovery Charge	Q_{rr}		122	nC
Peak Reverse Recovery Current	I_{rrm}		3.75	A

IGBT

Parameter	Symbol	Conditions	Value min.	Value typ.	Value max.	Unit
IGBT Characteristic						
Turn-on delay time	$t_{d(on)}$	T_j=25°C, V_{CC}=400V, I_C=75A, V_{GE}=0/15V, r_G=5Ω, L_σ=100nH, C_σ=39pF L_σ, C_σ from Fig. E Energy losses include "tail" and diode reverse recovery.	-	33	-	ns
Rise time	t_r		-	36	-	
Turn-off delay time	$t_{d(off)}$		-	330	-	
Fall time	t_f		-	35	-	
Turn-on energy	E_{on}		-	2.0	-	mJ
Turn-off energy	E_{off}		-	2.5	-	
Total switching energy	E_{ts}		-	4.5	-	
Anti-Parallel Diode Characteristic						
Diode reverse recovery time	t_{rr}	T_j=25°C, V_R=400V, I_F=75A, di_F/dt=1460A/µs	-	121	-	ns
Diode reverse recovery charge	Q_{rr}		-	2.4	-	µC
Diode peak reverse recovery current	I_{rrm}		-	38.5	-	A
Diode peak rate of fall of reverse recovery current during t_b	di_{rr}/dt		-	921	-	A/µs

Compare Different Power Switches

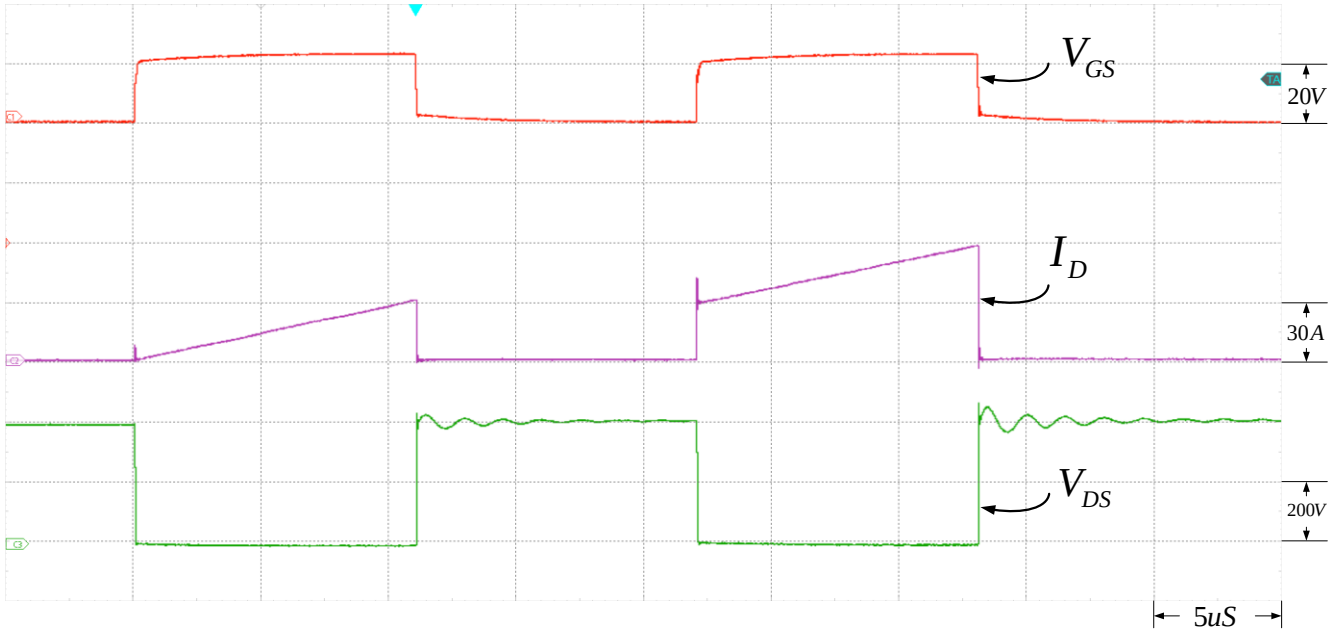
☐ Switching loss comparison (V_{dc}=300V，R_g=5Ω)

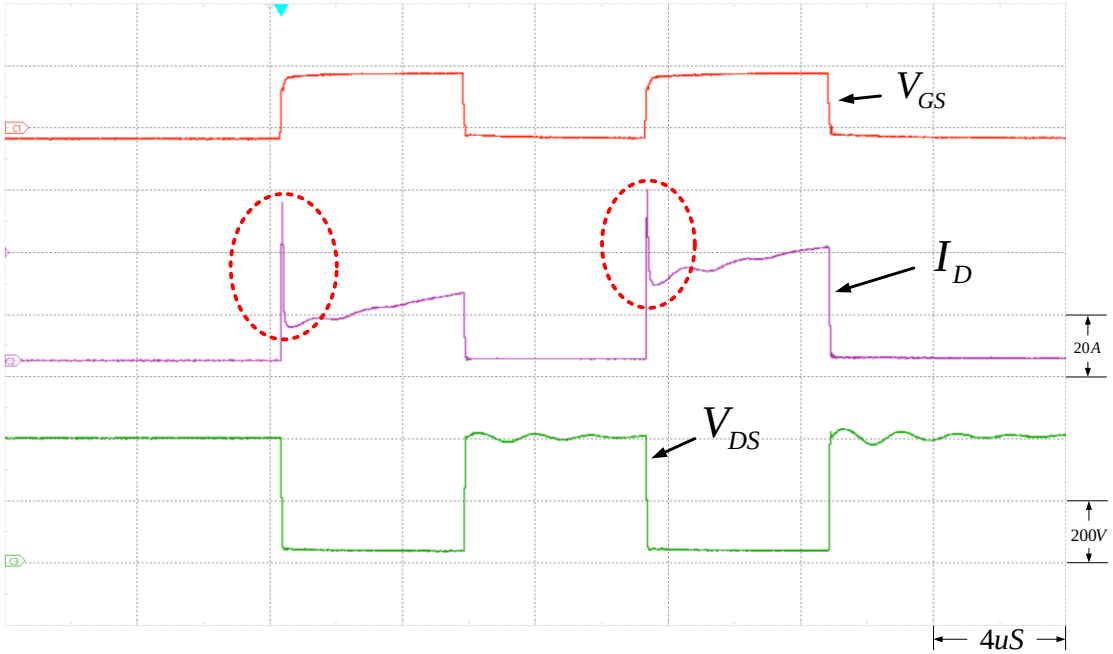
	SiC MOSFET	IGBT
Turn on		
Turn off		

Switching loss of the SiC MOSFET and IGBT are 253.2μJ and 1597.0μJ, respectively.

Miller Effect

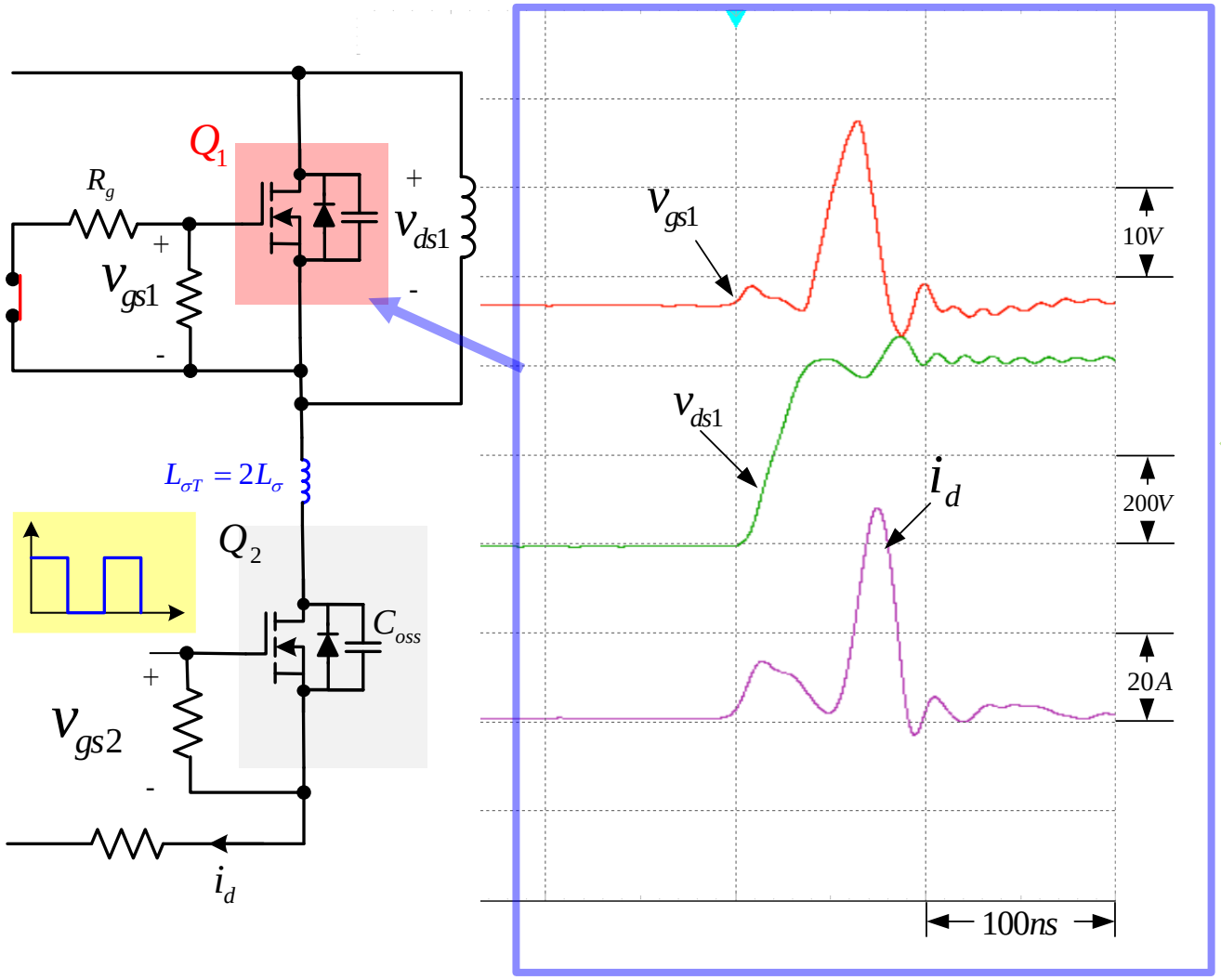
☐ Larger current spike at turn-on transient

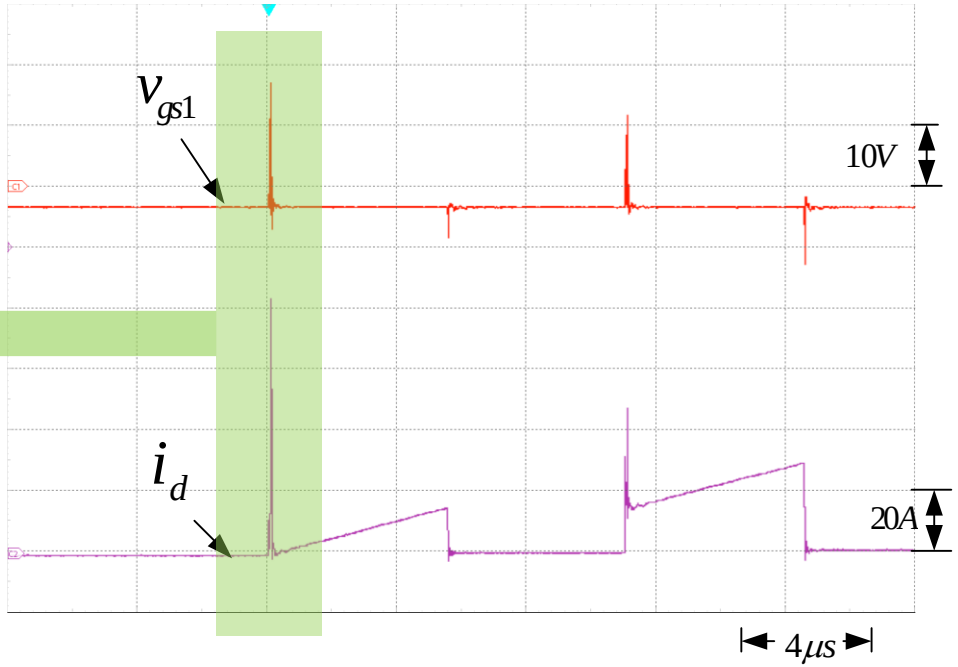




Miller Effect

☐Miller effect at turn on transient (Q2 OFF ->ON and Q1 OFF)



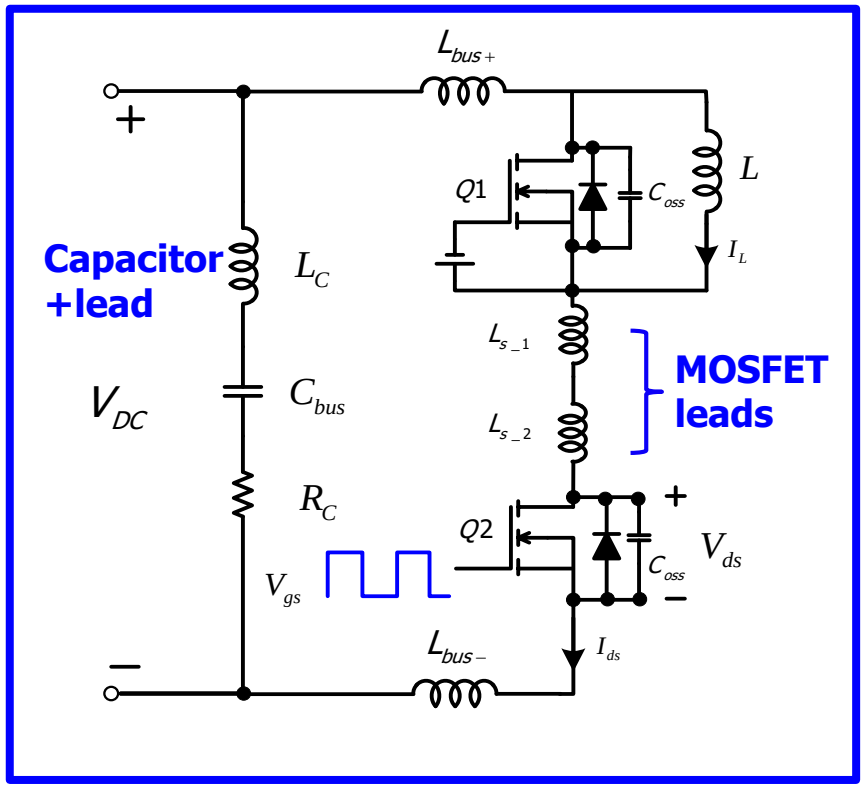


Outline

- ☐ Introduction
- ☐ Key Components
- ☐ DPT in Power Switch Applications
- ☐ **DPT in Power Stage Design and Verifications**
- ☐ DPT Demo

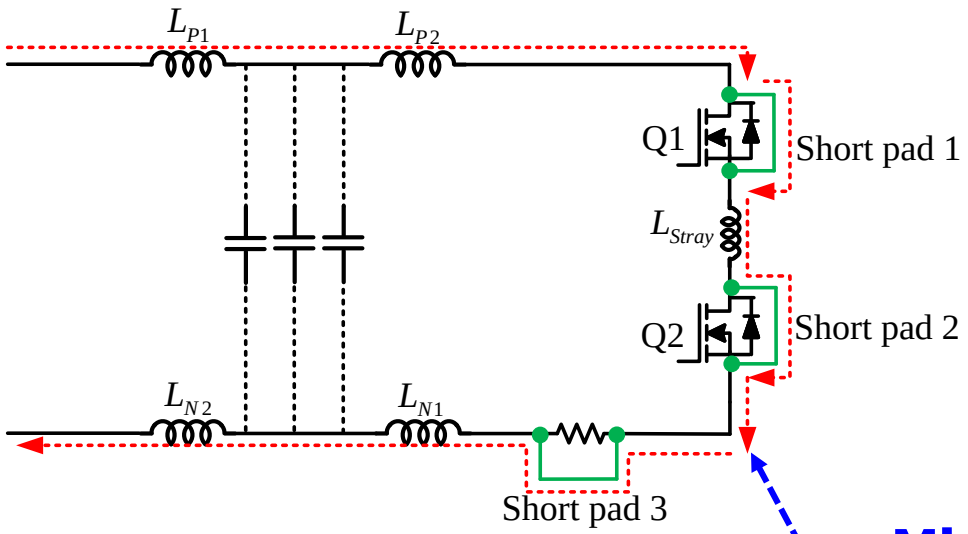
The Influence of Stray Inductance on Power Stage Design

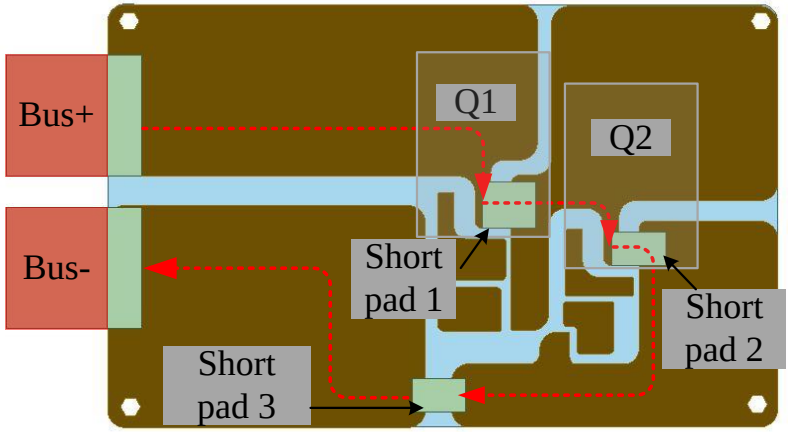
- Stray inductance may exist in power traces of PCB, leads of power switches (module), capacitor
- The stray inductance may induce voltage stress at turn-off transient, EMI , and imbalanced current sharing among paralleled power switches.



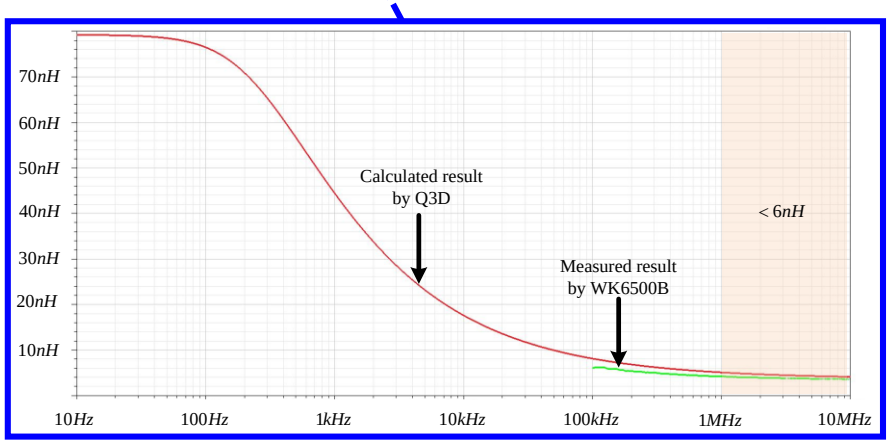
The Influence of Stray Inductance on Power Stage Design

- Extract and reduce stray inductance of main power flow path by Ansys Q3D in PCB design stage and use DPT to verify the design.





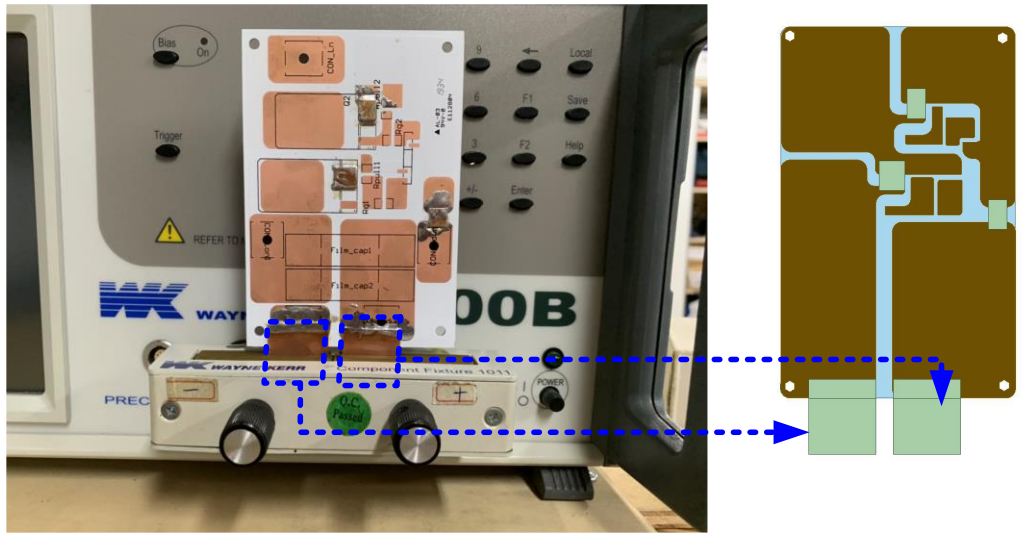
Minimize the stray inductance by Q3D to reduce turn-off voltage spike



Verify PCB Design

☐Stray inductance measurement by impedance analyzer (WK 6500B)

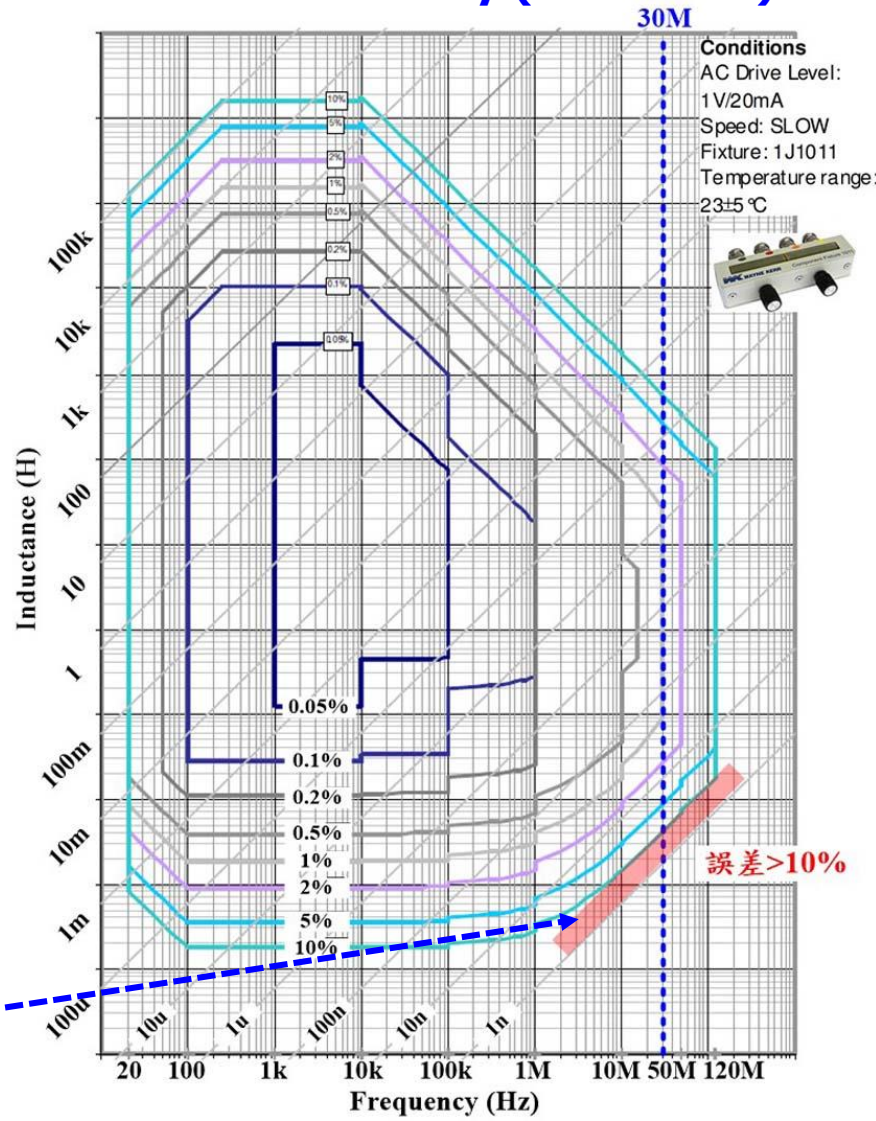
Valid method only for specified PCB shape



	1MHz	10MHz
Calculated inductance by Q3D(nH)	5.17	4.21
Measured inductance by WK 6500B(nH)	4.18	3.67
Error	23.68%	14.71%

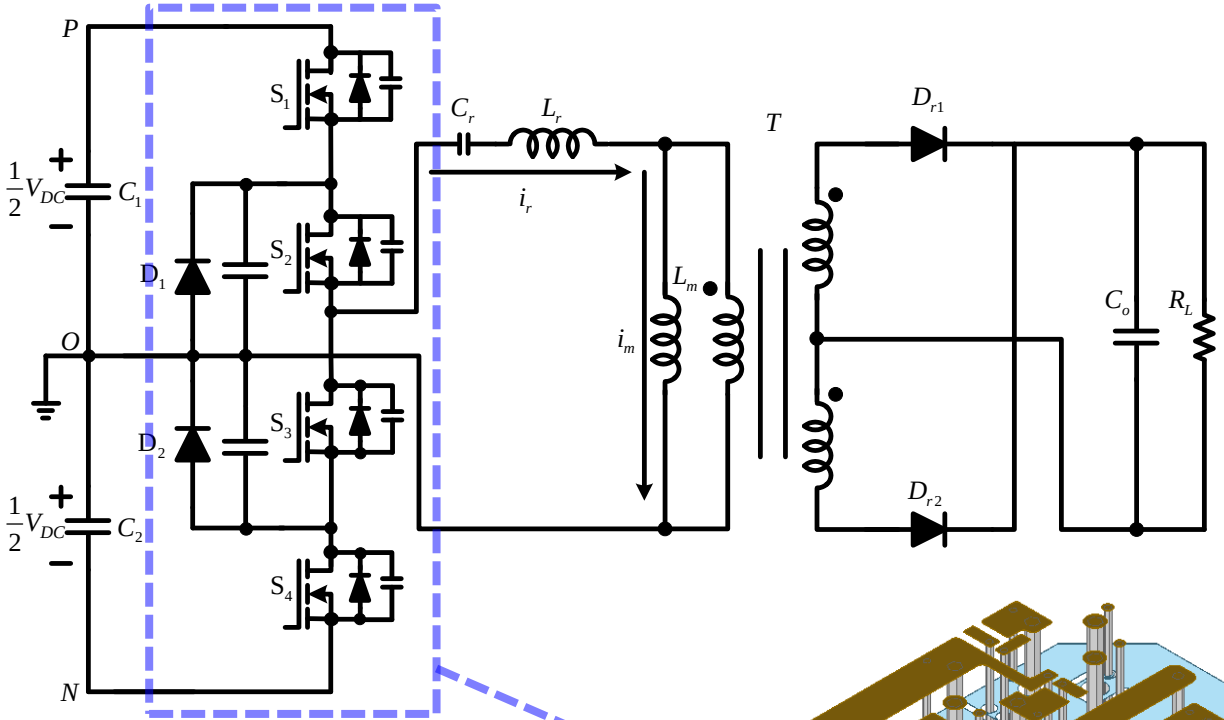
The measured error may be induced by the WK 6500B.

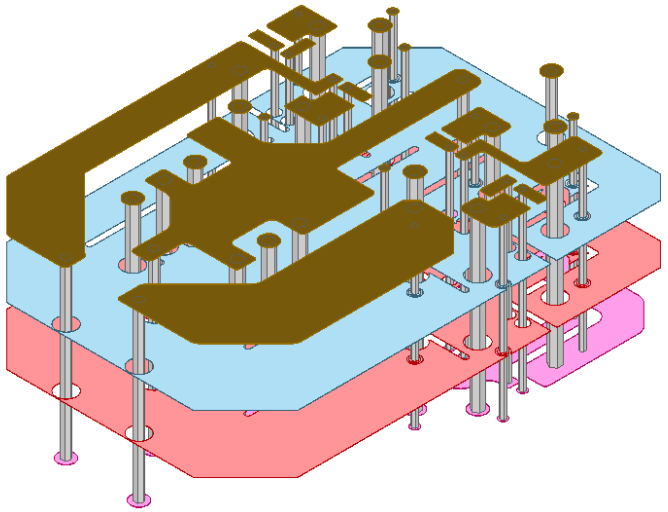
Measured accuracy (WK 6500B)

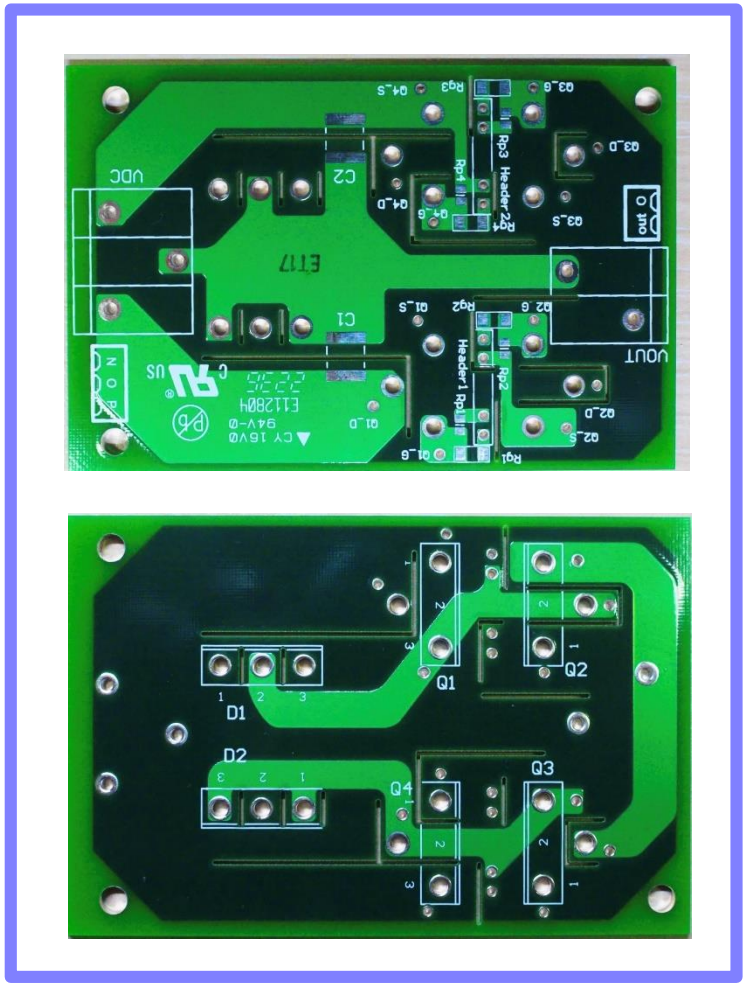


Verify PCB Design

☐Three level LLC with SiC MOSFET (TO 247)

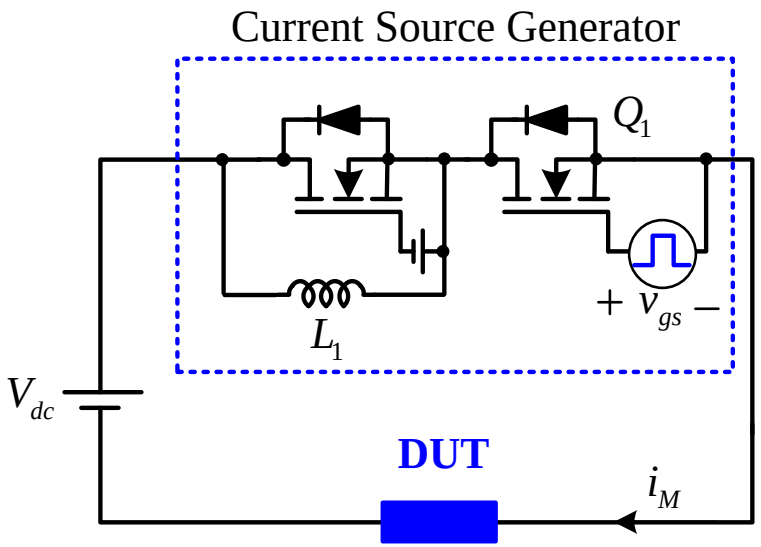


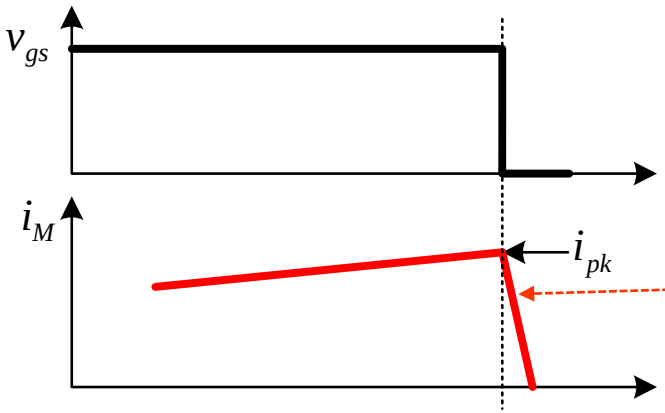


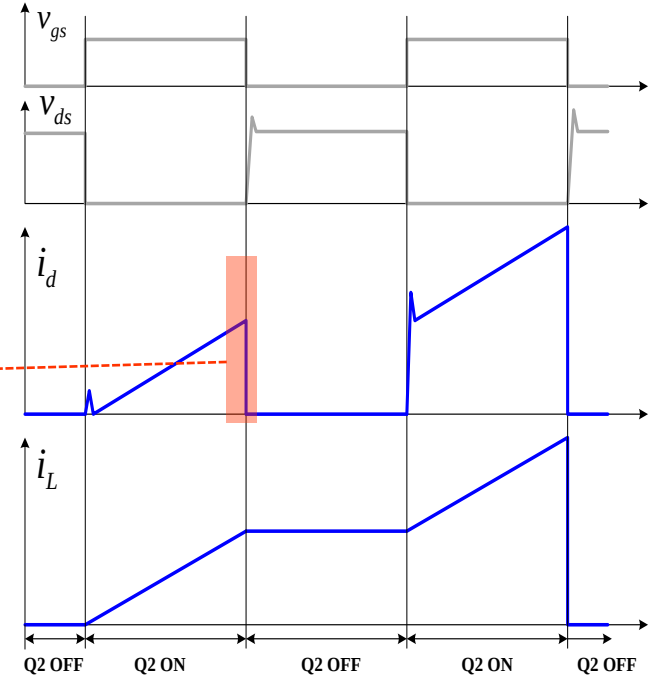


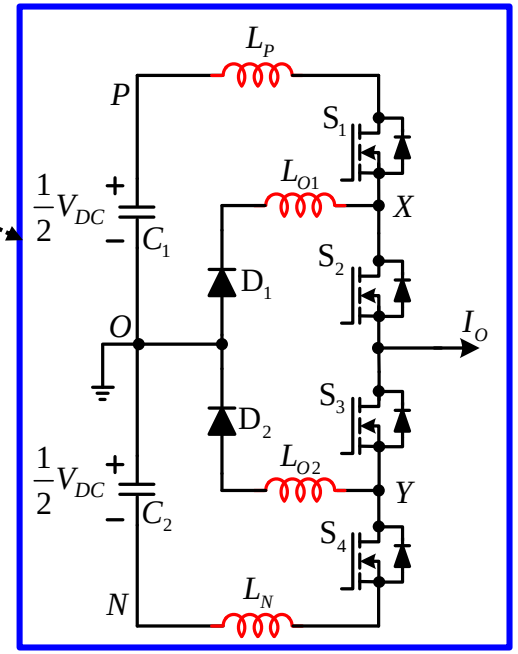
Verify PCB Design

☐Three level LLC with SiC MOSFET (TO 247)



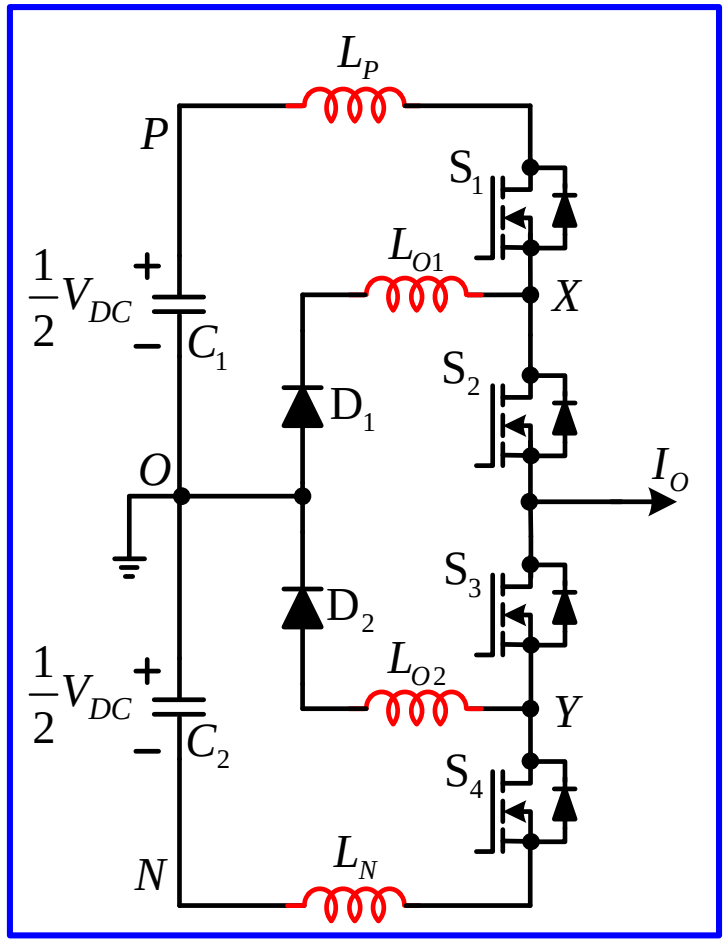


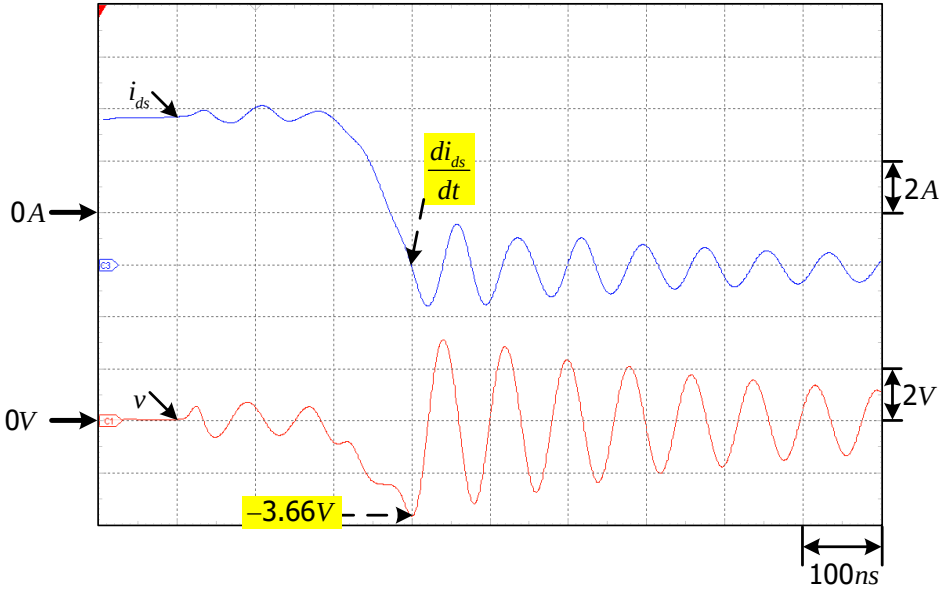




Verify PCB Design

☐Three level LLC with SiC MOSFET (TO 247)

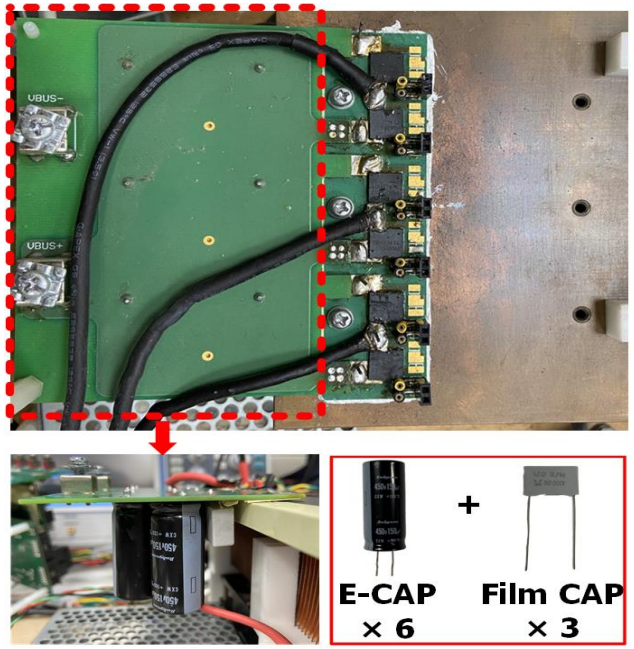


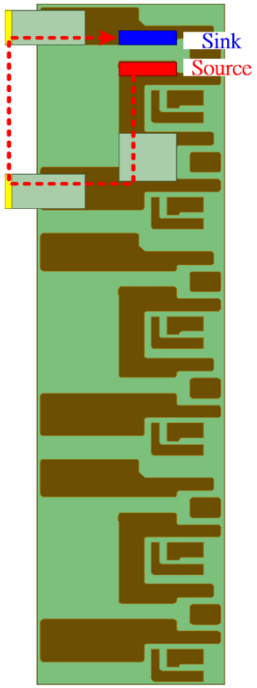


	L_P	L_{O1}	L_{O2}	L_N
Q3D	11.1nH	22.4nH	18nH	8.9nH
DPT	10.2nH	20.4nH	16.6nH	9.5nH
Error	7.8%	8.9%	7.6%	6.7%

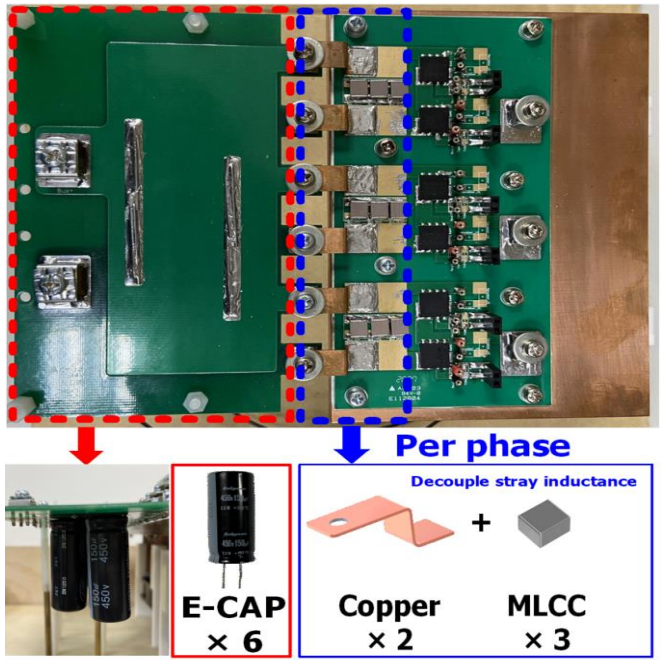
Investigate the Effect of MLCC in GaN-Based Power Stage

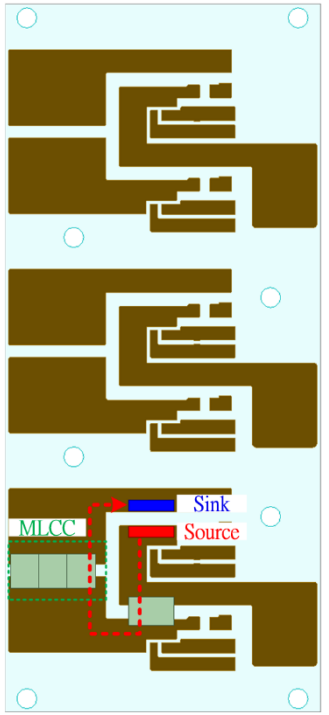
☐ Power PCB layout





Initial design





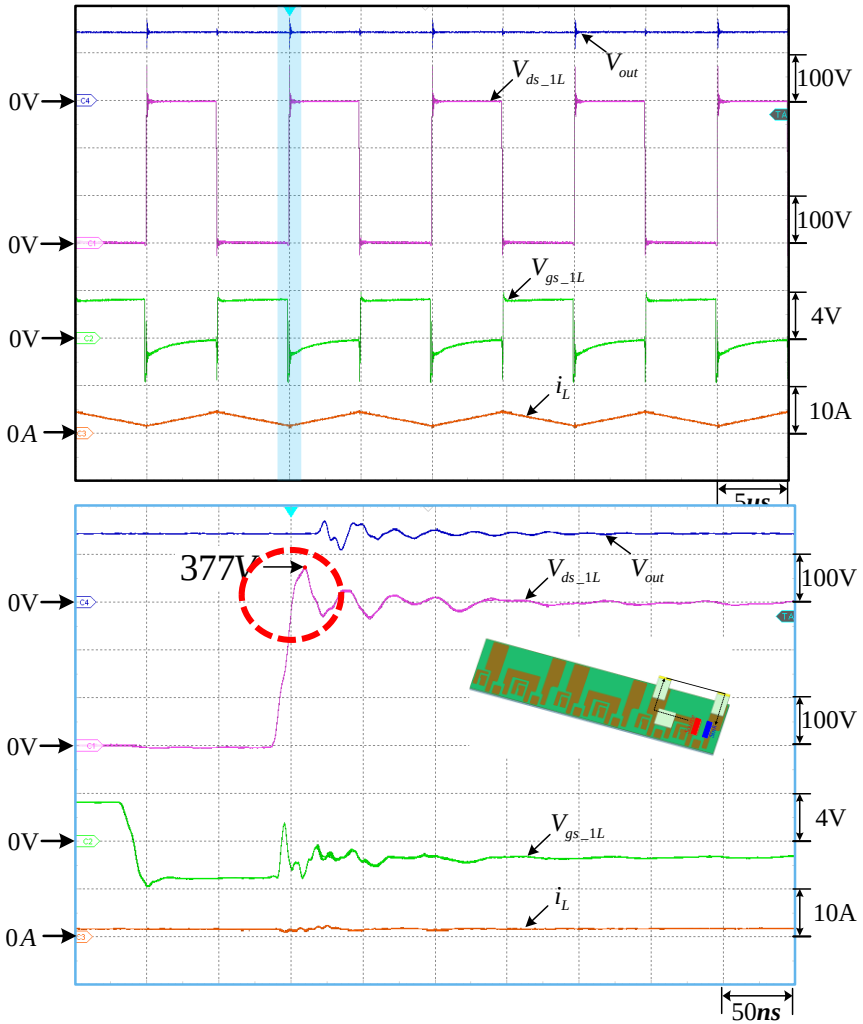
Modified design

	Stray inductance (@30MHz)
Initial design	6.38nH
Modified design	1.34nH

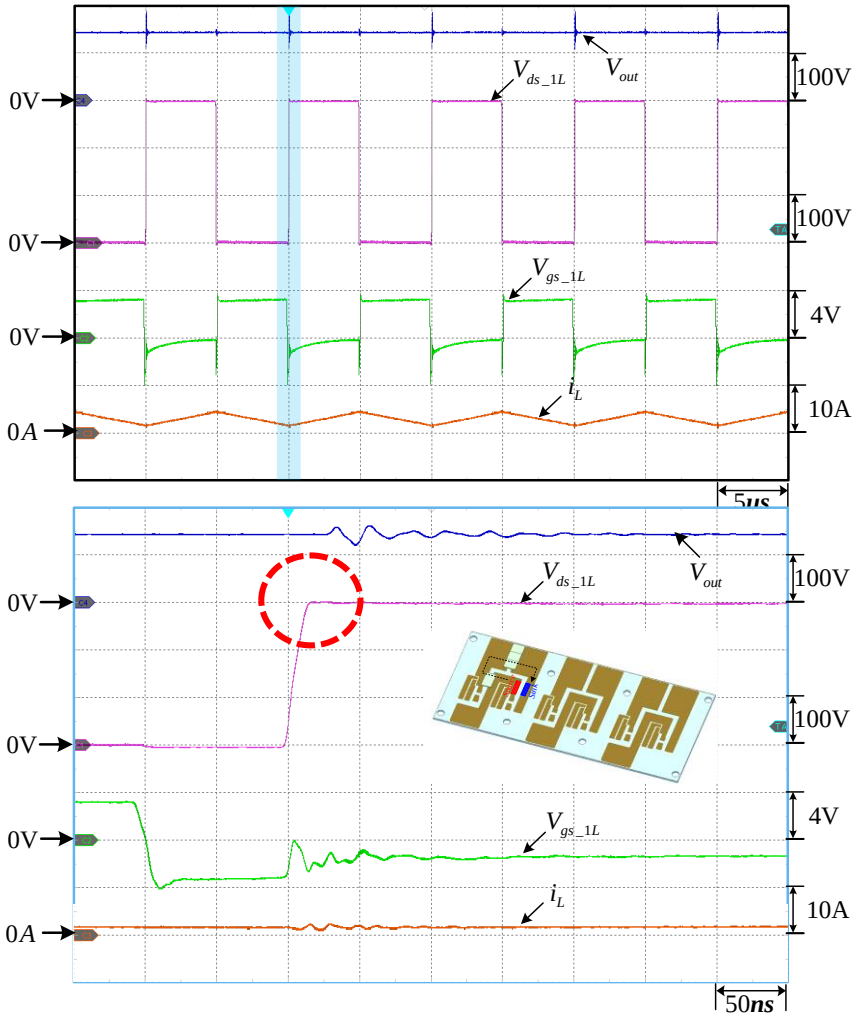
Investigate the Effect of MLCC in GaN-Based Power Stage

☐ Turn-off transient spike voltage measurement

Initial design



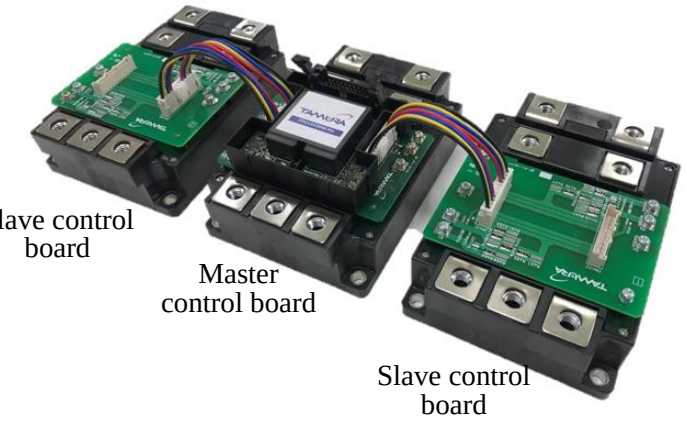
Modified design

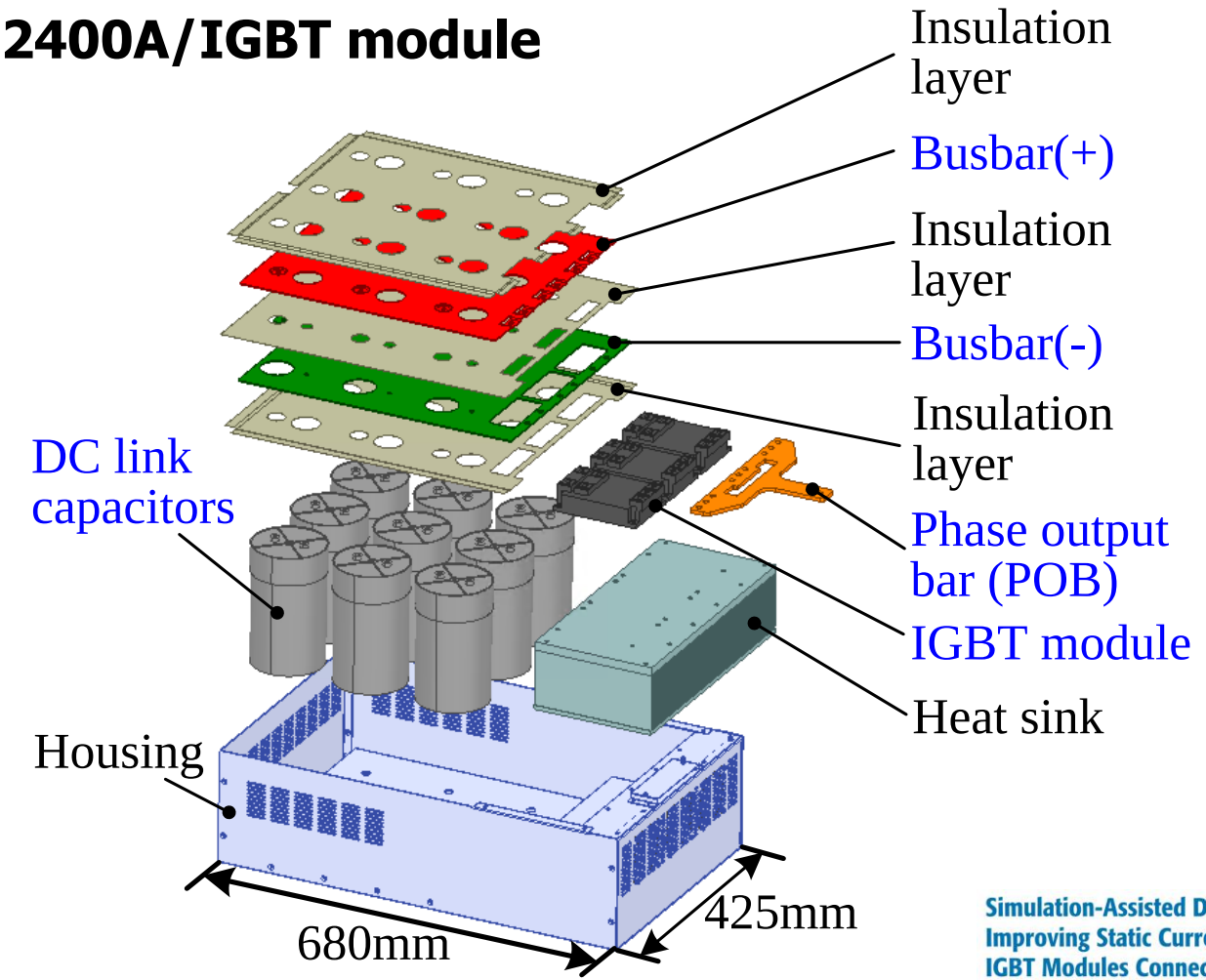


Current Sharing Among Paralleled IGBTs

☐Power stack design with three paralleled IGBTs

- ✓ **DC link voltage: 1000V**
- ✓ **Maximum current: 7200A/phase, 2400A/IGBT module**





Simulation-Assisted Design of a Power Stack for Improving Static Current Sharing Among Three IGBT Modules Connected in Parallel

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[1]Department of Electrical Engineering, National Taipei University of Technology, Taipei 106, Taiwan
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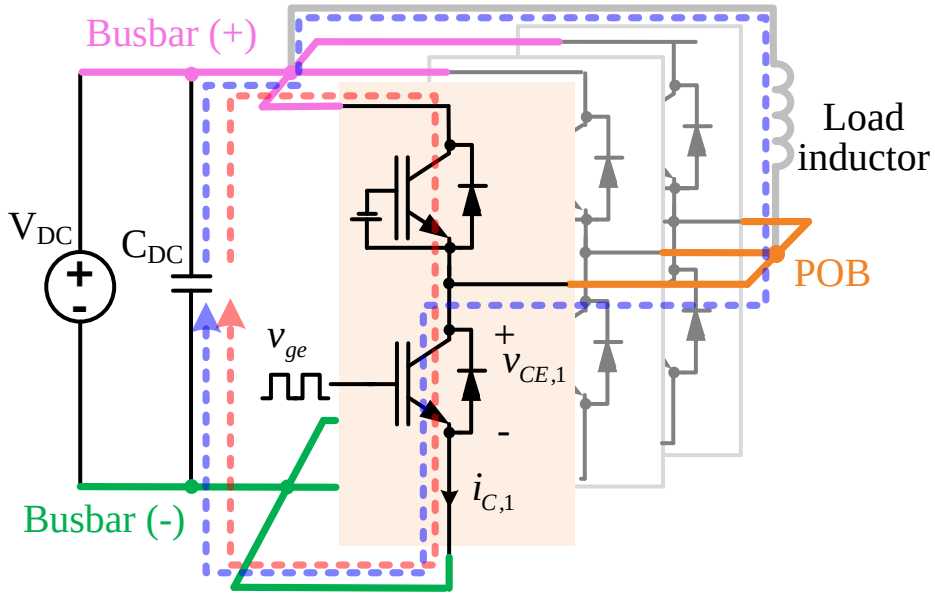
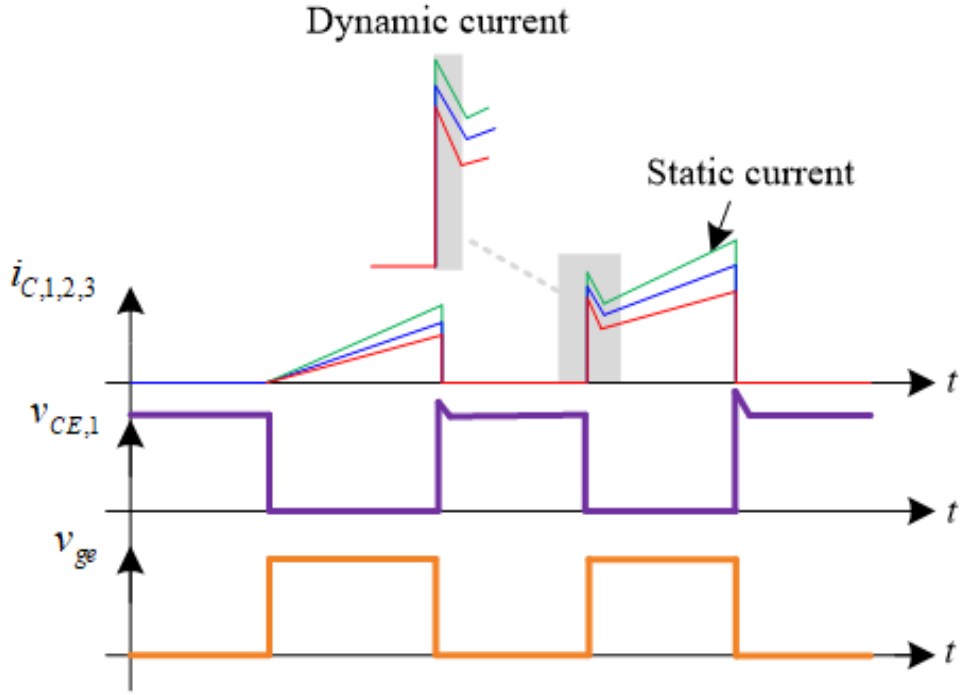
Corresponding author: Zheng-Feng Li (u94102@gmail.com)

Current Sharing Among Paralleled IGBTs

☐The influence factors of balanced current sharing





Influence factors	Dynamic (Internal circulation)	Static (To load)
Characteristic of power module	○	○
Gate driver	○	○
DC link busbar	○	○
Phase output bar (POB)	×	○

Improving static current sharing

↓

Parameter extraction of IGBT module

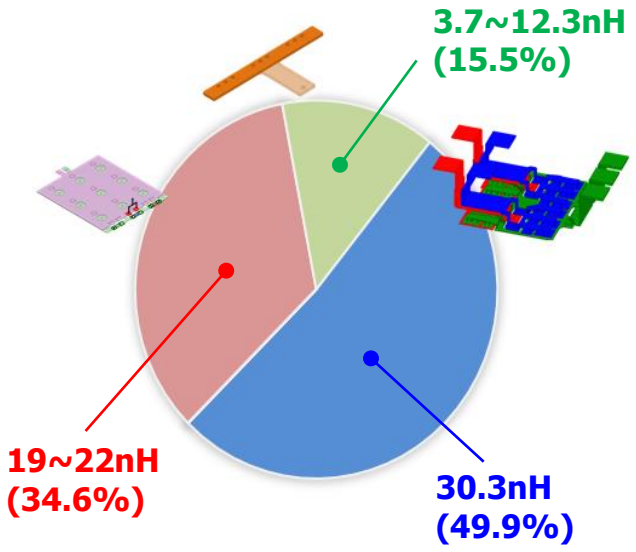
↓

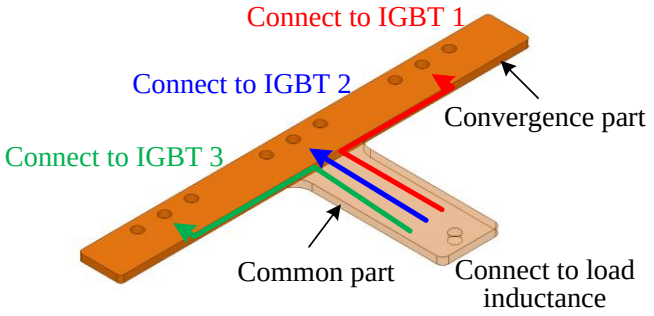
Design POB, DC link busbar

Current Sharing Among Paralleled IGBTs

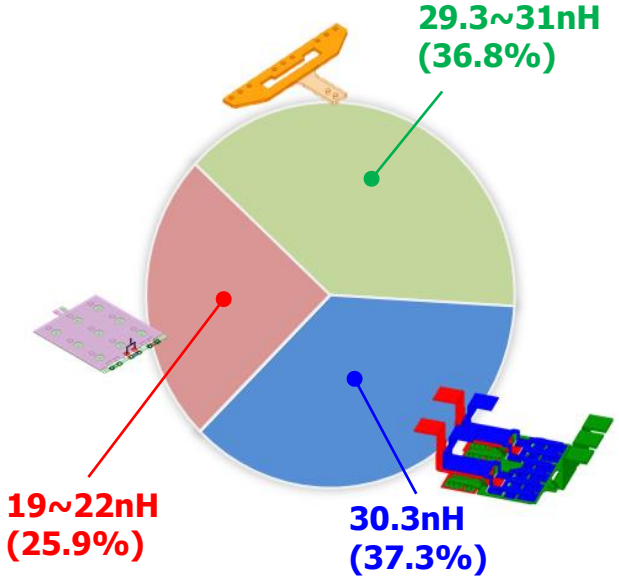
☐Stray inductance distribution

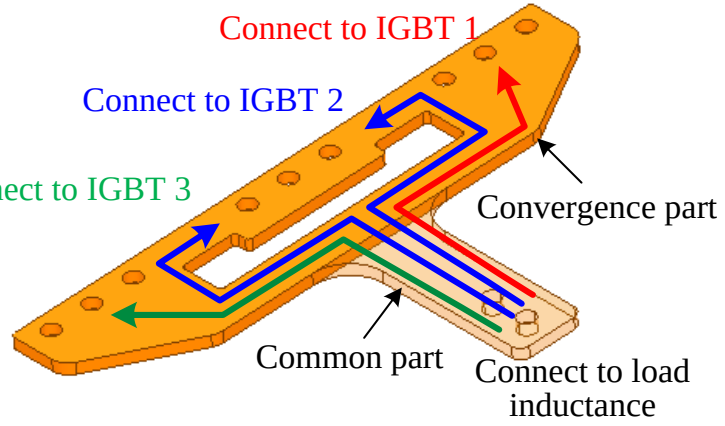
■ Initial design

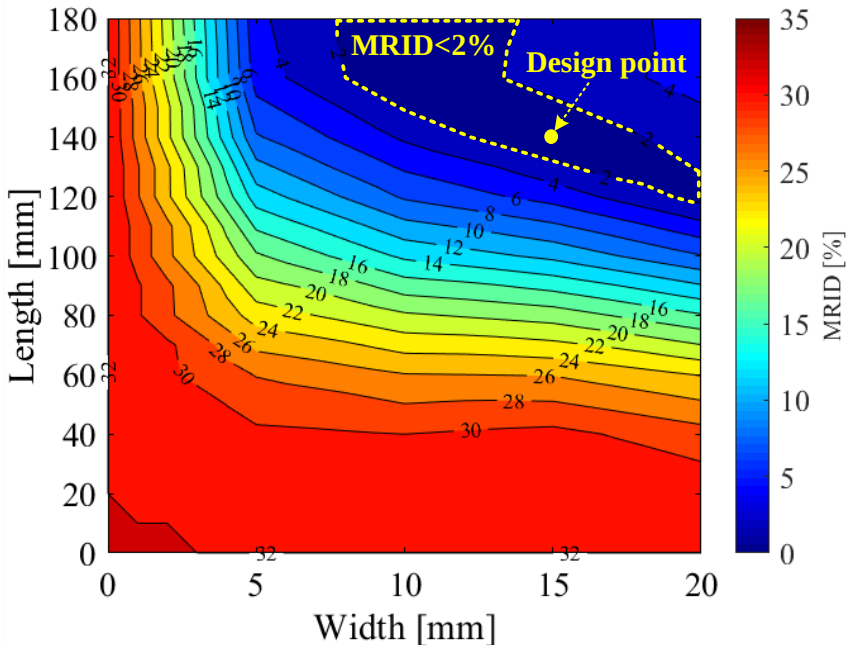




■ Proposed design







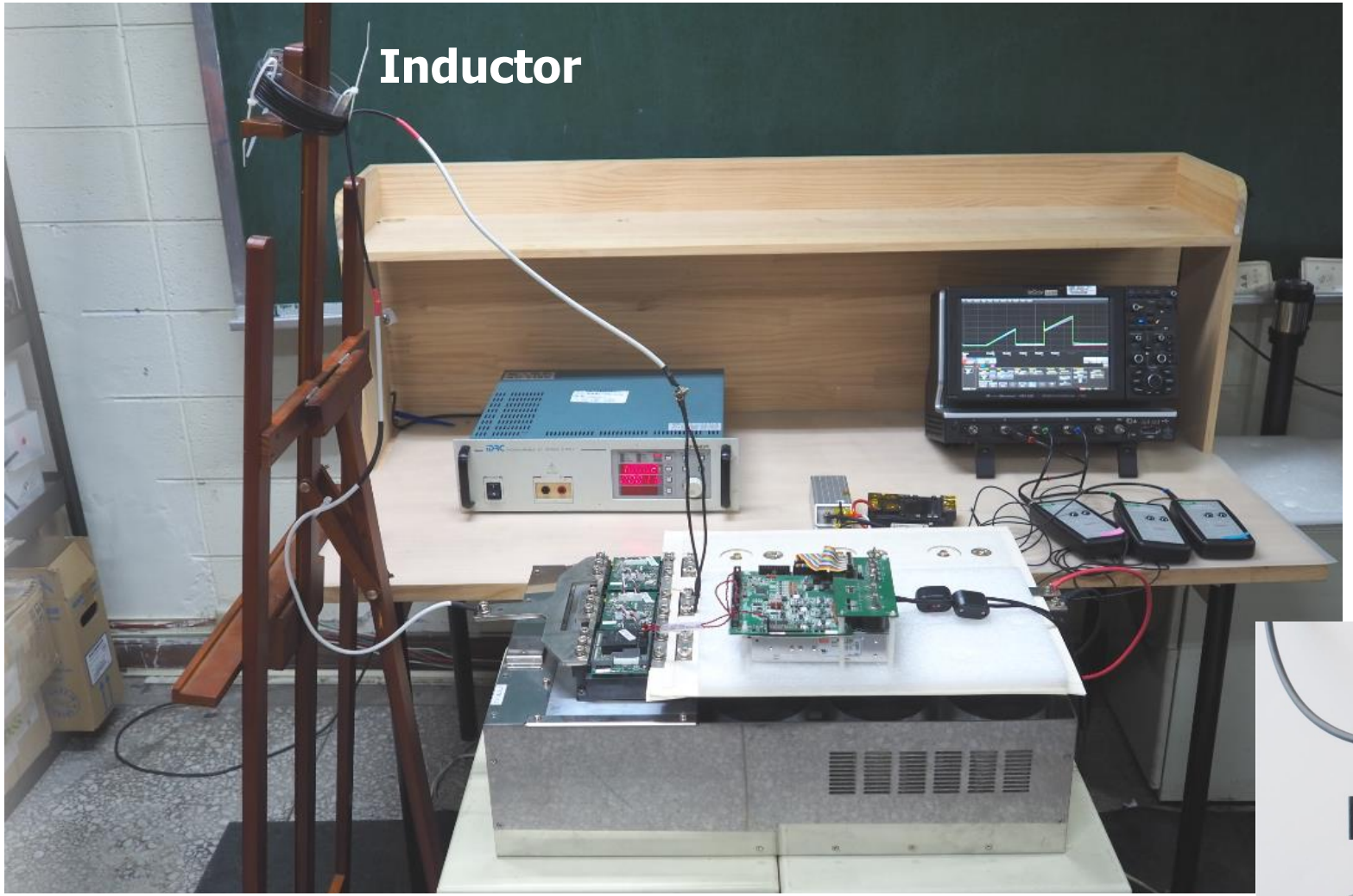
MRID: The maximum ratio of inductance difference

$$MRID(\%) = \frac{\left|L_{POBC,1} - L_{POBC,2}\right|}{L_{POBC(Avg.)}} \times 100$$

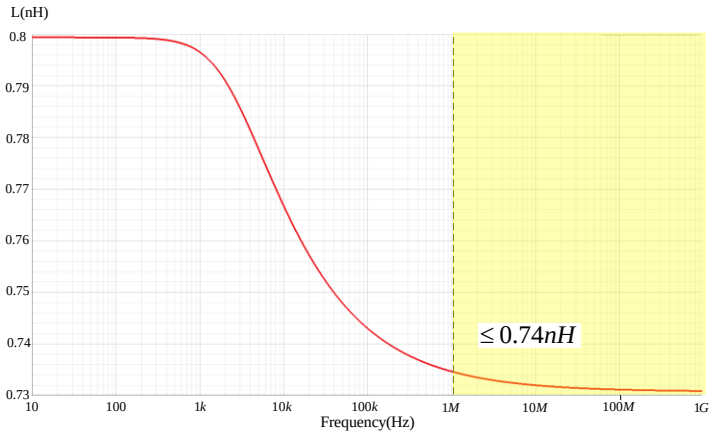
$$L_{POBC(Avg.)} = \frac{\sum_{k=1}^{3} L_{POBC,k}}{3}$$

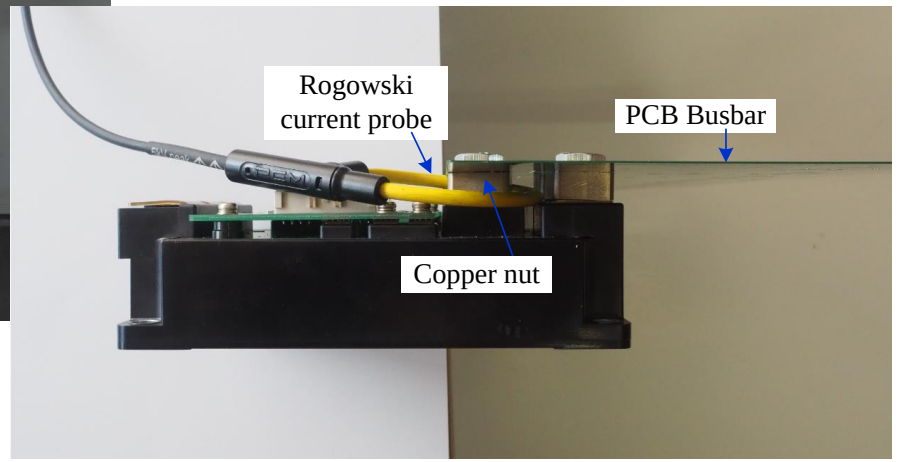
Current Sharing Among Paralleled IGBTs

☐Test Setup



Inductance of the copper nut



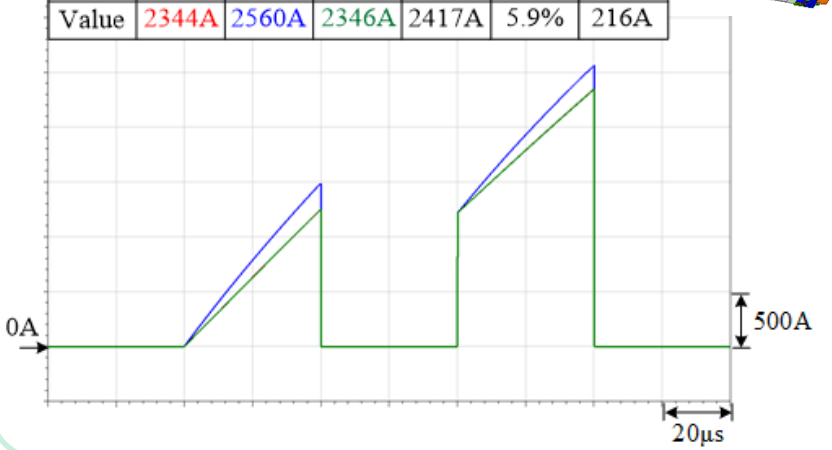


Current Sharing Among Paralleled IGBTs

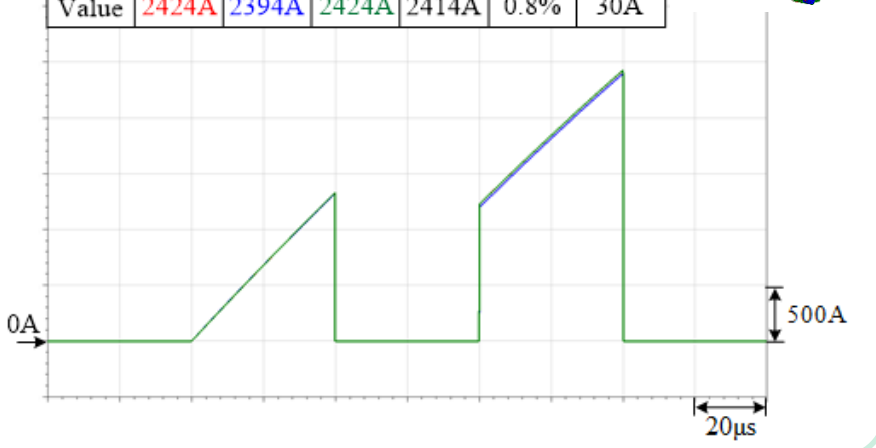
☐Co-simulation and measured results

Co-simulation

	$i_{peak,1}$	$i_{peak,2}$	$i_{peak,3}$	$i_{peak(Avg.)}$	MRIC	MCD
Value	2344A	2560A	2346A	2417A	5.9%	216A

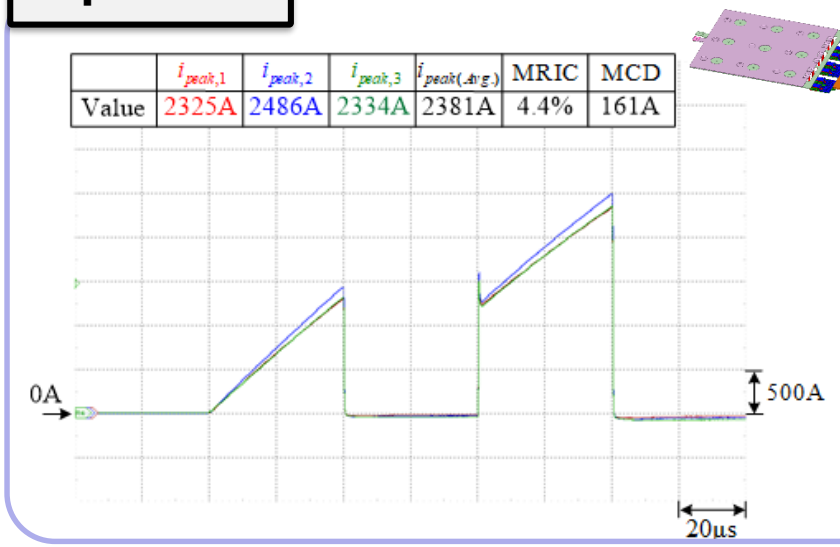


	$i_{peak,1}$	$i_{peak,2}$	$i_{peak,3}$	$i_{peak(Avg.)}$	MRIC	MCD
Value	2424A	2394A	2424A	2414A	0.8%	30A

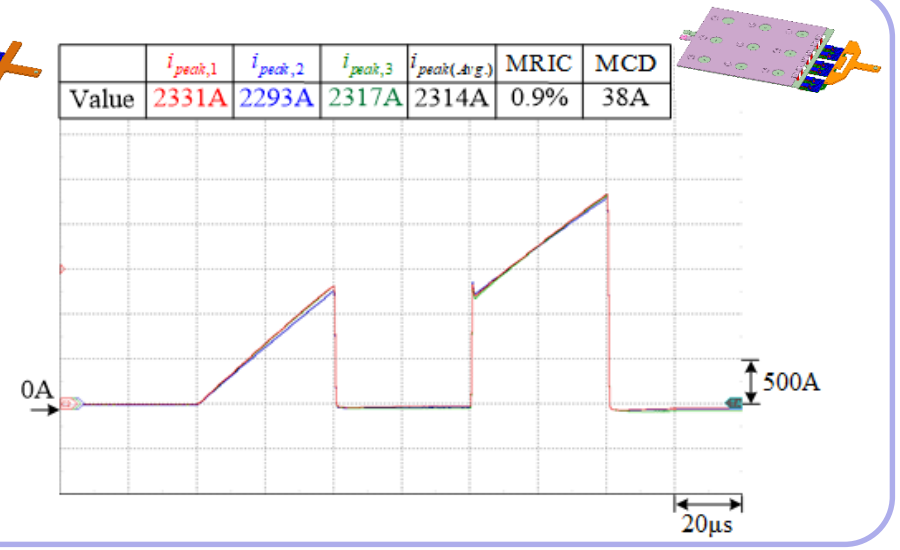


Experiment

	$i_{peak,1}$	$i_{peak,2}$	$i_{peak,3}$	$i_{peak(Avg.)}$	MRIC	MCD
Value	2325A	2486A	2334A	2381A	4.4%	161A



	$i_{peak,1}$	$i_{peak,2}$	$i_{peak,3}$	$i_{peak(Avg.)}$	MRIC	MCD
Value	2331A	2293A	2317A	2314A	0.9%	38A



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Q and A