# 車聯網時代之車載通訊的蛻變與挑戰

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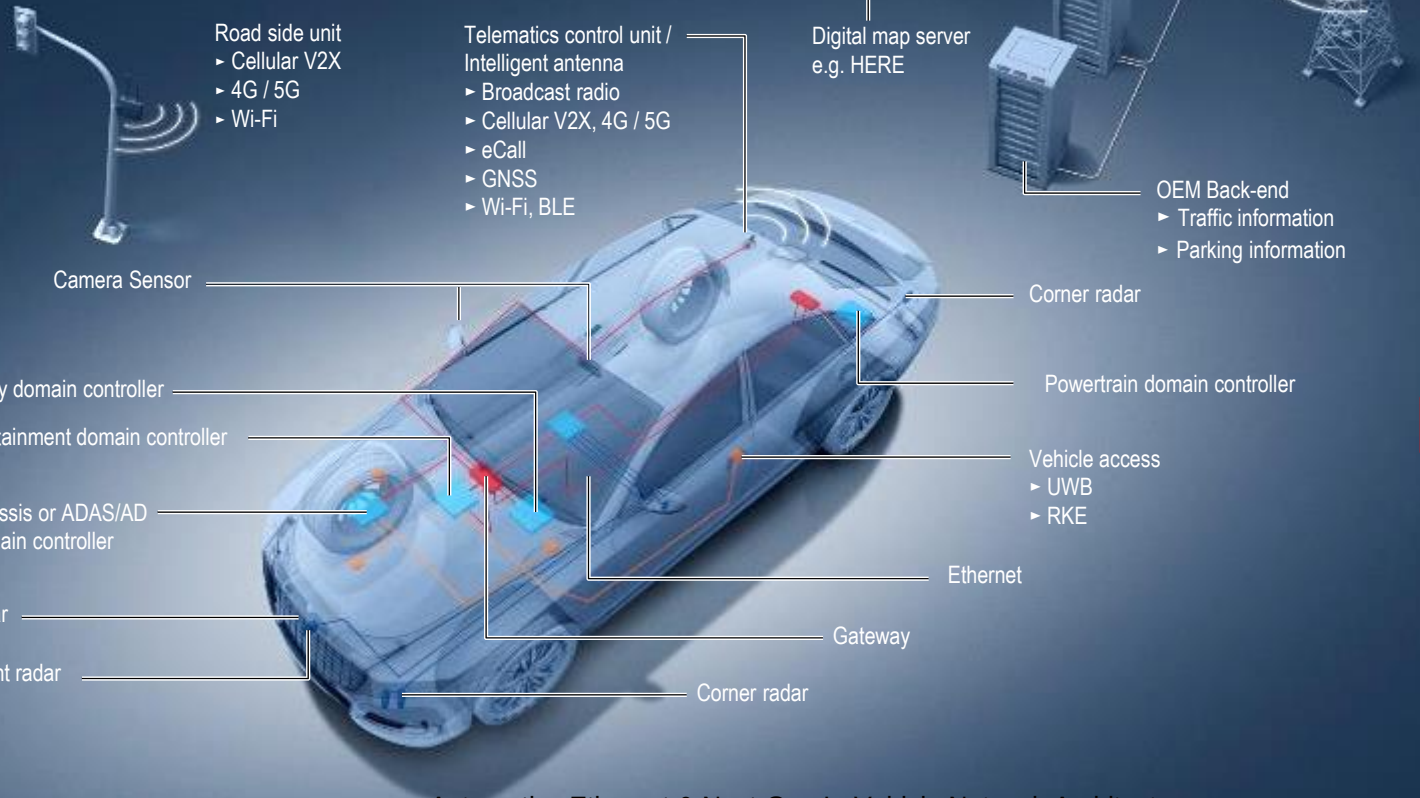
Application Engineer

ROHDE&SCHWARZ
Make ideas real

# AGENDA

- Automotive In-Vehicle Network trends
- Introduce to Automotive Ethernet
- Automotive Ethernet Test Requirement
  - Compliance Test
  - Automotive bus protocol Decode
- CAN/LIN Bus
- Summary

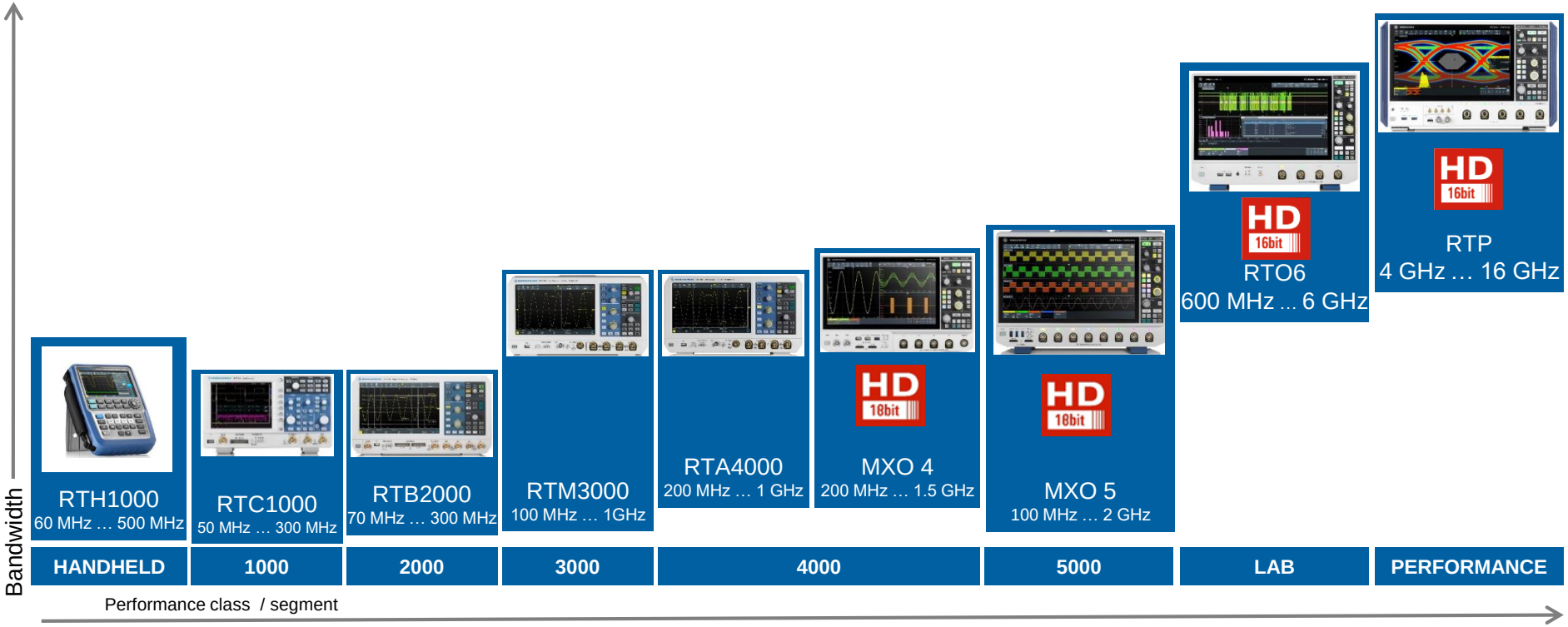
# VEHICLE ARCHITECTURE WITH HIGH PERFORMANCE COMPUTERS



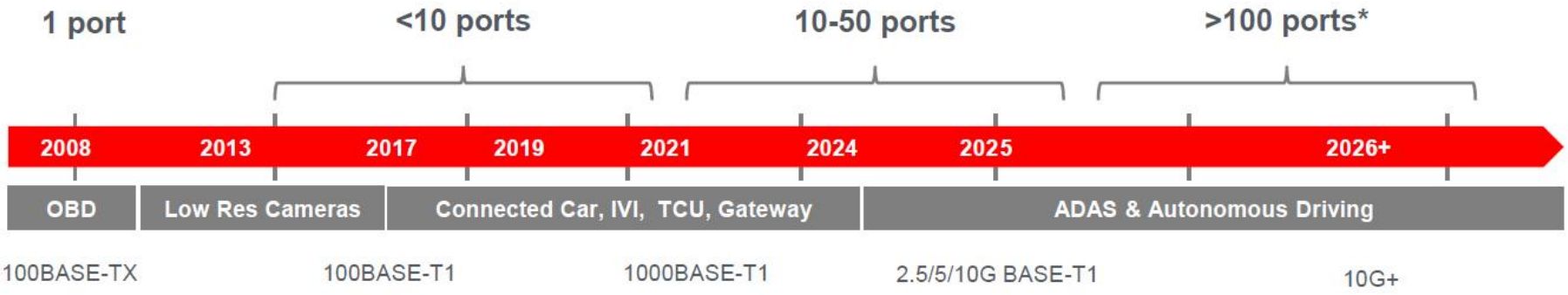

## Automotive Test Solutions

- Radar
- Connectivity
- 4G / 5G Network; Quality Analysis
- Infotainment
- In-Vehicle Networks (AUT Ethernet)
- ECU & Domain Controller Testing
- Battery Management Systems
- EMC / Full Vehicle Antenna Testing
- Storage Solutions & Cybersecurity

# MOST MODERN SCOPE LINE FROM 50 MHZ TO 16 GHZ



# Trends in Automotive Ethernet

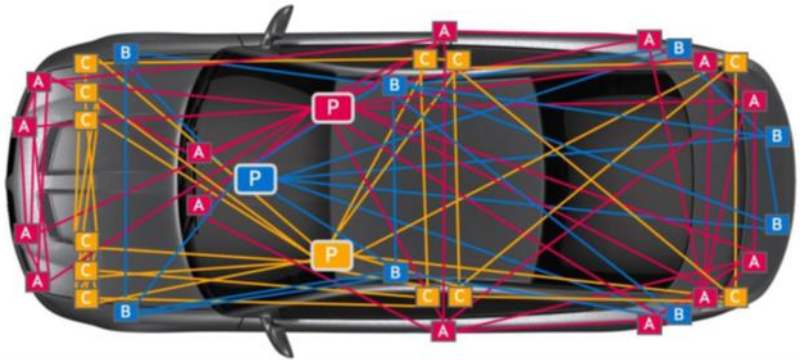



*average Ethernet ports per vehicle
** Photo courtesy of Marvell Technology Group

# TRANSITION FROM DOMAIN TO ZONAL ARCHITECTURE

## Domain architecture

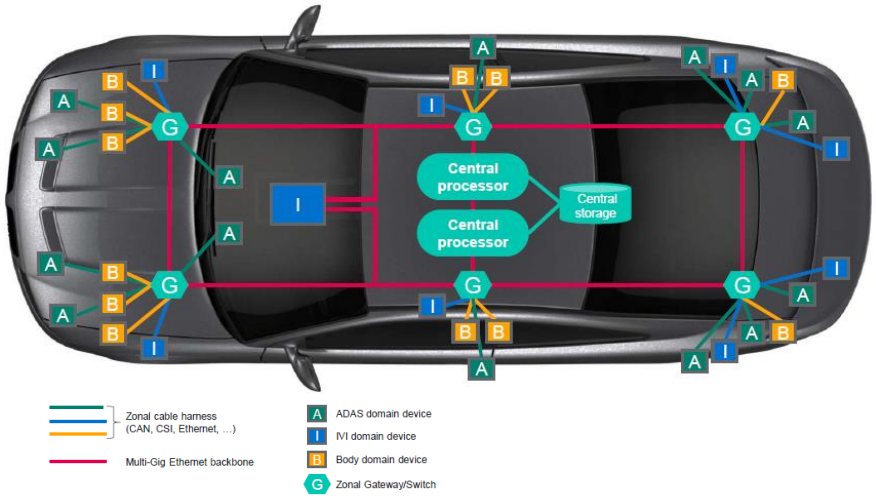
- Central domain controller/high performance computer
- Ability to handle more complex functions
- Consolidation of functions (cost optimization)
- But: cable harness is rigid and expensive




Source: Marvell Automotive Ethernet Congress 2022

## Zonal architecture

- Local ethernet gateway per zone
- Ultra high-speed secured backbone between zones
- Centralized SW
- Central computing & storage



# FUTURE AUTOMOTIVE ETHERNET STANDARDS

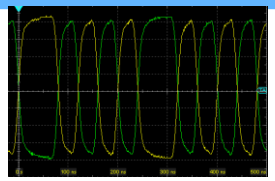
## 10BASE-T1S

IEEE 802.3cg

Multidrop
PoDL

OA TC6 & TC14

Coding NRZ

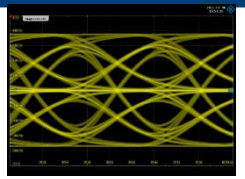


## 100BASE-T1

IEEE 802.3bw

Established &
On the road

Coding PAM3



## 1000BASE-T1

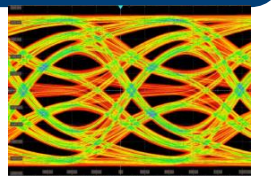
IEEE 802.3bp

3 PHYs released

SOP 2020

OA TC8/TC9/TC12

Coding PAM3



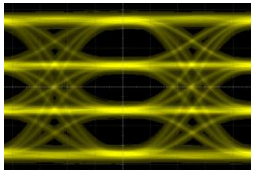
## Multi-gig

2.5/5/10GBASE-T1
STP cable

IEEE 802.3ch
OA TC15 PMA spec
under preparation

OA TC9 (3rd draft released)

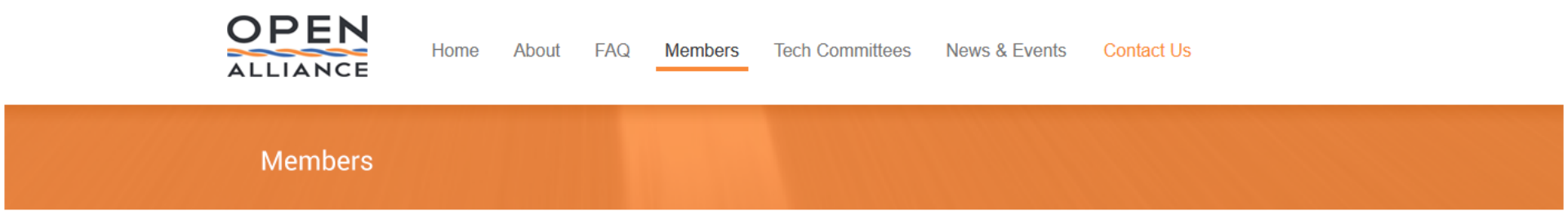
Coding PAM4



...

| | | | | |
|---|---|---|---|---|
| Symbol Rate | 12.5 MBaud | 66.66 MBaud | 750 MBaud | 1.4/2.8/5.6 GBaud |
| Scope | 600MHz scope<br>RTO/RTP | 600MHz scope<br>RTO/RTP | 2GHz scope<br>RTO/RTP | 2.5GBASE-T1: 4GHz → RTP4<br>5GBASE-T1: 8GHz → RTP8<br>10GBASE-T1: 16GHz → RTP16 |
| VNA | ZNB/ZND (4.5GHz) | ZNB/ZND (4.5 GHz) | ZNB/ZND (4.5GHz) | ZNB/ZND (8.5GHz) |

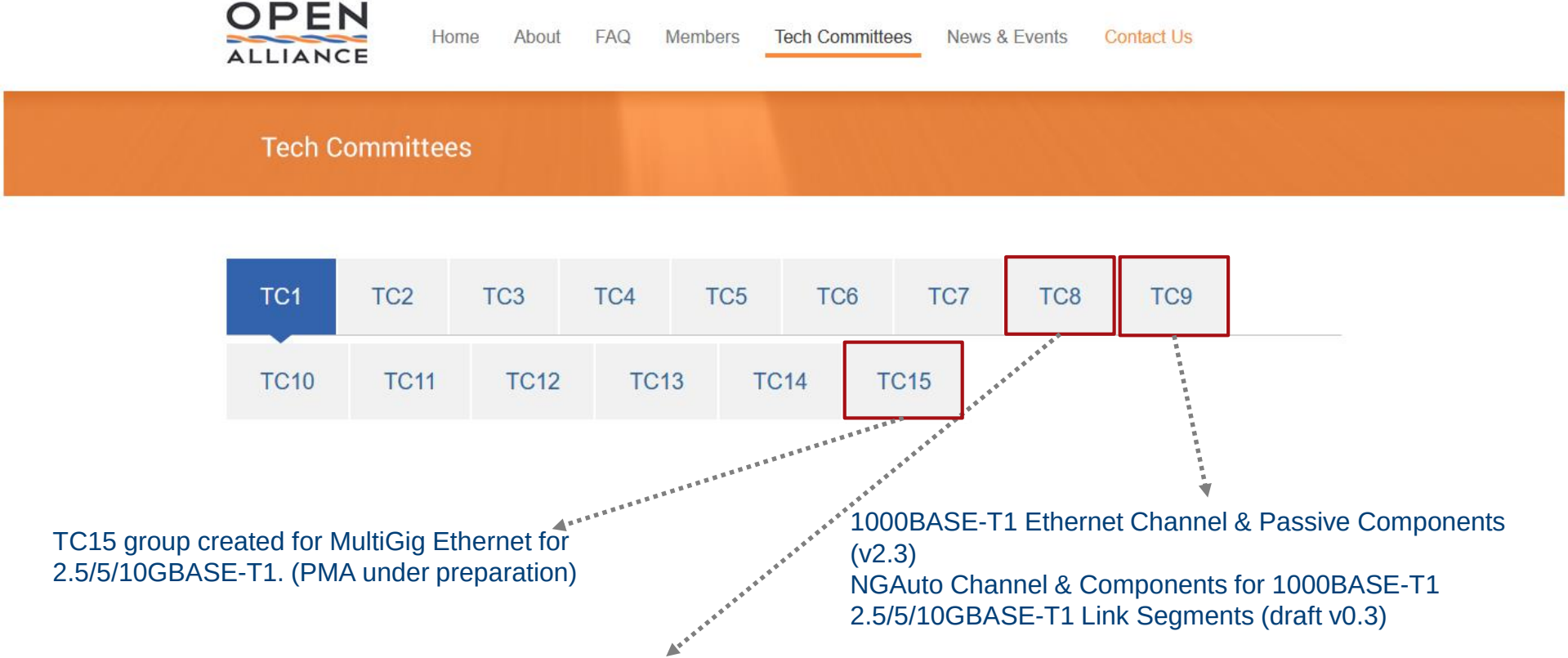
TC8 ECU Specification




# Driven by OEMs

12 Promoters
124 Adopters

http://www.opensig.org/


OPEN ALLIANCE
Home
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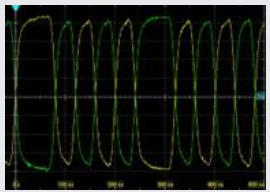
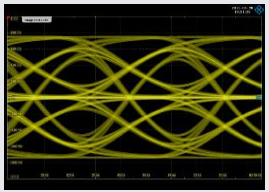
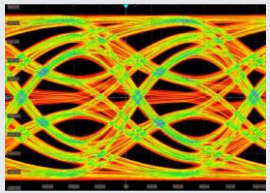
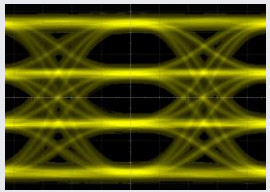
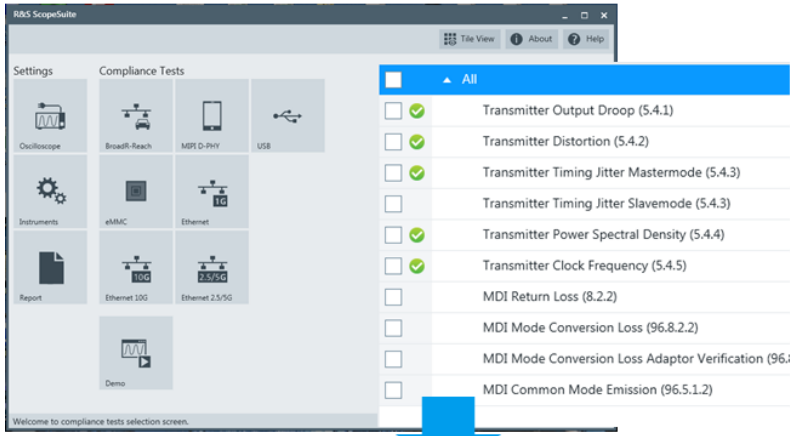
Tech Committees
TC1
TC2
TC3
TC4
TC5
TC6
TC7
TC8
TC9
TC10
TC11
TC12
TC13
TC14
TC15
TC15 group created for MultiGig Ethernet for 2.5/5/10GBASE-T1. (PMA under preparation)
1000BASE-T1 Ethernet Channel & Passive Components (v2.3)
NGAuto Channel & Components for 1000BASE-T1 2.5/5/10GBASE-T1 Link Segments (draft v0.3)
Automotive Ethernet ECU Test Specification (v3.0)
Currently supports 100/1000BASE-T1

# AUTOMOTIVE ETHERNET SUMMARY

| | 10Base-T1S | 100Base-T1 | 1000Base-T1 | NGBase-T1 |
|---|---|---|---|---|
| Datarate | 10Mbps | 100Mbps | 1Gbps | 2.5/5/10Gbps |
| Symbol rate | 12.5MHz | 66.66MHz | 750MHz | 1.4/2.8/5.6GHz |
| Voltage | 1Vpp | 2.2Vpp | 1.3Vpp | 1.3Vpp |
| Communication | Half Duplex or Full Duplex | Full Duplex | Full Duplex | Full Duplex |
| Configuration | Point to Point<br>Multidrop | Point to Point | Point to Point | Point to Point |
| Encoding | 2-Level DME  | PAM3  | PAM3  | PAM4  |
| Application | Audio, Parking ECU, Engine ECU, Body ECU.. | Infotainment, Driver Assistance systems | Infotainment, Driver Assistance systems | Infotainment, Driver Assistance systems, ECU to ECU |

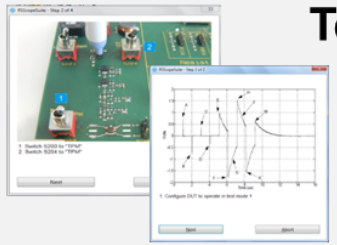
# R&S ScopeSuite
# BUILT-IN COMPLIANCE TEST SOFTWARE & REPORTING TOOL



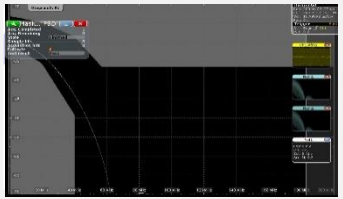

## Pass-Fail results

| Test | Description | Run | Result | Detail |
|---|---|---|---|---|
| Output Droop | | 1 | ✓ | 2/2 |
| Transmitter Distortion No TX_TCLK No Disturber | | 1 | ✓ | 11/11 |
| Transmitter Timing Jitter Mastermode | | 1 | ✓ | 1/1 |
| Power Spectral Density | | 1 | ✗ | 0/1 |
| Power Spectral Density | | 2 | ✓ | 1/1 |
| Transmitter Clock Frequency | | 1 | ✓ | 1/1 |

## Test



Guided steps



Auto measurements

## Report

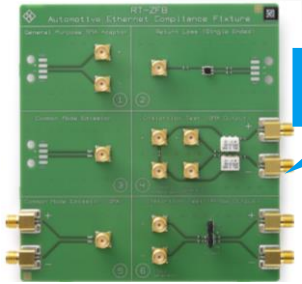
- Screenshot
- Measurement result
- Pass-Fail result
- Test summary

# FROM 10BASE-T1 TO 10GBASE-T1 COMPLIANCE TEST

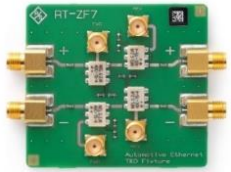
## Key Features

- Complete test solution from R&S (PHY layer)
- Includes OEM required test cases
- Future proof solution for Automotive Ethernet
- UNH-IOL uses RTO + ZNB for all automotive Ethernet tests
- Dedicated test fixtures made by R&S – OA TC8 compliant!

New → MultiGBASE-T1 (only a software option – K88)



Compliance Test fixture RT-ZF8

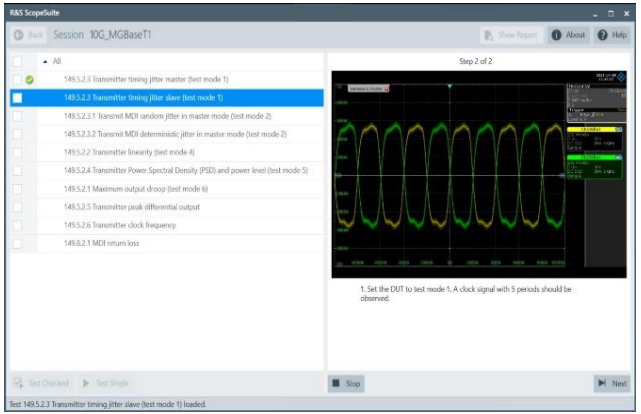


Decoding fixture RT-ZF7

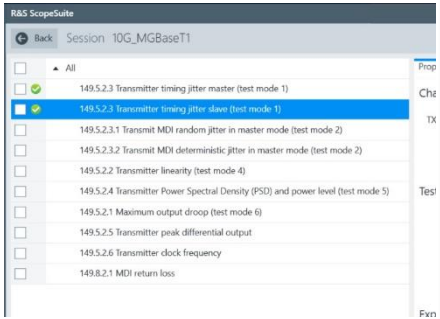
SMA adapter for TD & Compliance RT-ZF7A

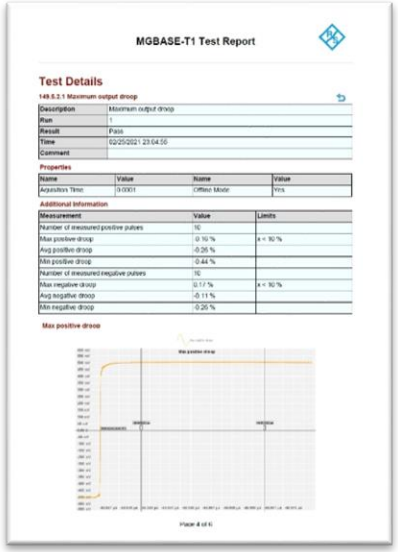
Frequency converter RT-ZF3/6

# NEW MULTIGBASE-T1 COMPLIANCE TEST SOLUTION


- New K88 AUT Ethernet compliance option for 2.5/5/10G speeds
- Based on the IEEE 802.3ch
- Uses PAM4 modulation with symbol rates of 1.4/2.8/5.6 GHz
- Runs exclusively on shielded twisted pair (STP)
- Additional information:
  - Available on both the RTO (up to 2.5G) and RTP
  - Coverage of all relevant test cases
  - No additional options required (e.g. jitter)
  - Complete solution with VNA and ZF7A test fixtures



# IEEE 802.3CH CLAUSE 149 TEST PATTERNS TABLE 149-17


### 149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

#### 149.5.1 Test modes

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

# TEST MODE 1


**149.5 PMA electrical specifications**

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

**149.5.1 Test modes**

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
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| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

- “Normal operation” test mode
- Transmit reduced PHY symbol clock (TX_TCLK_175) to measure clock jitter
- Clock frequency of 175.78125 MHz
- Access through SMA connector or pin header

# TEST MODE 2

### 149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

#### 149.5.1 Test modes

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
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| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

**Table 149–18—Jitter test modes**

| Test pattern |
|---|
| Square wave: TX_TCLK_175 |
| JP03A (as specified in 94.2.9.1) |
| JP03B (as specified in 94.2.9.2) |

# TEST MODE 2.1


### 149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

#### 149.5.1 Test modes

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

**Table 149–18—Jitter test modes**

| Test pattern |
|---|
| Square wave: TX_TCLK_175 |
| JP03A (as specified in 94.2.9.1) |
| JP03B (as specified in 94.2.9.2) |

- 175.78125 MHz square wave
- Measures MDI random jitter

# TEST MODE 2.2

**149.5 PMA electrical specifications**

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

**149.5.1 Test modes**

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

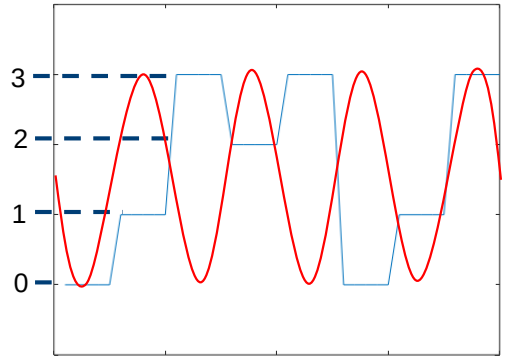
**Table 149–18—Jitter test modes**

| Test pattern |
|---|
| Square wave: TX_TCLK_175 |
| JP03A (as specified in 94.2.9.1) |
| JP03B (as specified in 94.2.9.2) |

- High frequency (sine wave) test pattern
- PAM4 encoded {0,3} sequence
- Measures MDI deterministic jitter

PAM4 Sequence

JP03A



# TEST MODE 2.3

**149.5 PMA electrical specifications**

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

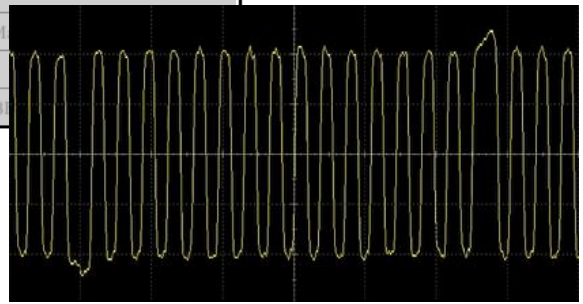
**149.5.1 Test modes**

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD M |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BI |

**Table 149–18—Jitter test modes**

| Test pattern |
|---|
| Square wave: TX_TCLK_175 |
| JP03A (as specified in 94.2.9.1) |
| JP03B (as specified in 94.2.9.2) |



- Mixed frequency test pattern
- PAM4 encoded sequence of 15×S {0,3} +16×S {3,0} symbols
- Inserts “33” and “00” every 30 symbols
- Measures MDI Even-Odd jitter

# TEST MODE 4

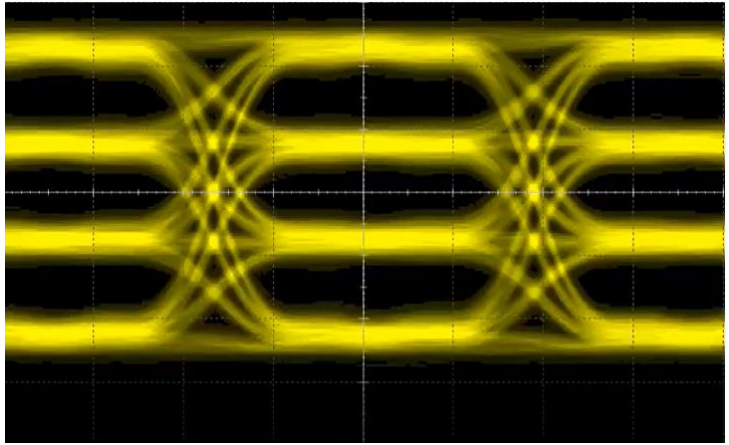
**149.5 PMA electrical specifications**

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

**149.5.1 Test modes**

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |



- Used for transmitter linearity
- PRBS13Q – “Q” for quad or 4-level PRBS
- 8191 symbol sequence created from Gray coding two PRBS13 patterns into PAM4 symbols

# TEST MODE 5


**149.5 PMA electrical specifications**

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

**149.5.1 Test modes**

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

- Used for TX PSD / Power level
- Scrambled PAM4 symbols
- MASTER mode scrambler from idle sequence

# TEST MODE 5

### 149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

#### 149.5.1 Test modes

**Table 149–17—MDIO management registers settings for test modes**

| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
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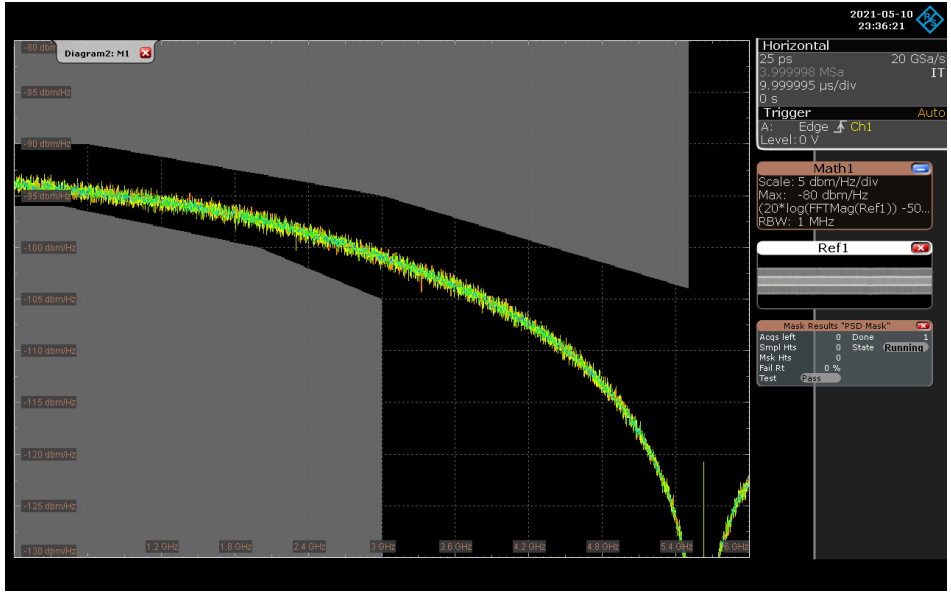
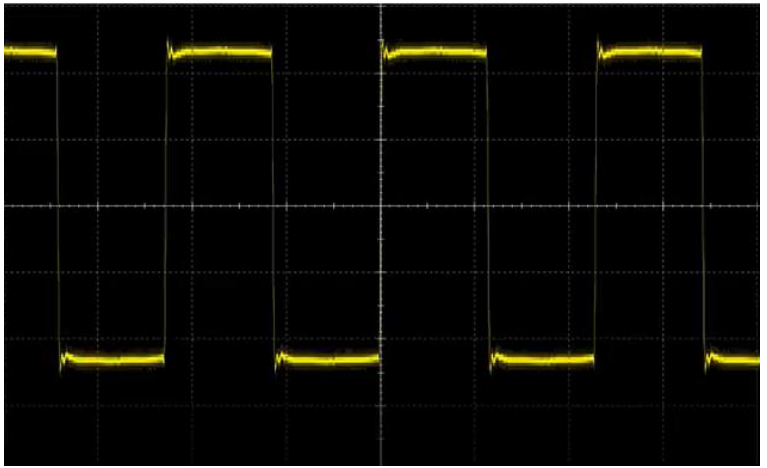
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |



# TEST MODE 6



### 149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

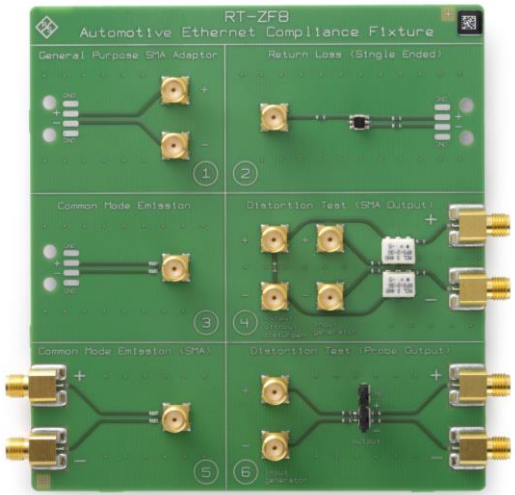
#### 149.5.1 Test modes

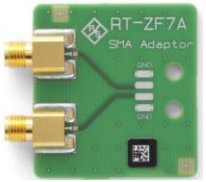
**Table 149–17—MDIO management registers settings for test modes**

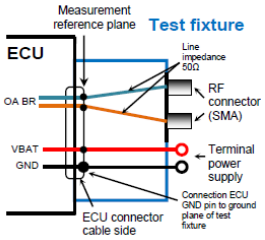
| Register description |
|---|
| Normal (non-test mode) operation. |
| Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode. |
| Test mode 2—Transmit MDI jitter test in MASTER mode. |
| Test mode 3—Precoder test mode. |
| Test mode 4—Transmitter linearity test. |
| Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test. |
| Test mode 6—Transmitter droop test mode. |
| Test mode 7—Normal operation with zero data pattern. This is for BER monitoring. |

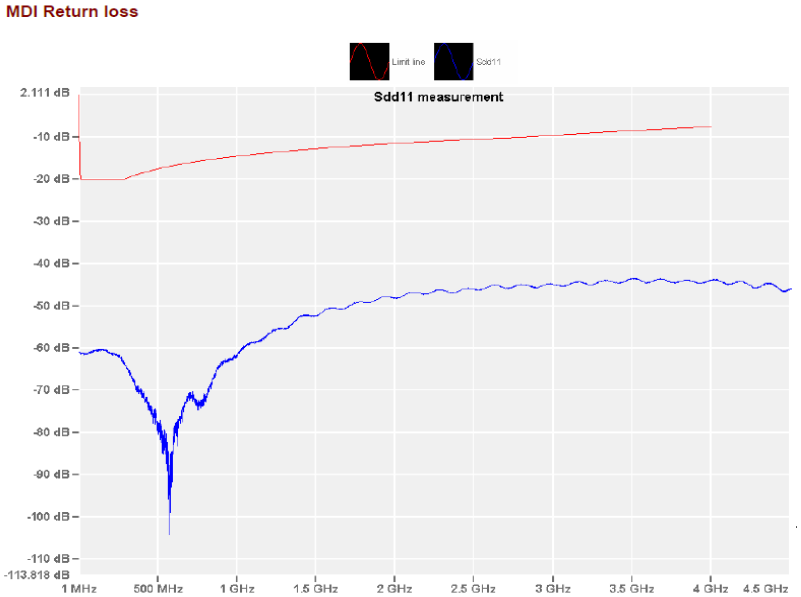
- Low frequency square wave for measuring TX droop
- 128×S {+1} + 128×S {-1} symbols

# MDI Return loss 149.8.2.1



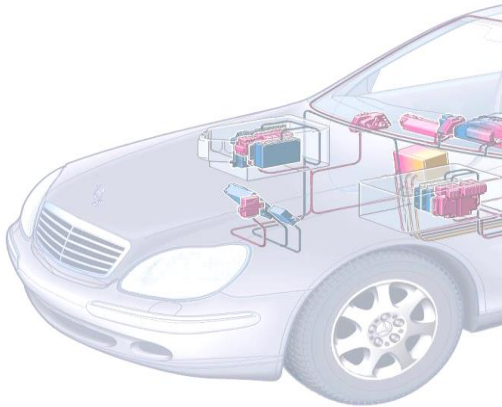

R&S®ZNB 4-port VNA 9kHz – 40GHz

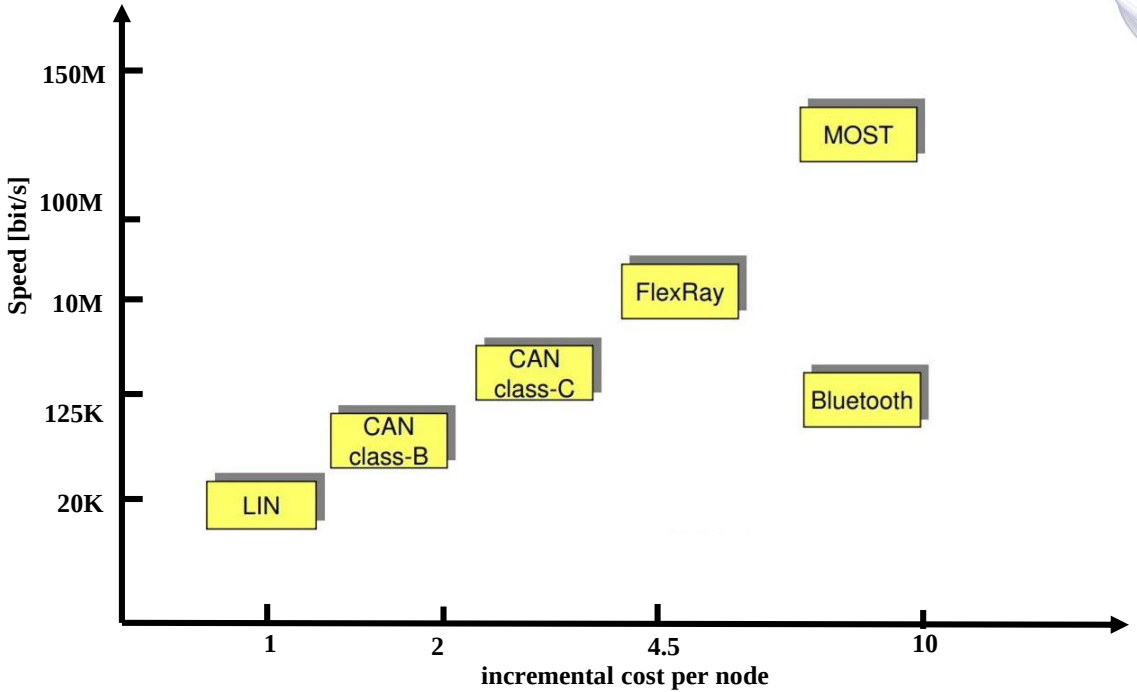
# AUTOMOTIVE TESTING PHY LAYER SUMMARY

| | | | |
|---|---|---|---|
|  | R&S®RTP | Max freq. 16GHz | OA TC8 & OA TC15<br>Supports speeds up to 10GBASE-T1 |
|  | R&S®RTO6 | Max freq. 6GHz | OA TC8 & OA TC15<br>Supports speeds up to 2.5GBASE-T1 |
|  | R&S®ZNB | 4-port VNA<br>9kHz – 40GHz | OA TC9, OA TC8 & OA TC15<br>8GHz VNA sufficient for 10GBASE-T1 |

# SERIAL BUS CAN/LIN IN THE AUTOMOBILE

# OVERVIEW – PERFORMANCE VS. COST/COMPLEXITY

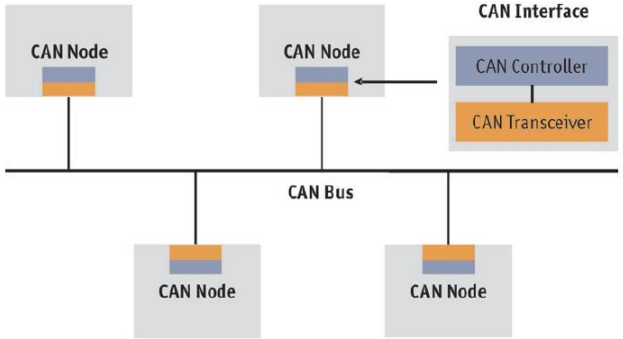




# CAN – INTRODUCTION (I)

- Controller Area Network (CAN) is ISO standard (ISO 11898) for serial communication
- Developed 1980s by BOSCH for automotive applications
  - Also found in industrial and medicine applications
- CAN standard defines
  - Physical layer
    - Low-speed (max. 125 kbps), high-speed (max. 1 Mbps)
    - Driver/receiver characteristics
    - Bit enconding/decoding and synchronization
  - Data-link layer
    - Message types
    - Arbitration rules for bus access
    - Methods for fault detection and fault confinement

# CAN – INTRODUCTION (II)

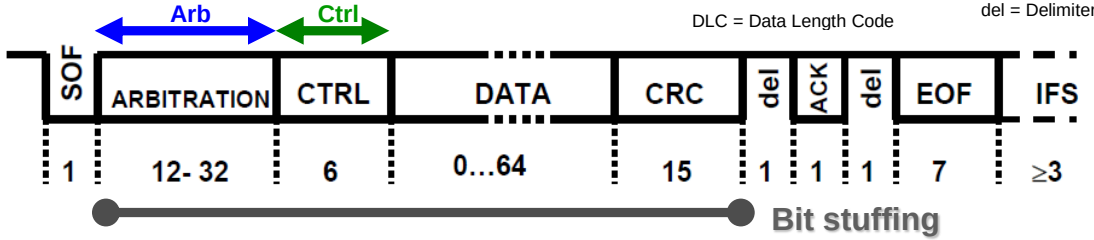



- Asynchronous Serial Bus
  - Transfer rate: 10 kbps to 1 Mbps
- Multi-master / Broadcasting concept
- Absence of node addressing
  - Message identifier specifies contents and priority
  - Lowest message identifier has highest priority
- Non-destructive arbitration system
  - CSMA for collision detection
- Sophisticated error detection and handling
  - Operating 1000 h/year, transfer rate 500 kbps and mean bus load 25% yields one undetected faulty frame in 4000 years

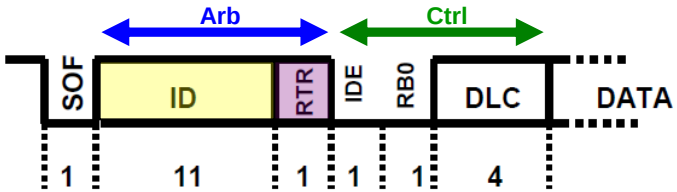
# CAN – DATA / REMOTE FRAME

SOF = Start of Frame
RTR = Remote Transm. Request
SRR = Substitute Remote Requ.
IDE = Identifier Extension
RB0/1 = Reserved bits
DLC = Data Length Code

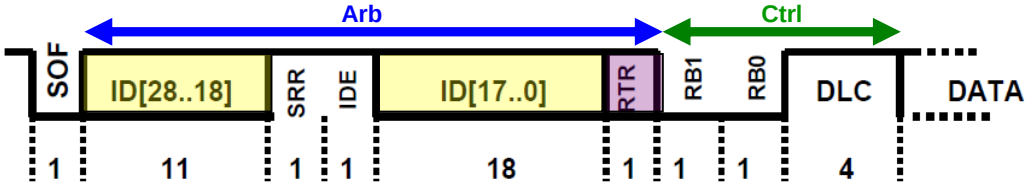
CRC = Cyclic Redundancy Check
ACK = Acknowledge
EOF = End of Frame
IFS = Inter Frame Spacing
del = Delimiter




Standard format




Extended format

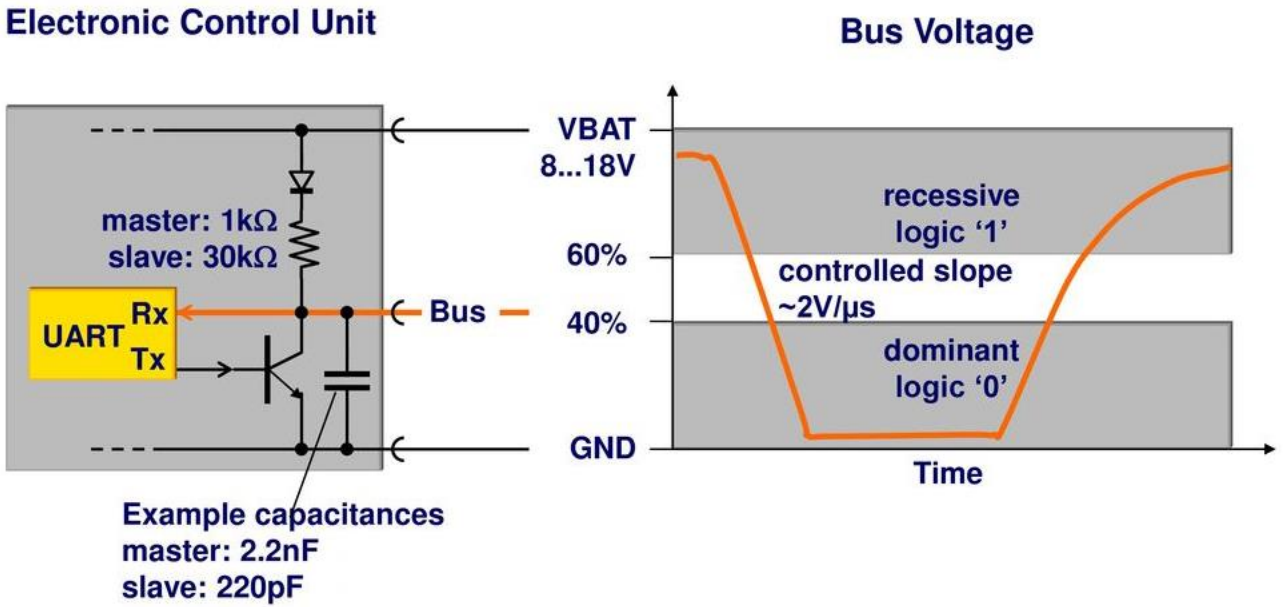



**Remember:** Remote frames always lack data field even when DLC > 0

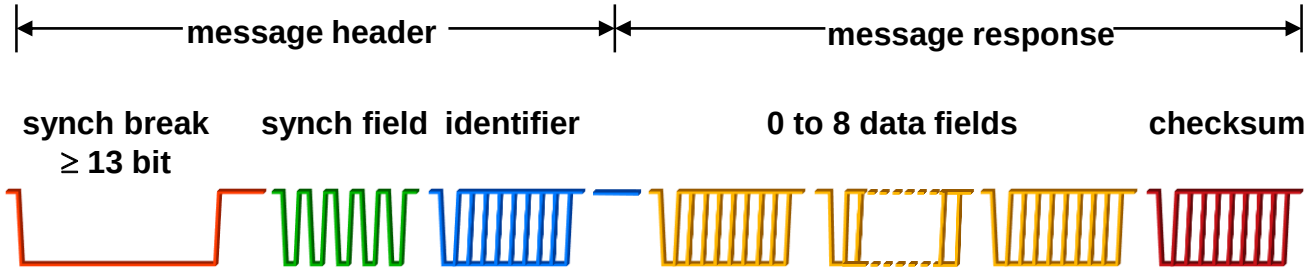
# LIN – OVERVIEW

- Local Interconnect Network (LIN) standard developed by LIN Consortium
  - Several versions coexist: v1.3 (2002), v2.0 (major revision, basis for SAE J2602, 2003), v2.1 (clarifications, diagnostics added, and more, 2006)
- LIN provides cost-efficient communication where bandwidth and versatility of CAN is not required
  - Mirror, window lift, door lock, air conditioning, windshield wipers, turning light...
- Low cost single-wire implementation
- Speed up to 20 Kbit/s
- Single Master / Multiple Slave communication
- Low cost silicon implementation based on UART interface hardware
- Self-synchronization without crystal or ceramics resonators in slave nodes
- Only very basic error detection,
  error handling happens at application code level

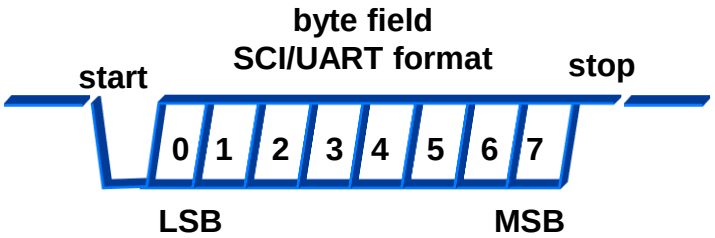
# LIN – PHYSICAL INTERFACE



# LIN – MESSAGE FRAME (I)




- Break field
  - Determines start of frame
- Synch field
  - Toggling pattern (55h) for synchronization of slave clock to master clock



# EASY ACCESS VIA THE APP-COCKPIT


RTO6

RTP

MXO 4

MXO 5

# TRIGGER AND DECODE SUMMARY

| | | |
|---|---|---|
| **RTP** |  | I²C SPI CAN LIN 100M 1000M |
| **RTO6** |  | I²C SPI CAN LIN 100M 1000M |
| **MXO 5** |  | I²C SPI CAN LIN |
| **MXO 4** |  | I²C SPI CAN LIN |

# Test it! Trust it!