車聯網時代之車載通訊的蛻變與挑戰
- 車用乙太網路測試

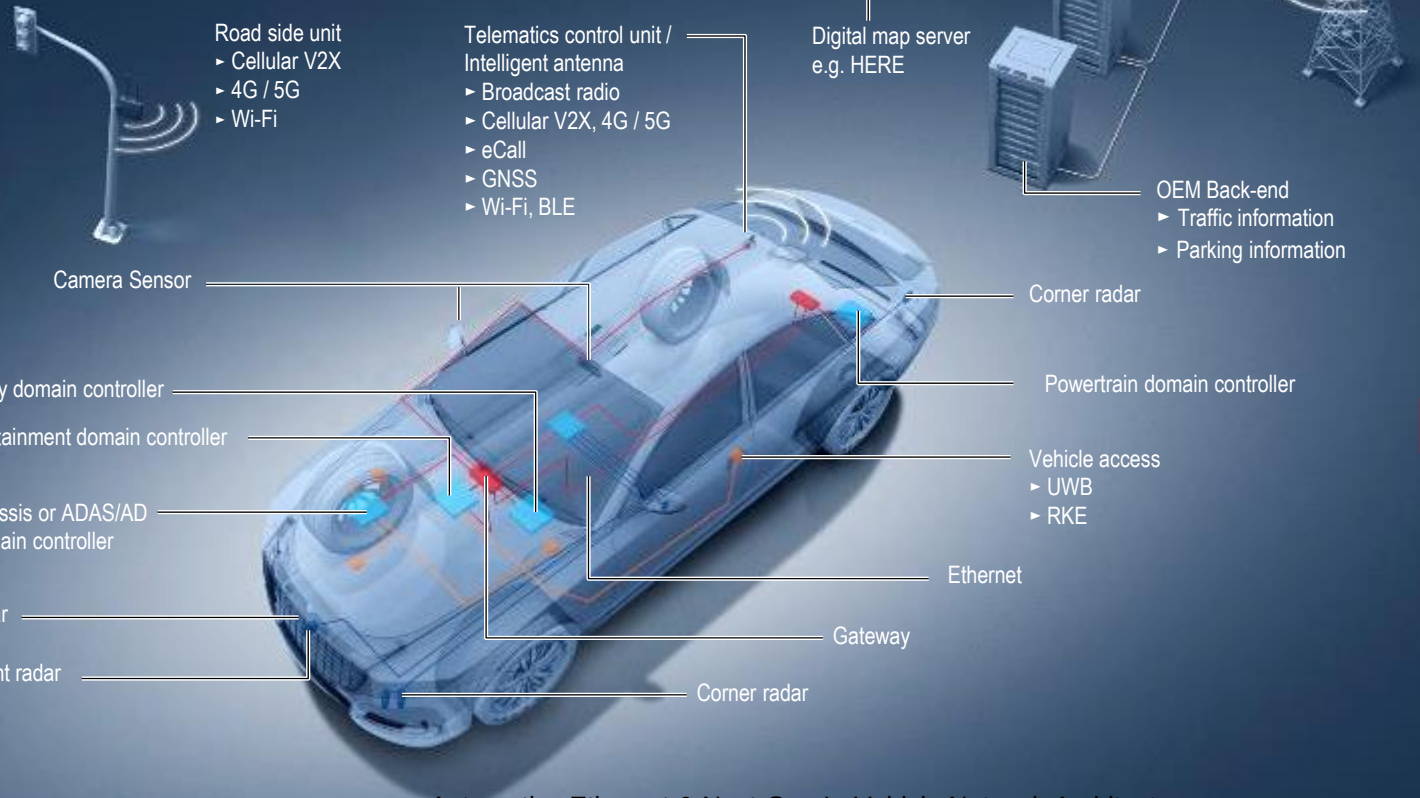
Rohde & Schwarz Taiwan Ltd.
Oscilloscope

ROHDE&SCHWARZ
Make ideas real

AGENDA

- Automotive In-Vehicle Network trends
- Introduce to Automotive Ethernet
- Automotive Ethernet Test Requirement
  - Compliance Test
  - Automotive bus protocol Decode
  - EMI debugging
- CAN/LIN Bus
- Summary

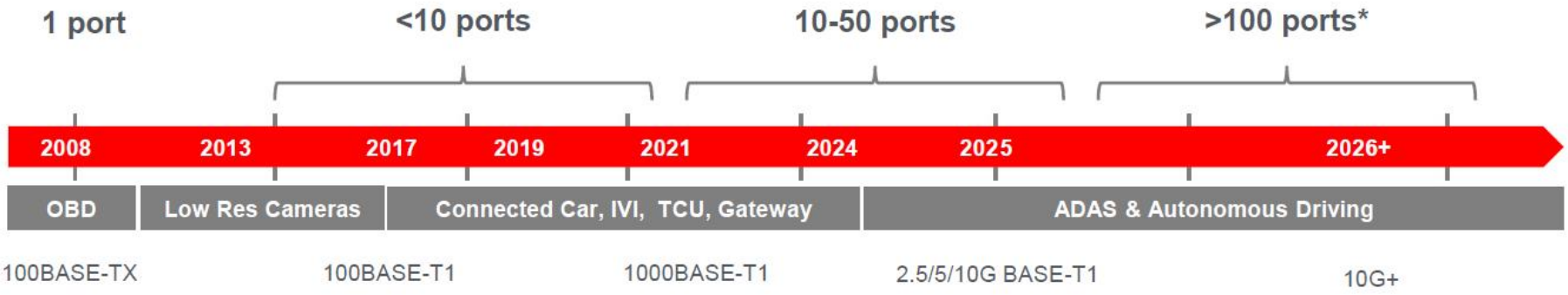
VEHICLE ARCHITECTURE WITH HIGH PERFORMANCE COMPUTERS



Automotive Test Solutions

- Radar
- Connectivity
- 4G / 5G Network; Quality Analysis
- Infotainment
- In-Vehicle Networks (AUT Ethernet)
- ECU & Domain Controller Testing
- Battery Management Systems
- EMC / Full Vehicle Antenna Testing
- Storage Solutions & Cybersecurity

Trends in Automotive Ethernet



*average Ethernet ports per vehicle
** Photo courtesy of Marvell Technology Group

FUTURE AUTOMOTIVE ETHERNET STANDARDS

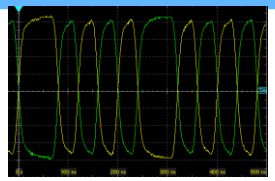
10BASE-T1S

IEEE 802.3cg

Multidrop
PoDL

OA TC6 & TC14

Coding NRZ



Symbol Rate 12.5 MBaud

Scope 600MHz scope
RTO/RTP

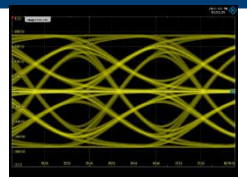
VNA ZNB/ZND (4.5GHz)

100BASE-T1

IEEE 802.3bw

Established &
On the road

Coding PAM3



66.66 MBaud

600MHz scope
RTO/RTP
ZNB/ZND (4.5 GHz)

1000BASE-T1

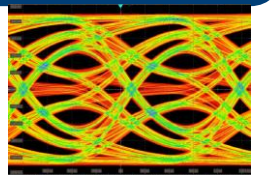
IEEE 802.3bp

3 PHYs released

SOP 2020

OA TC8/TC9/TC12

Coding PAM3



750 MBaud

2GHz scope
RTO/RTP
ZNB/ZND (4.5GHz)

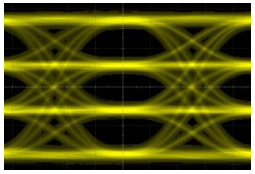
Multi-gig

2.5/5/10GBASE-T1
STP cable

IEEE 802.3ch
OA TC15 PMA spec
under preparation

OA TC9 (3rd draft released)

Coding PAM4

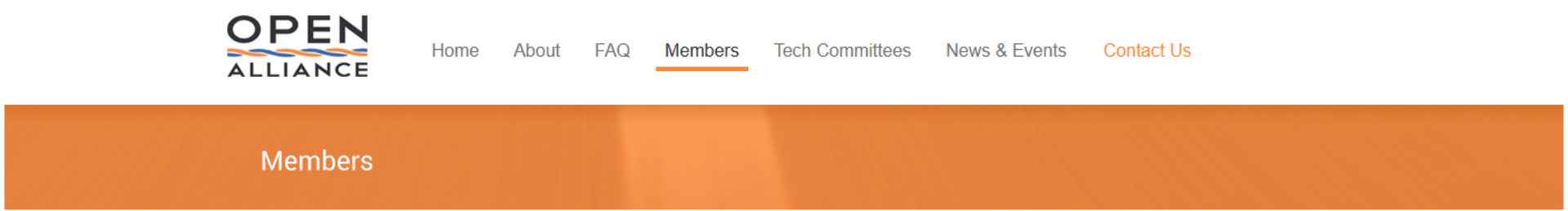


1.4/2.8/5.6 GBaud

2.5GBASE-T1: 4GHz → RTP4
5GBASE-T1: 8GHz → RTP8
10GBASE-T1: 16GHz → RTP16
ZNB/ZND (8.5GHz)

...

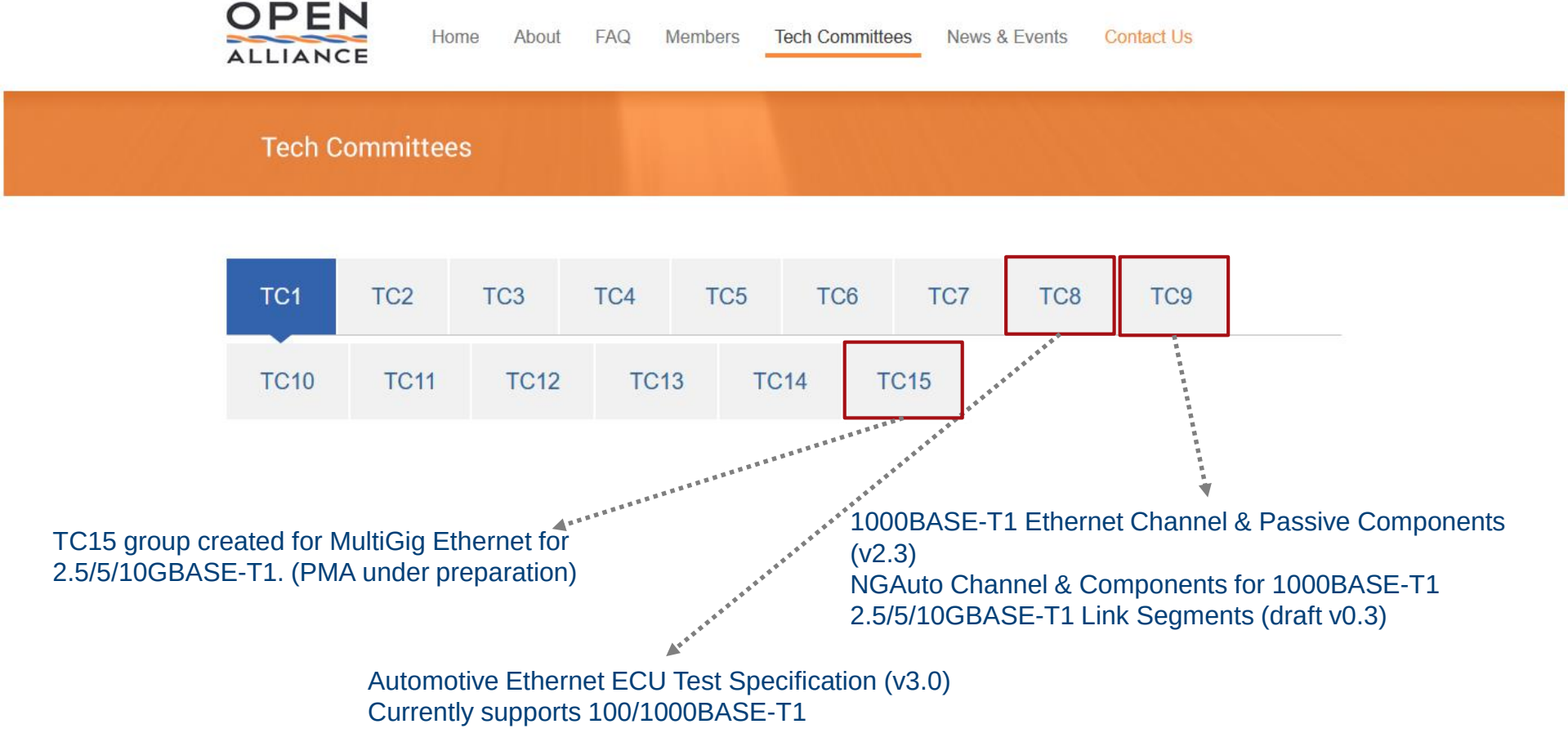
TC8 ECU Specification



Driven by OEMs

12 Promoters
124 Adopters

http://www.opensig.org/


OPEN ALLIANCE
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News & Events
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Tech Committees
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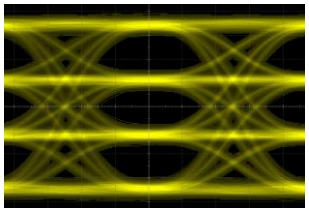
TC12
TC13
TC14
TC15
TC15 group created for MultiGig Ethernet for 2.5/5/10GBASE-T1. (PMA under preparation)
1000BASE-T1 Ethernet Channel & Passive Components (v2.3)
NGAuto Channel & Components for 1000BASE-T1 2.5/5/10GBASE-T1 Link Segments (draft v0.3)
Automotive Ethernet ECU Test Specification (v3.0)
Currently supports 100/1000BASE-T1

AUTOMOTIVE ETHERNET SUMMARY

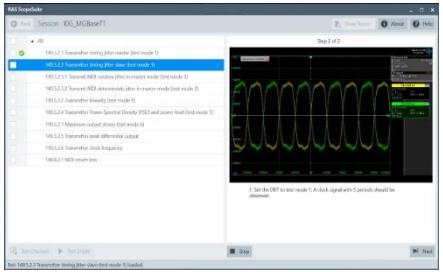
	10Base-T1S	100Base-T1	1000Base-T1	NGBase-T1
Datarate	10Mbps	100Mbps	1Gbps	2.5/5/10Gbps
Symbol rate	12.5MHz	66.66MHz	750MHz	1.4/2.8/5.6GHz
Coding	4B/5B, Differential Manchester Encoding(DME)	PAM3	PAM3	PAM4
Voltage	1Vpp	2.2Vpp	1.3Vpp	1.3Vpp
Communication	Half Duplex or Full Duplex	Full Duplex	Full Duplex	Full Duplex
Configuration	Point to Point Multidrop	Point to Point	Point to Point	Point to Point
Cable length	15/25m	15m	15m	15m
Cable type	24-26 AWG	Unshielded twisted pair	Unshielded twisted pair	Unshielded twisted pair
Application	Audio, Parking ECU, Engine ECU, Body ECU..	Infotainment, Driver Assistance systems	Infotainment, Driver Assistance systems	Infotainment, Driver Assistance systems, ECU to ECU

DEMO

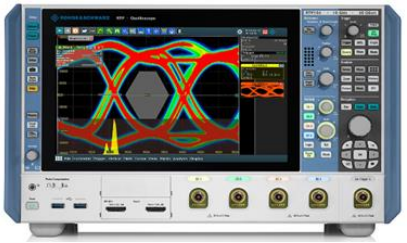
Objective: Verify general PMA performance (jitter, eye) and conduct TX compliance testing



Step 1: Step through test modes to visually confirm patterns are correct

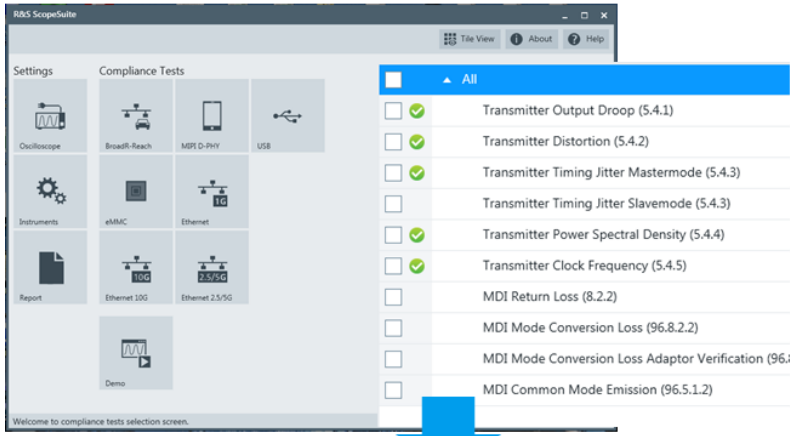


Step 2: Run 802.3 PHY conformance tests with ScopeSuite automation software



Step 3: Characterize TX performance with additional signal integrity analysis

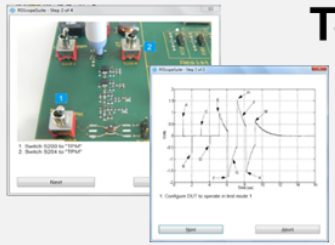
R&S ScopeSuite
BUILT-IN COMPLIANCE TEST SOFTWARE & REPORTING TOOL



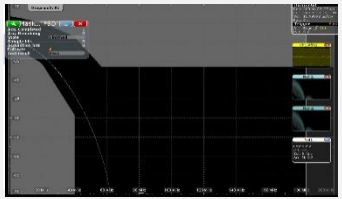
Pass-Fail results

Test	Description	Run	Result	Detail
Output Droop		1	✓	2/2
Transmitter Distortion No TX_TCLK No Disturber		1	✓	11/11
Transmitter Timing Jitter Mastermode		1	✓	1/1
Power Spectral Density		1	✗	0/1
Power Spectral Density		2	✓	1/1
Transmitter Clock Frequency		1	✓	1/1

Test



Guided steps



Auto measurements

Report

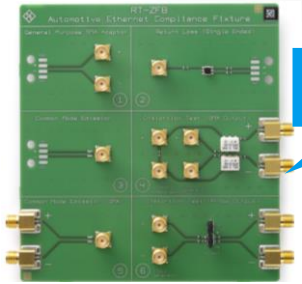
- Screenshot
- Measurement result
- Pass-Fail result
- Test summary

FROM 10BASE-T1 TO 10GBASE-T1 COMPLIANCE TEST

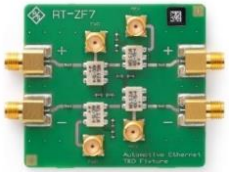
Key Features

- Complete test solution from R&S (PHY layer)
- Includes OEM required test cases
- Future proof solution for Automotive Ethernet
- UNH-IOL uses RTO + ZNB for all automotive Ethernet tests
- Dedicated test fixtures made by R&S – OA TC8 compliant!

New → MultiGBASE-T1 (only a software option – K88)



Compliance Test fixture RT-ZF8

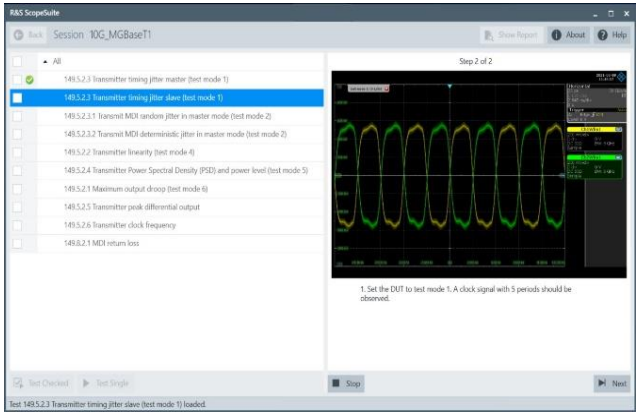


Decoding fixture RT-ZF7

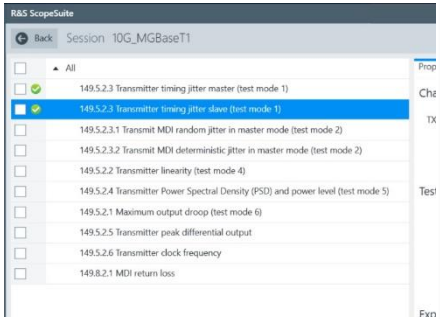
SMA adapter for TD & Compliance RT-ZF7A

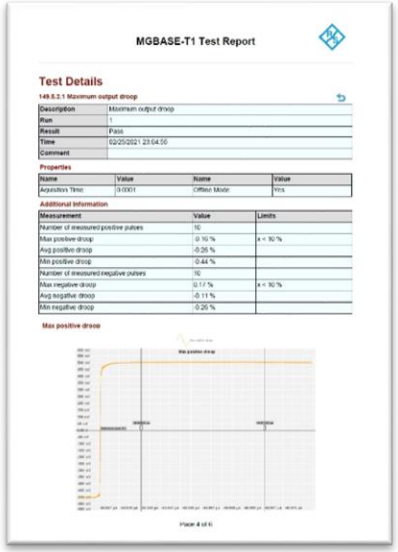
Frequency converter RT-ZF3/6

NEW MULTIGBASE-T1 COMPLIANCE TEST SOLUTION



- New K88 AUT Ethernet compliance option for 2.5/5/10G speeds
- Based on the IEEE 802.3ch
- Uses PAM4 modulation with symbol rates of 1.4/2.8/5.6 GHz
- Runs exclusively on shielded twisted pair (STP)
- Additional information:
  - Available on both the RTO (up to 2.5G) and RTP
  - Coverage of all relevant test cases
  - No additional options required (e.g. jitter)
  - Complete solution with VNA and ZF7A test fixtures





IEEE 802.3CH CLAUSE 149 TEST PATTERNS TABLE 149-17

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

TEST MODE 1

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
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Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- “Normal operation” test mode
- Transmit reduced PHY symbol clock (TX_TCLK_175) to measure clock jitter
- Clock frequency of 175.78125 MHz
- Access through SMA connector or pin header

TEST MODE 2

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

TEST MODE 2.1

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
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Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

- 175.78125 MHz square wave
- Measures MDI random jitter

TEST MODE 2.2

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

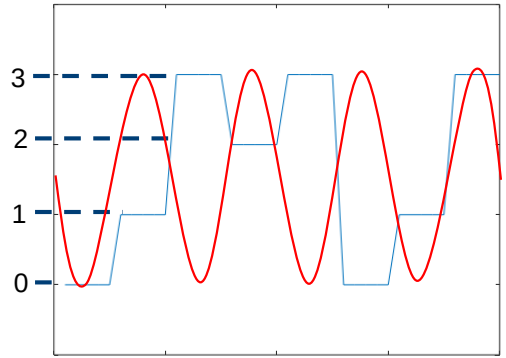
Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

- High frequency (sine wave) test pattern
- PAM4 encoded {0,3} sequence
- Measures MDI deterministic jitter

PAM4 Sequence

JP03A



TEST MODE 2.3

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Table 149–18—Jitter test modes

Test pattern
Square wave: TX_TCLK_175
JP03A (as specified in 94.2.9.1)
JP03B (as specified in 94.2.9.2)

- Mixed frequency test pattern
- PAM4 encoded sequence of 15×S {0,3} +16×S {3,0} symbols
- Inserts “33” and “00” every 30 symbols
- Measures MDI Even-Odd jitter

TEST MODE 4

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- Used for transmitter linearity
- PRBS13Q – “Q” for quad or 4-level PRBS
- 8191 symbol sequence created from Gray coding two PRBS13 patterns into PAM4 symbols

TEST MODE 5

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

- Used for TX PSD / Power level
- Scrambled PAM4 symbols
- MASTER mode scrambler from idle sequence

TEST MODE 5

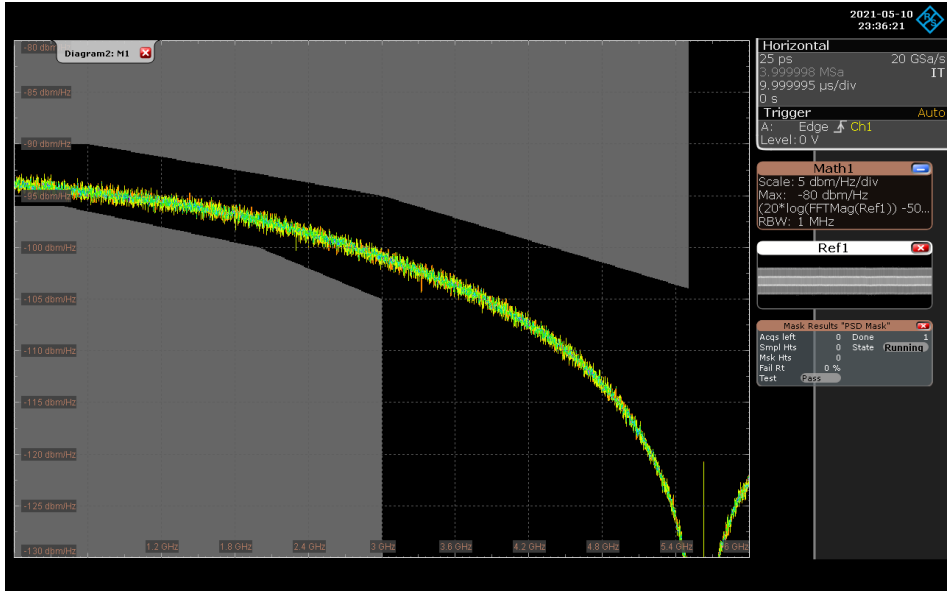
149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

Table 149–17—MDIO management registers settings for test modes

Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.



TEST MODE 6

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

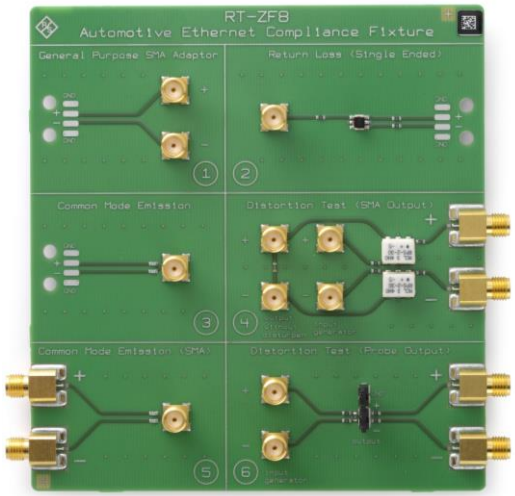
149.5.1 Test modes

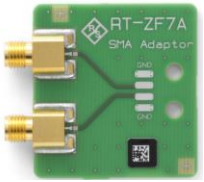
Table 149–17—MDIO management registers settings for test modes

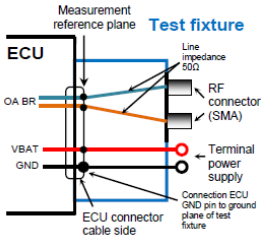
Register description
Normal (non-test mode) operation.
Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
Test mode 2—Transmit MDI jitter test in MASTER mode.
Test mode 3—Precoder test mode.
Test mode 4—Transmitter linearity test.
Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
Test mode 6—Transmitter droop test mode.
Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

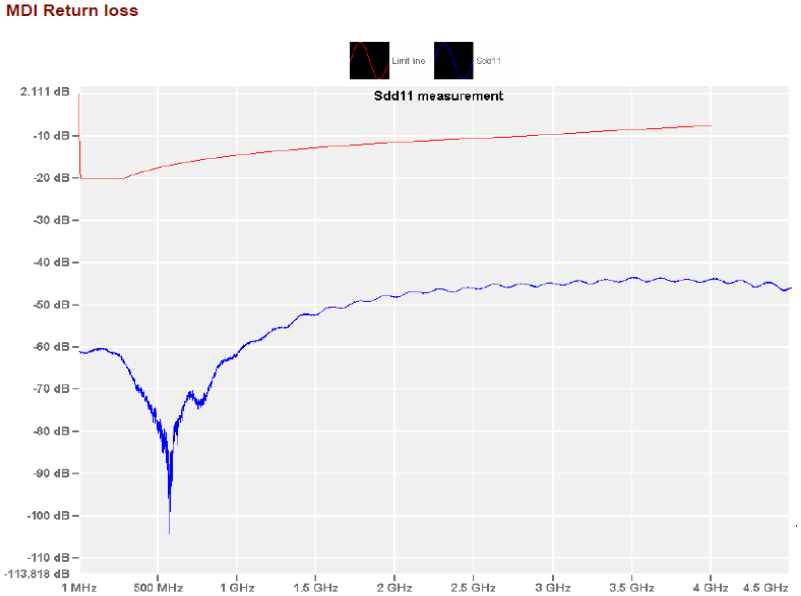
- Low frequency square wave for measuring TX droop
- 128×S {+1} + 128×S {-1} symbols

MDI Return loss 149.8.2.1









R&S®ZNB 4-port VNA 9kHz – 40GHz

100/1000BASE-T1 TRIGGER & DECODE APPLICATIONS
EXAMPLE: VERIFY TSN SWITCH PERFORMANCE

RTP with K35 sw option

Ch.1/2

Ch.3/4

TSN Box 3.0 Talker

DUT
TSN Switch

TSN Box 3.0 Listener

RT-ZF7/7A test fixtures

***Switch delay** = Trig(Ch.1) to frame(Ch.2)

Meas Result 1

Protocol measurement	Current	Max	Min	Mean	RMS	σ (S-dev)	Event count	Wave count
Trig to frame	1.0998 µs	1.1005 µs	1.0675 µs	1.0861 µs	1.0862 µs	12.315 ns	1009	1022

TELEMATICS CONTROL UNIT (TCU): THE GATEWAY TO CONNECTED CARS

Image source: Ficosa

Important to know:

- Some automotive 4G LTE modems implemented in the TCU can operate at 300-400 Mbps

- IAM: 5G speeds up to 1.6Gbps*

*Maximum theoretical download speed

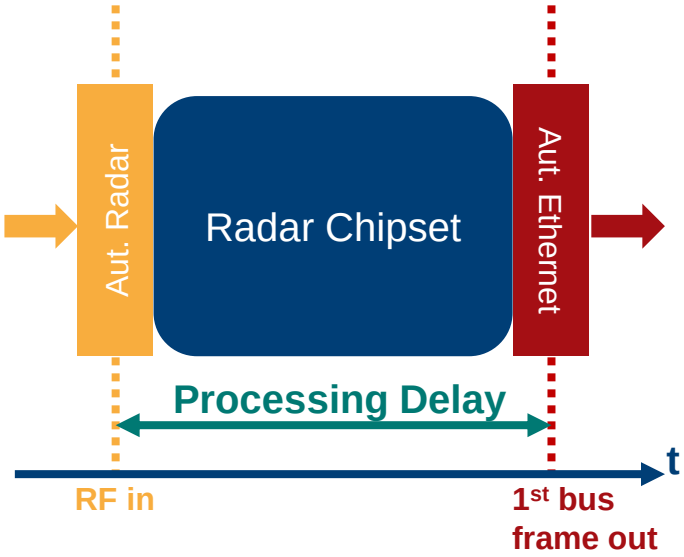
Image source: Continental

100/1000BASE-T1 TRIGGER & DECODE APPLICATIONS
EXAMPLE: ADAS SENSOR LATENCY

- Safety-critical applications (e.g. self-driving vehicles) have **strict latency** requirements

- Oscilloscope multi-domain capabilities allow measuring system delay of single components and verifying if latency requirements are met

Mode	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5GBASE-T1	1x	10 240	20	4096
5GBASE-T1	1x	10 240	20	2048
5GBASE-T1	2x	13 824	27	2764.8
10GBASE-T1	1x	10 240	20	1024
10GBASE-T1	2x	13 824	27	1382.4
10GBASE-T1	4x	20 480	40	2048



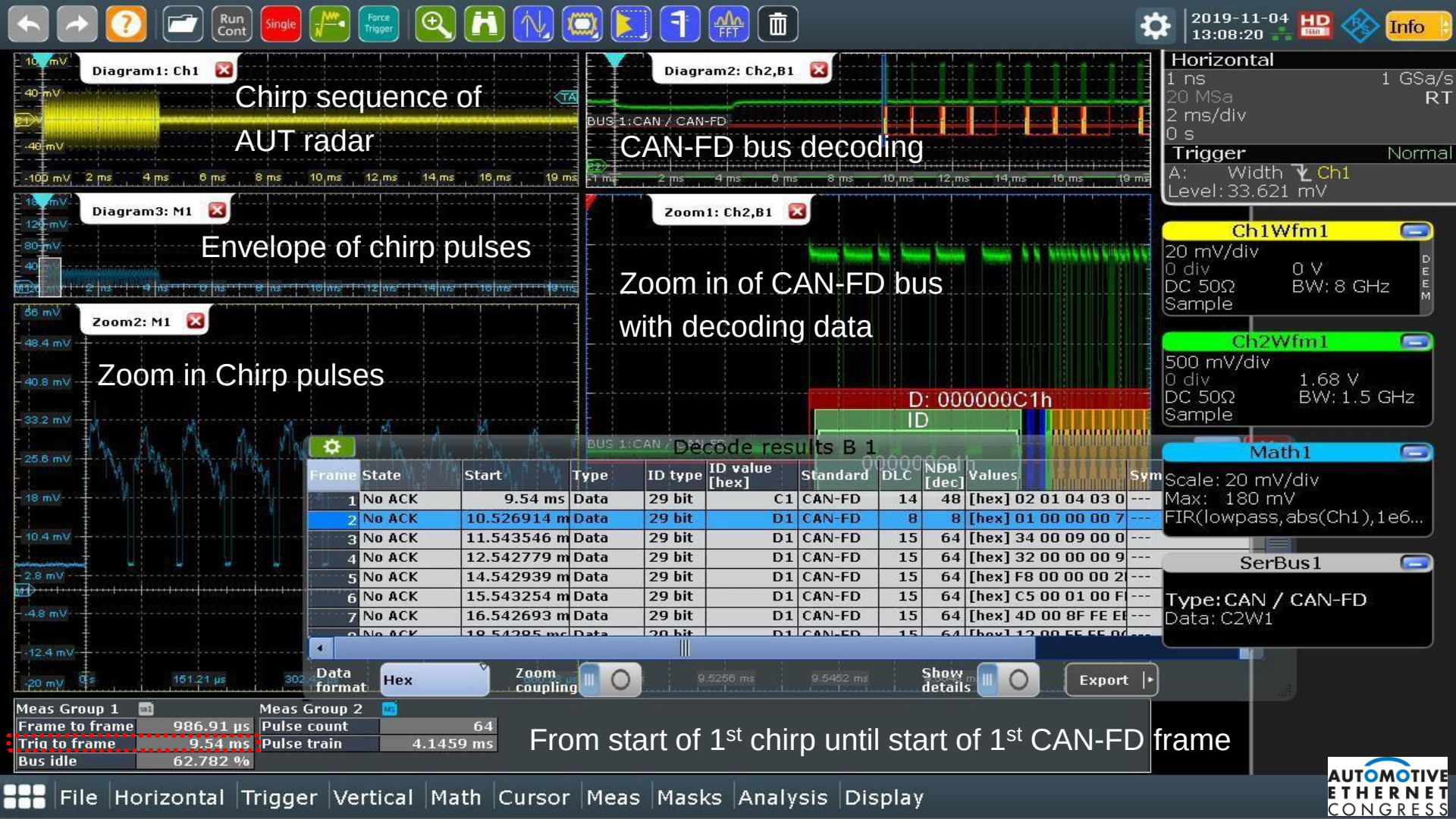
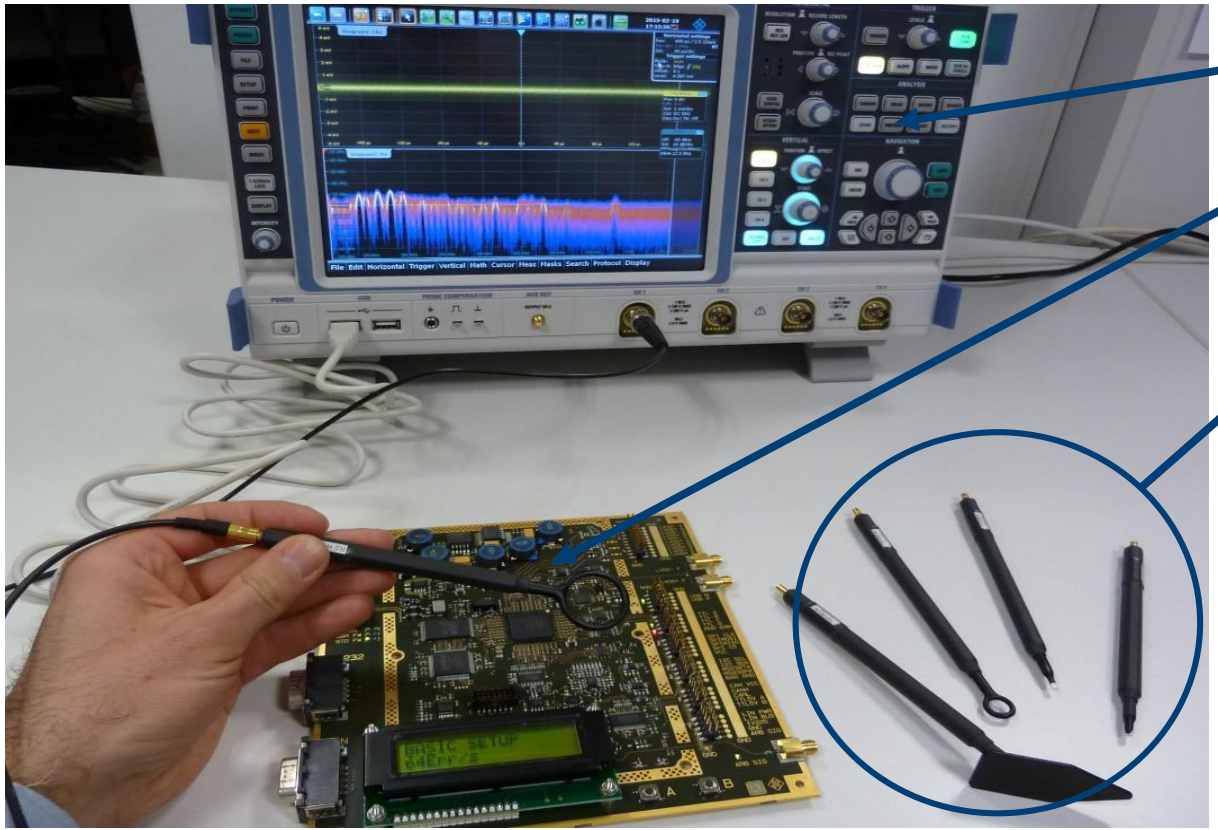


Diagram1: Ch1
Chirp sequence of
AUT radar
Diagram2: Ch2,B1
BUS 1:CAN / CAN-FD
CAN-FD bus decoding
Diagram3: M1
Envelope of chirp pulses
Zoom1: Ch2,B1
Zoom in of CAN-FD bus
with decoding data
Zoom2: M1
Zoom in Chirp pulses
D: 000000C1h
ID
Decode results B 1
Frame State Start Type ID type ID value [hex] Standard DLC NDB [dec] Values Sym
1 No ACK 9.54 ms Data 29 bit C1 CAN-FD 14 48 [hex] 02 01 04 03 0 ---
2 No ACK 10.526914 m Data 29 bit D1 CAN-FD 8 8 [hex] 01 00 00 00 7 ---
3 No ACK 11.543546 m Data 29 bit D1 CAN-FD 15 64 [hex] 34 00 09 00 0 ---
4 No ACK 12.542779 m Data 29 bit D1 CAN-FD 15 64 [hex] 32 00 00 00 9 ---
5 No ACK 14.542939 m Data 29 bit D1 CAN-FD 15 64 [hex] F8 00 00 00 2 ---
6 No ACK 15.543254 m Data 29 bit D1 CAN-FD 15 64 [hex] C5 00 01 00 F ---
7 No ACK 16.542693 m Data 29 bit D1 CAN-FD 15 64 [hex] 4D 00 8F FE E ---
Data format Hex
Zoom coupling
Show details
Export
Horizontal
1 ns 1 GSa/s
20 MSa RT
2 ms/div
0 s
Trigger Normal
A: Width Ch1
Level: 33.621 mV
Ch1Wfm1
20 mV/div
0 div 0 V
DC 50Ω BW: 8 GHz
Sample
Ch2Wfm1
500 mV/div
0 div 1.68 V
DC 50Ω BW: 1.5 GHz
Sample
Math1
Scale: 20 mV/div
Max: 180 mV
FIR(lowpass,abs(Ch1),1e6...
SerBus1
Type: CAN / CAN-FD
Data: C2W1
Meas Group 1
Frame to frame 986.91 µs
Trig to frame 9.54 ms
Bus idle 62.782 %
Meas Group 2
Pulse count 64
Pulse train 4.1459 ms
From start of 1st chirp until start of 1st CAN-FD frame
File Horizontal Trigger Vertical Math Cursor Meas Masks Analysis Display

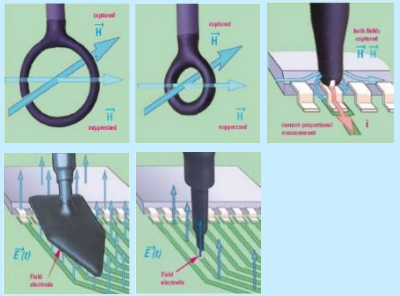
EMI DEBUGGING: EQUIPMENT



R&S ® RTO

Near-field sniffer Probes R&S ® HZ-15

E- and H-field



30 MHz – 1 GHz

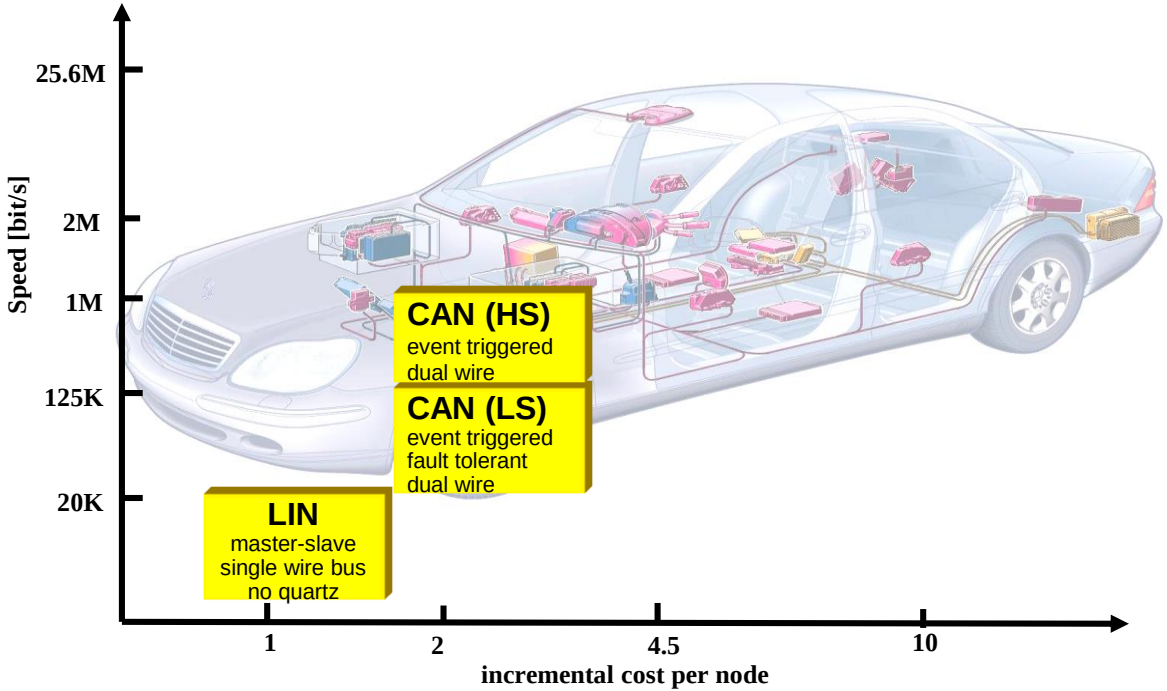
Can be used down to 100 kHz

Optional:
R&S ® HZ-16
Preamplifier

SERIAL BUS CAN/LIN IN THE AUTOMOBILE

ROHDE&SCHWARZ

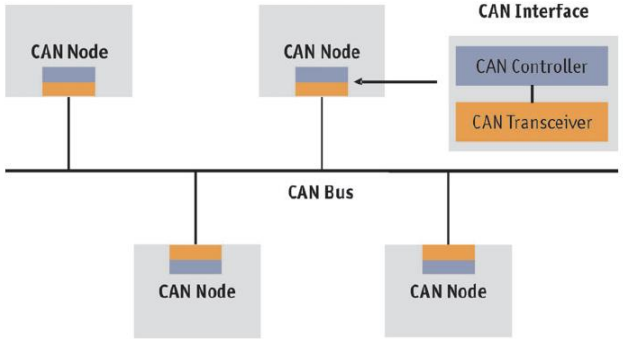
OVERVIEW – PERFORMANCE VS. COST/COMPLEXITY



CAN – INTRODUCTION (I)

- Controller Area Network (CAN) is ISO standard (ISO 11898) for serial communication
- Developed 1980s by BOSCH for automotive applications
  - Also found in industrial and medicine applications
- CAN standard defines
  - Physical layer
    - Low-speed (max. 125 kbps), high-speed (max. 1 Mbps)
    - Driver/receiver characteristics
    - Bit enconding/decoding and synchronization
  - Data-link layer
    - Message types
    - Arbitration rules for bus access
    - Methods for fault detection and fault confinement

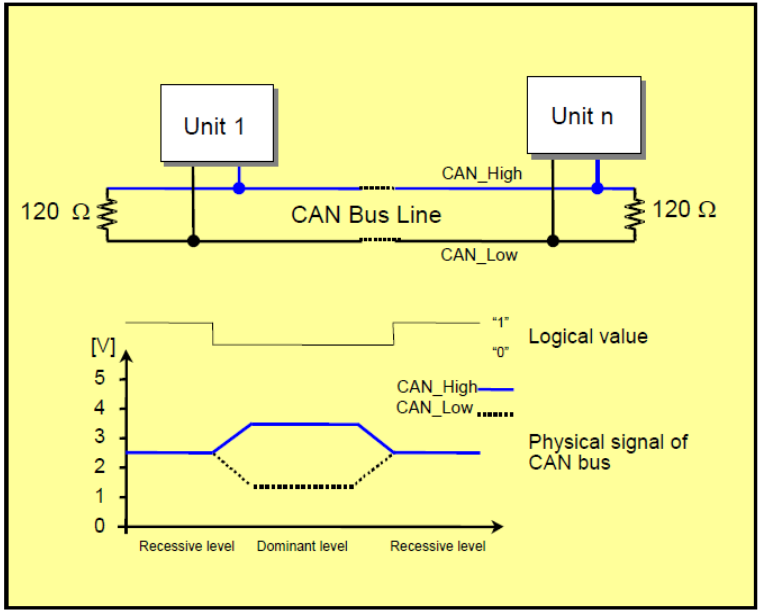
CAN – INTRODUCTION (II)



- Asynchronous Serial Bus
  - Transfer rate: 10 kbps to 1 Mbps
- Multi-master / Broadcasting concept
- Absence of node addressing
  - Message identifier specifies contents and priority
  - Lowest message identifier has highest priority
- Non-destructive arbitration system
  - CSMA for collision detection
- Sophisticated error detection and handling
  - Operating 1000 h/year, transfer rate 500 kbps and mean bus load 25% yields one undetected faulty frame in 4000 years

CAN – BUS LEVELS

- Differential signaling
  - CAN_High, CAN_Low
  - 120 Ohm termination
- Wired-AND bus logic
  - Dominant (logic 0) and recessive (logic 1) levels



Note: Picture depicts levels and bus connection for high-speed CAN. Same principle applies for low-speed CAN but levels and termination resistors slightly different.

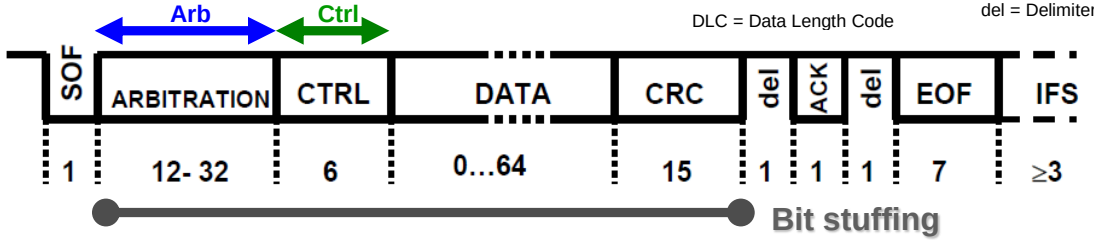
CAN – OVERVIEW OF FRAME TYPES

- Data frame
  - Data transmission
- Remote frame
  - Remote data request
- Error Frame
  - Issued by any bus node on detecting bus error
    - Frame content (CRC error)
    - Bit timing inconsistency (Bit stuffing error)
    - Frame structure inconsistency (Form error)
    - Missing acknowledgement (Ack error)
- Overload frame
  - Issued when one node needs to delay transmission of next frame
  - Overload frame = Error frame that starts just after last successfully transferred Data/Remote frame

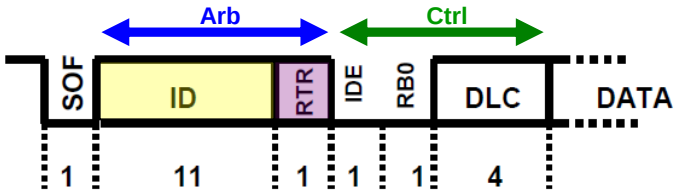
CAN – DATA / REMOTE FRAME

SOF = Start of Frame
RTR = Remote Transm. Request
SRR = Substitute Remote Requ.
IDE = Identifier Extension
RB0/1 = Reserved bits
DLC = Data Length Code

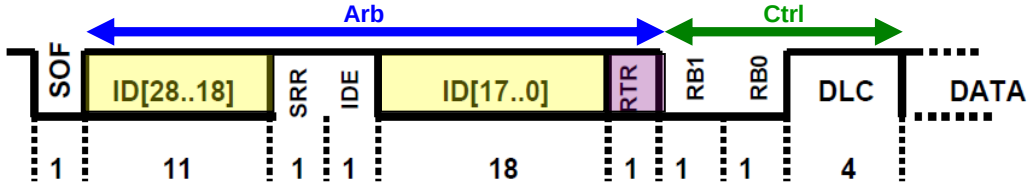
CRC = Cyclic Redundancy Check
ACK = Acknowledge
EOF = End of Frame
IFS = Inter Frame Spacing
del = Delimiter



Standard format



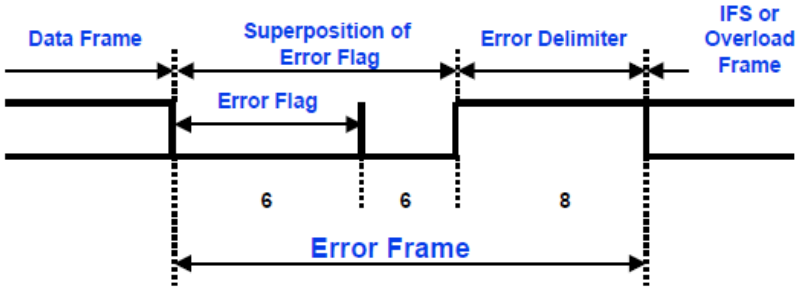
Extended format



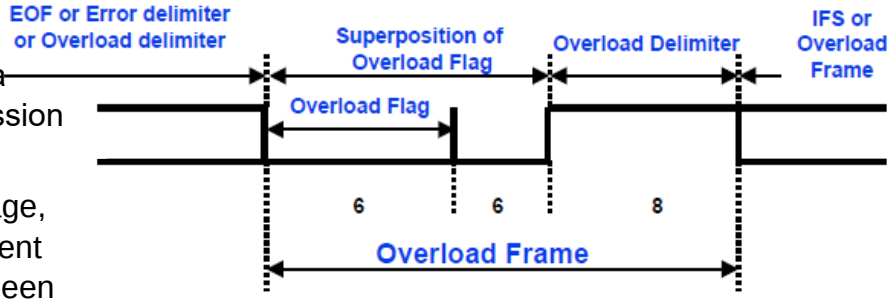
Remember: Remote frames always lack data field even when DLC > 0

CAN - ERROR / OVERLOAD FRAME

- Error Frame
  - Issued by any bus node on detecting bus error
  - Interrupts current message transmission
  - Sender repeats message



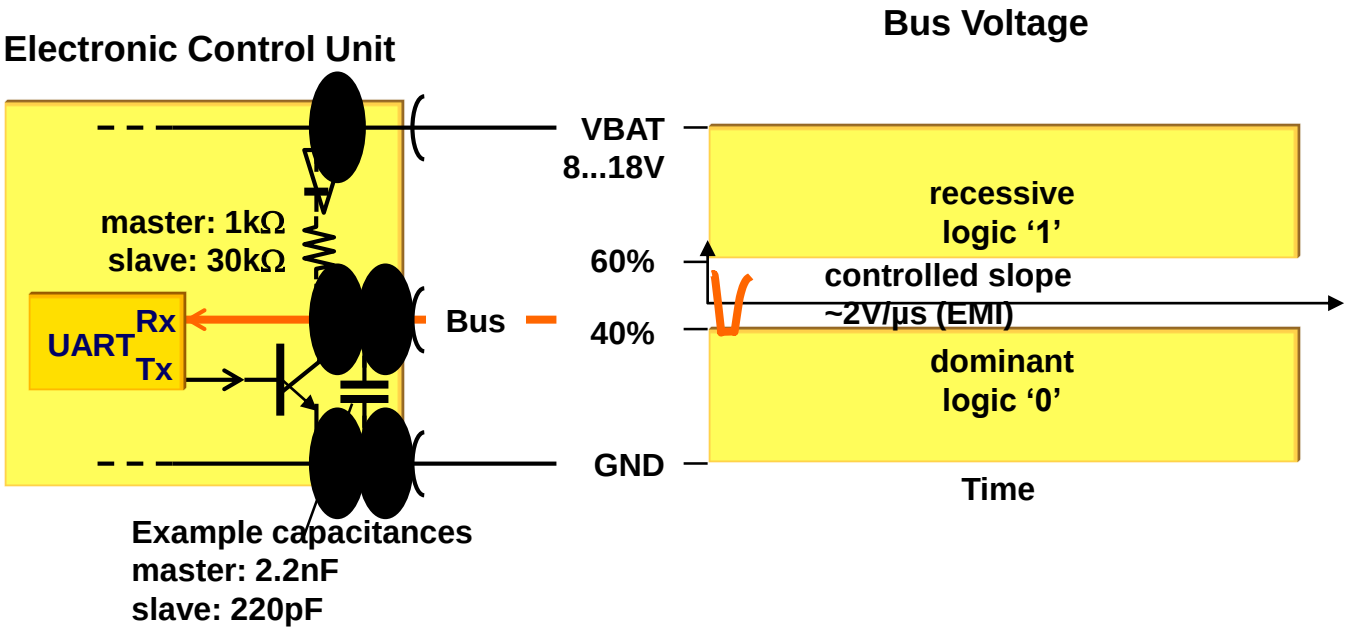
- Overflow Frame
  - Node suffering from “data overflow” delays transmission of next frame
  - Does not interrupt message, overflow frame shall be sent only after message has been completely transmitted



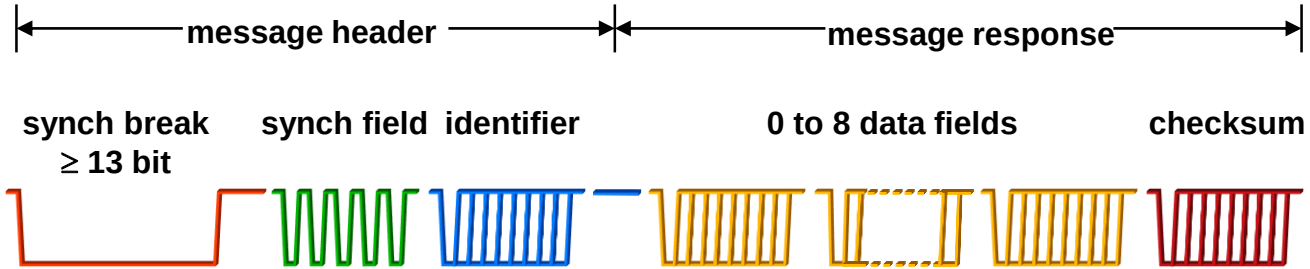
LIN – OVERVIEW

- Local Interconnect Network (LIN) standard developed by LIN Consortium
  - Several versions coexist: v1.3 (2002), v2.0 (major revision, basis for SAE J2602, 2003), v2.1 (clarifications, diagnostics added, and more, 2006)
- LIN provides cost-efficient communication where bandwidth and versatility of CAN is not required
  - Mirror, window lift, door lock, air conditioning, windshield wipers, turning light...
- Low cost single-wire implementation
- Speed up to 20 Kbit/s
- Single Master / Multiple Slave communication
- Low cost silicon implementation based on UART interface hardware
- Self-synchronization without crystal or ceramics resonators in slave nodes
- Only very basic error detection,
  error handling happens at application code level

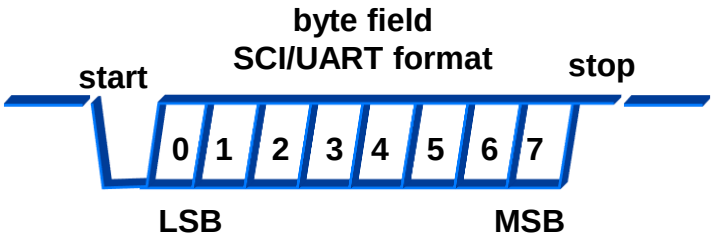
LIN – PHYSICAL INTERFACE



LIN – MESSAGE FRAME (I)



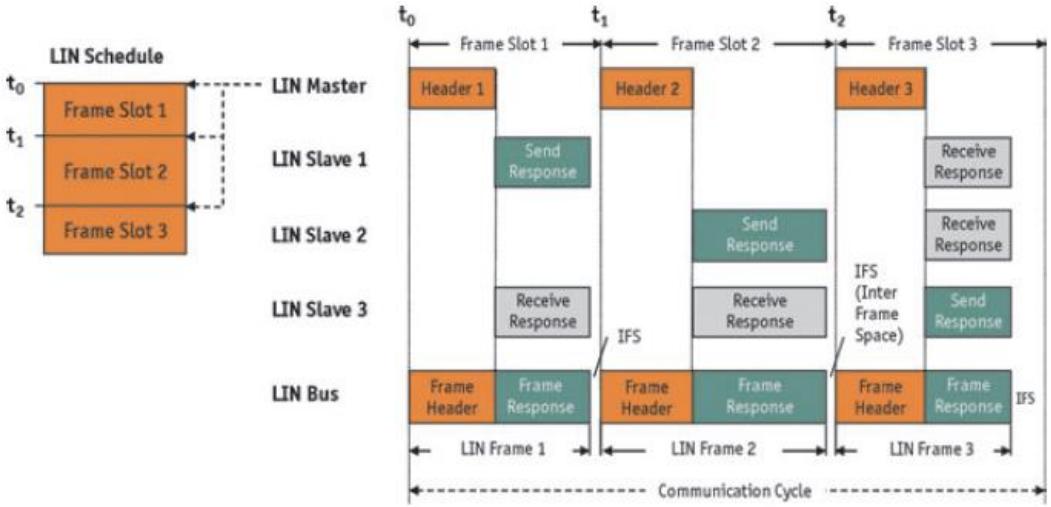
- Break field
  - Determines start of frame
- Synch field
  - Toggling pattern (55h) for synchronization of slave clock to master clock



LIN – MESSAGE FRAME (II)

- Identifier
  - Sent to the master to all LIN nodes
  - 64 different values (6 bits)
    - Values 60 (0x3C) and 61 (0x3D) carry diagnostic and configuration data
    - Values 62 (0x3E) and 63 (0x3F) reserved for future use
  - Protected Identifier: ID + 2 Parity bits (8 bits altogether)
- Data
  - Bytes transferred LSB-first
  - Data entities longer than one byte are transferred Little-Endian
    - Example: 16 bit value „0x0123“ transferred as byte sequence „0x23 0x01“
- Checksum
  - Classic checksum: carried over data bytes only (LIN v1.x)
  - Enhanced checksum: carried over identifier and data bytes (LIN v2.x)
  - Exception: Identifiers 60 (0x3C) and 61 (0x3D) always use Classic checksum

LIN – MASTER / SLAVE COMMUNICATION



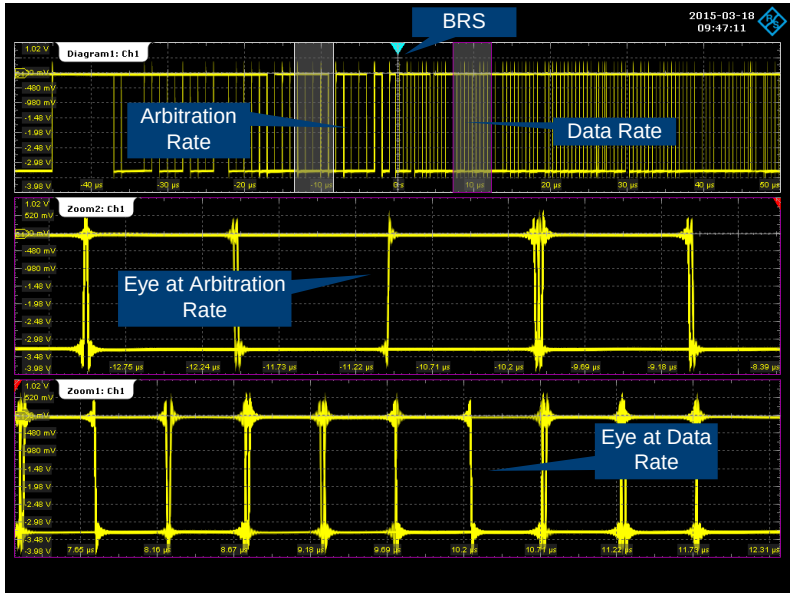
- All LIN nodes have a slave task to participate in the communication
- One LIN node has Master Task for controlling the LIN communication
  - Sends frame header (synchronization + message ID)
  - Allocates time for slave response (up to 40% more than nominal duration)
  - Processes the LIN schedule
  - Handles most of (if not all) of error detection, error recovery and diagnostics

EASY ACCESS VIA THE APP-COCKPIT

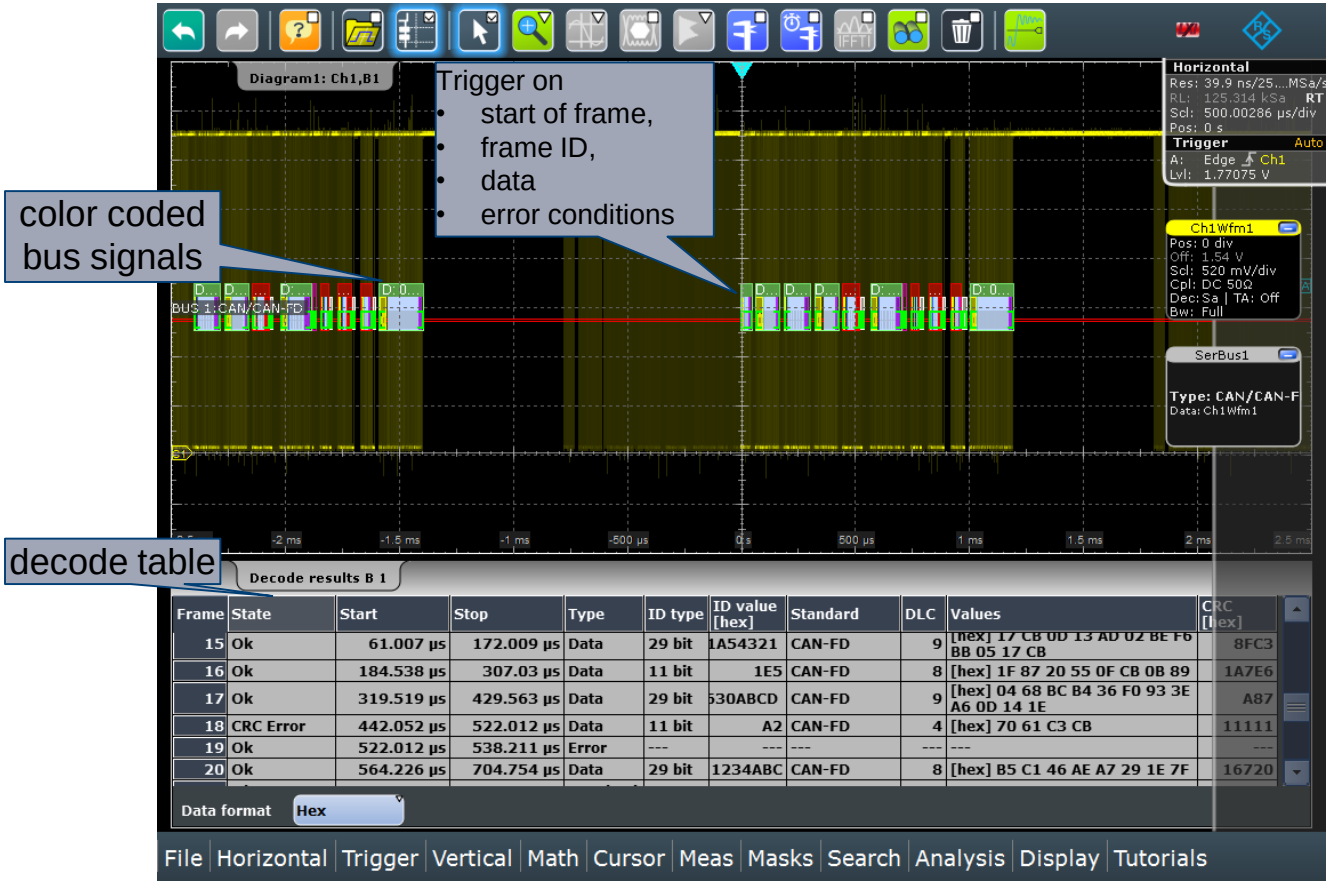
DEBUGGING WITH EYE MEASUREMENT

- Eye measurement help to identify signal problems like runts or glitches
- CAN has two data rates- so a simple eye does not help
- CAN FD eyes need to be separated between Arbitration Rate and Data Rate

With the RTO K option this can be achieved by triggering on BRS bit

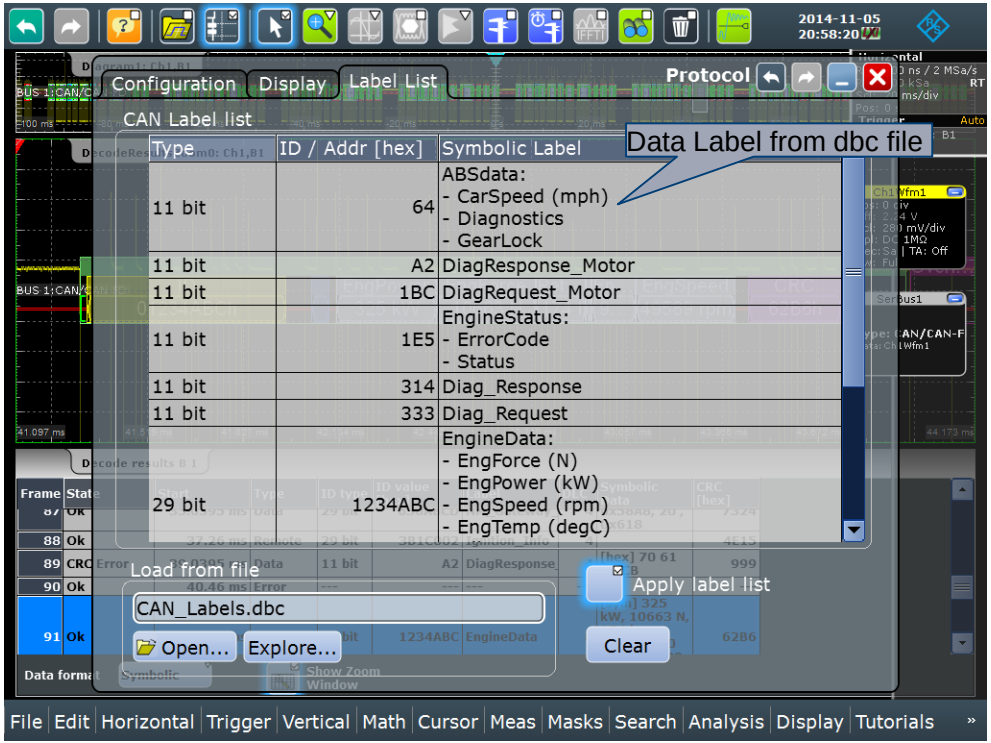


RTP/RTO6 CAN/CAN-FD TRIGGER AND DECODE

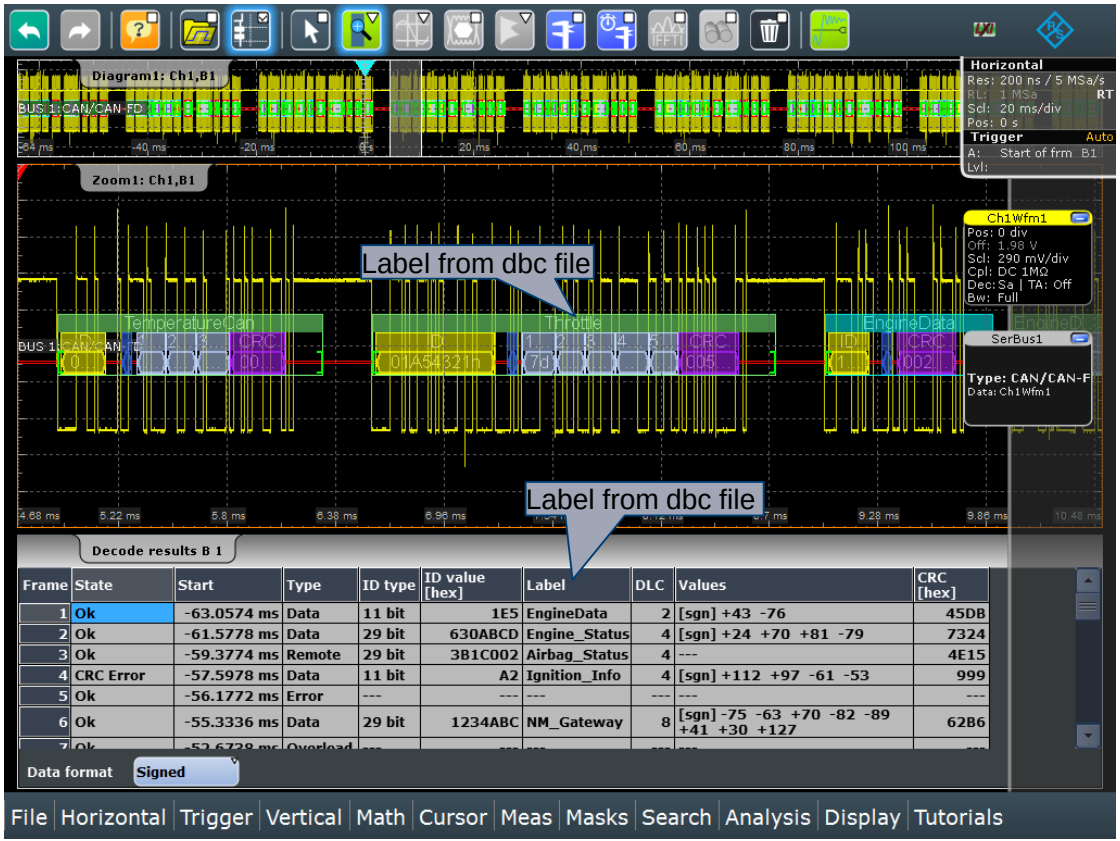


CAN/CAN-FD SETUP DIALOG

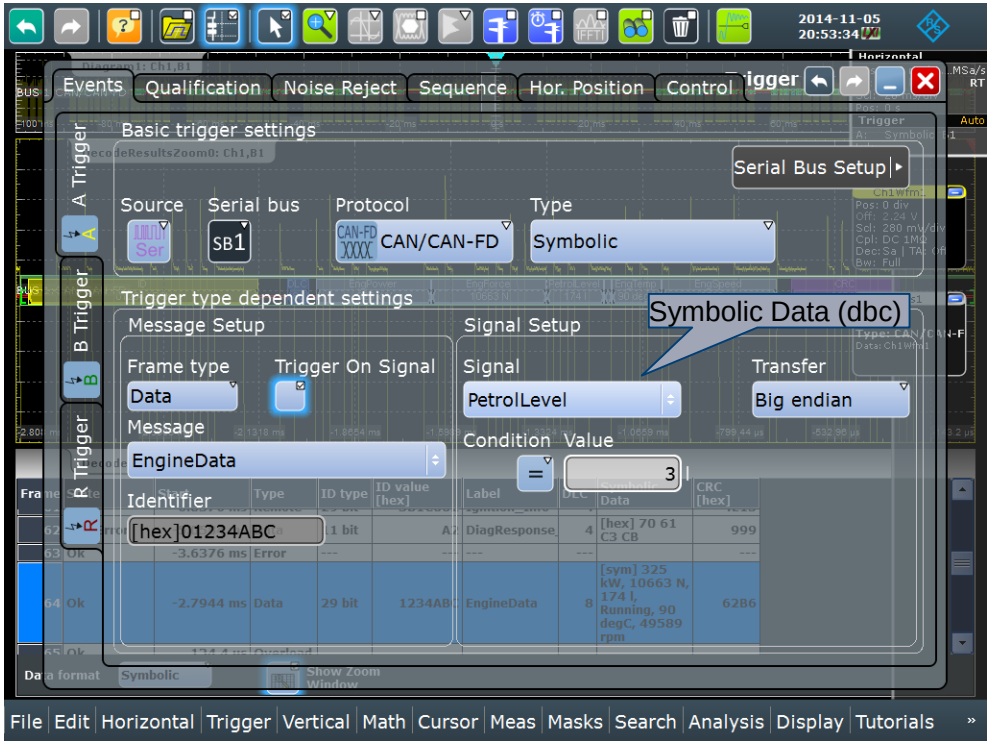
CAN-DBC FILE SUPPORT I – IMPORT DBC FILE



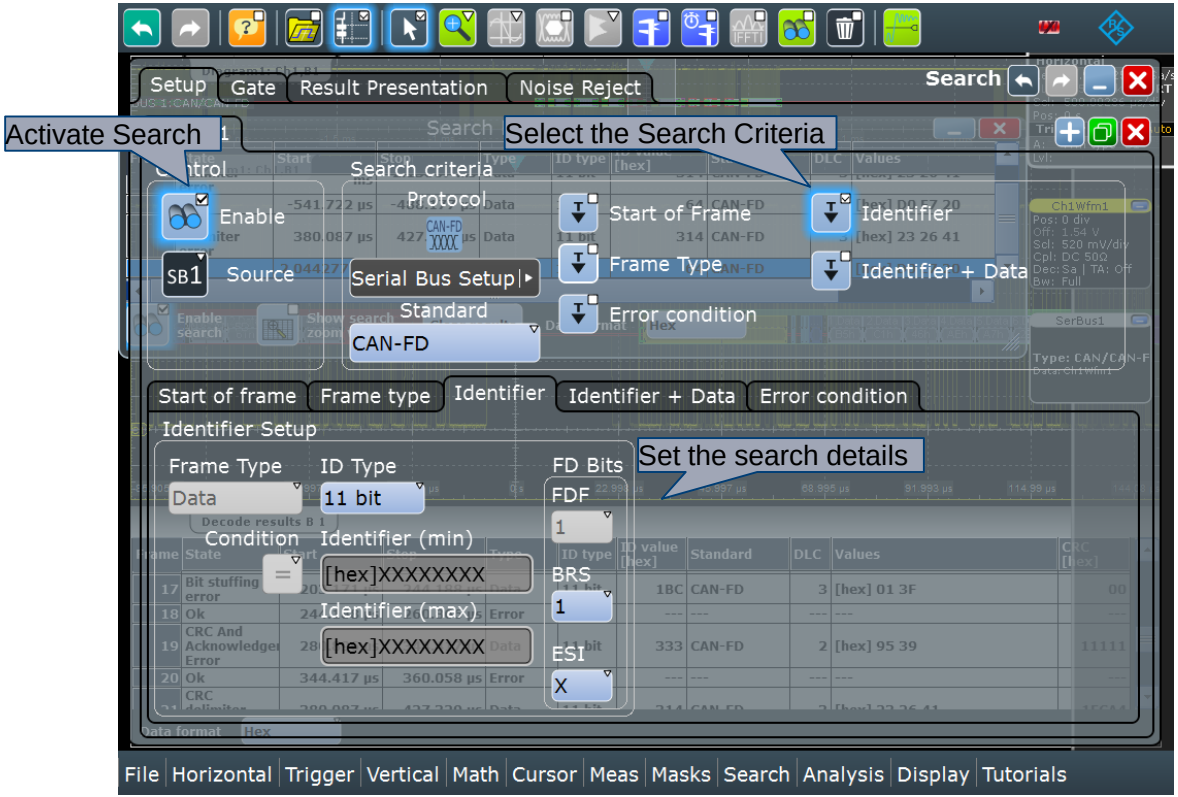
CAN-DBC FILE SUPPORT II – DECODE SYMBOLIC DATA



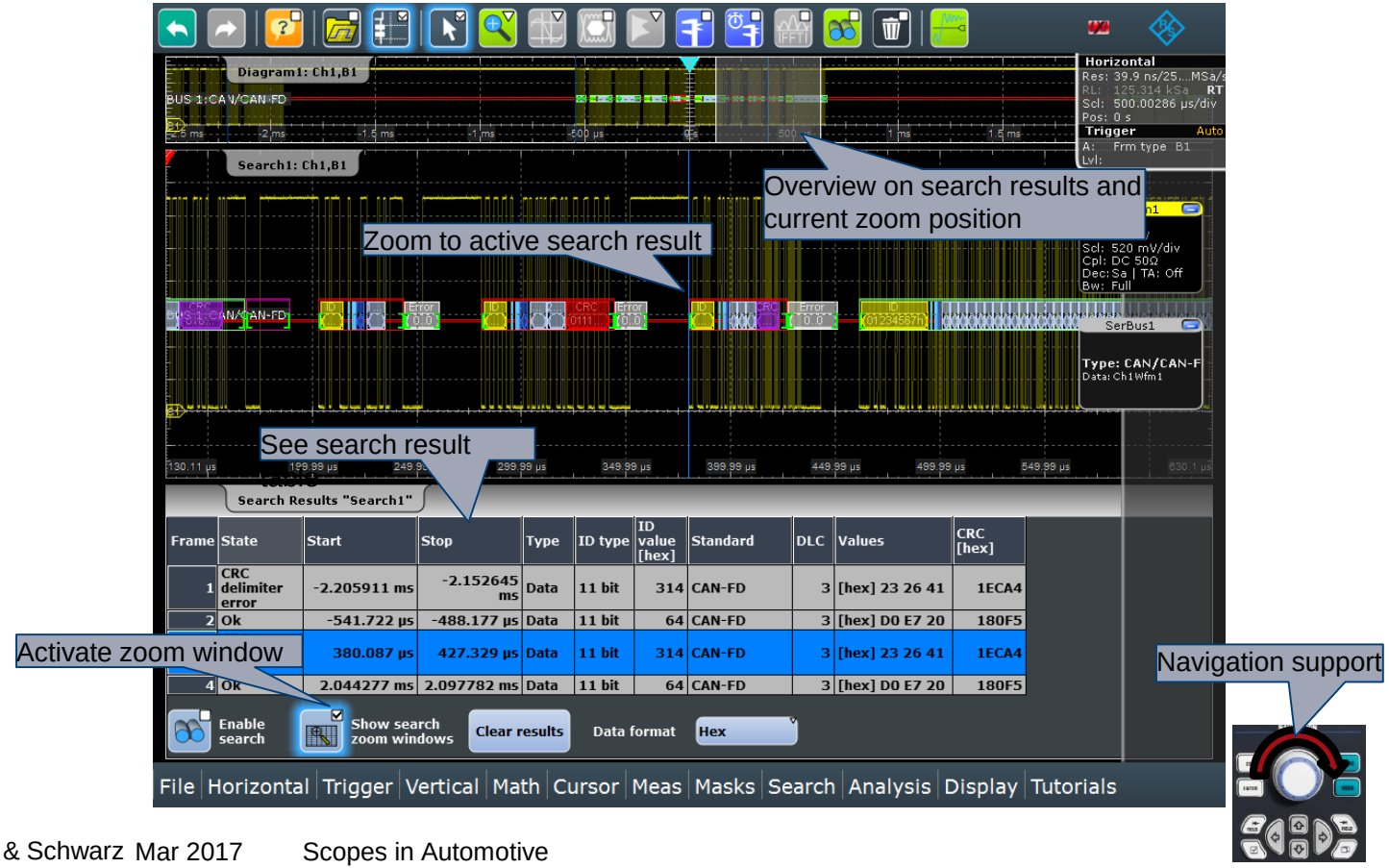
CAN-DBC FILE SUPPORT III – TRIGGER ON SYMBOLIC DATA



POWERFUL SEARCH AND NAVIGATE I



POWERFUL SEARCH AND NAVIGATE II



AUTOMOTIVE TESTING PHY LAYER SUMMARY

	R&S®RTP	Max freq. 16GHz	OA TC8 & OA TC15 Supports speeds up to 10GBASE-T1
	R&S®RTO6	Max freq. 6GHz	OA TC8 & OA TC15 Supports speeds up to 2.5GBASE-T1
	R&S®ZNB	4-port VNA 9kHz – 40GHz	OA TC9, OA TC8 & OA TC15 8GHz VNA sufficient for 10GBASE-T1

Test it! Trust it!