Full Digital Control PFC Development & Design Tips
全數位控制PFC理論與實務

A Leading Provider of Smart, Connected and Secure Embedded Solutions

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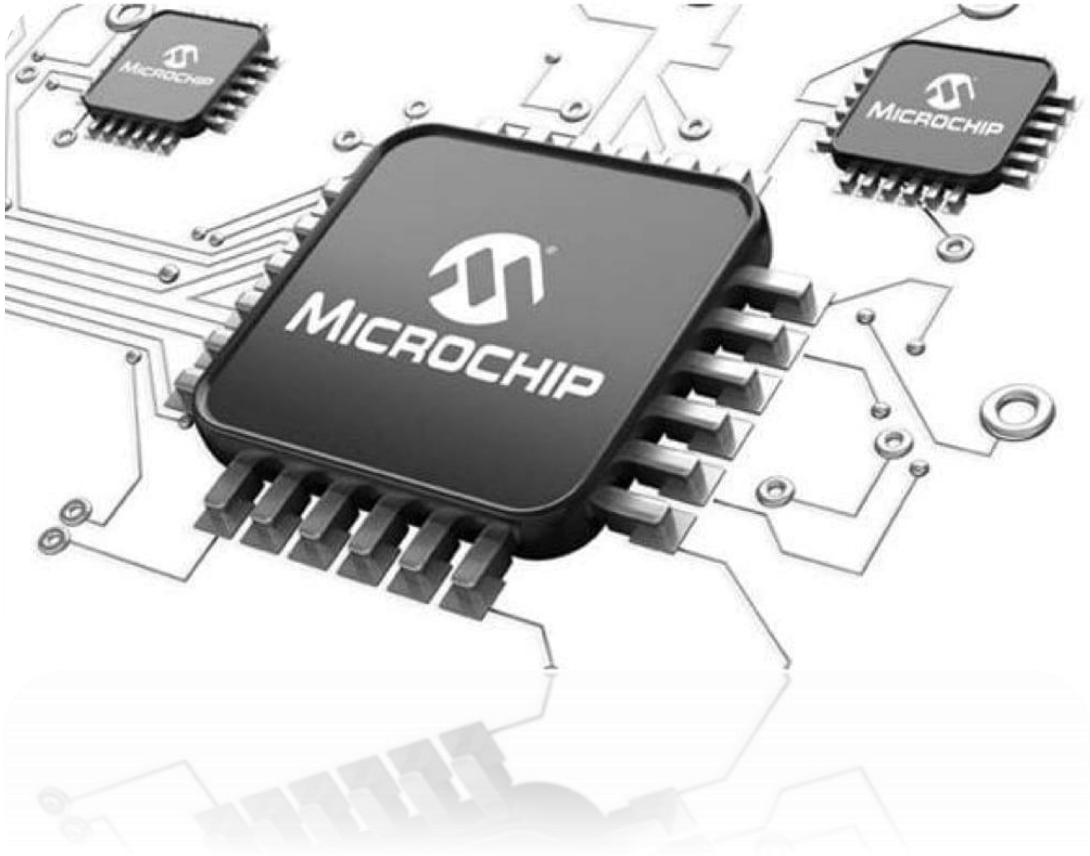
June-25, [redacted]

SMART | CONNECTED | SECURE

Agenda

- **Power Factor and its Significance**
- **How to Achieve Power Factor Correction**
- **Overview of Different Boost Type PFC Designs**
- **Digital PFC Control Algorithm**
- **Design Issue and Tips**



What is Power Factor?

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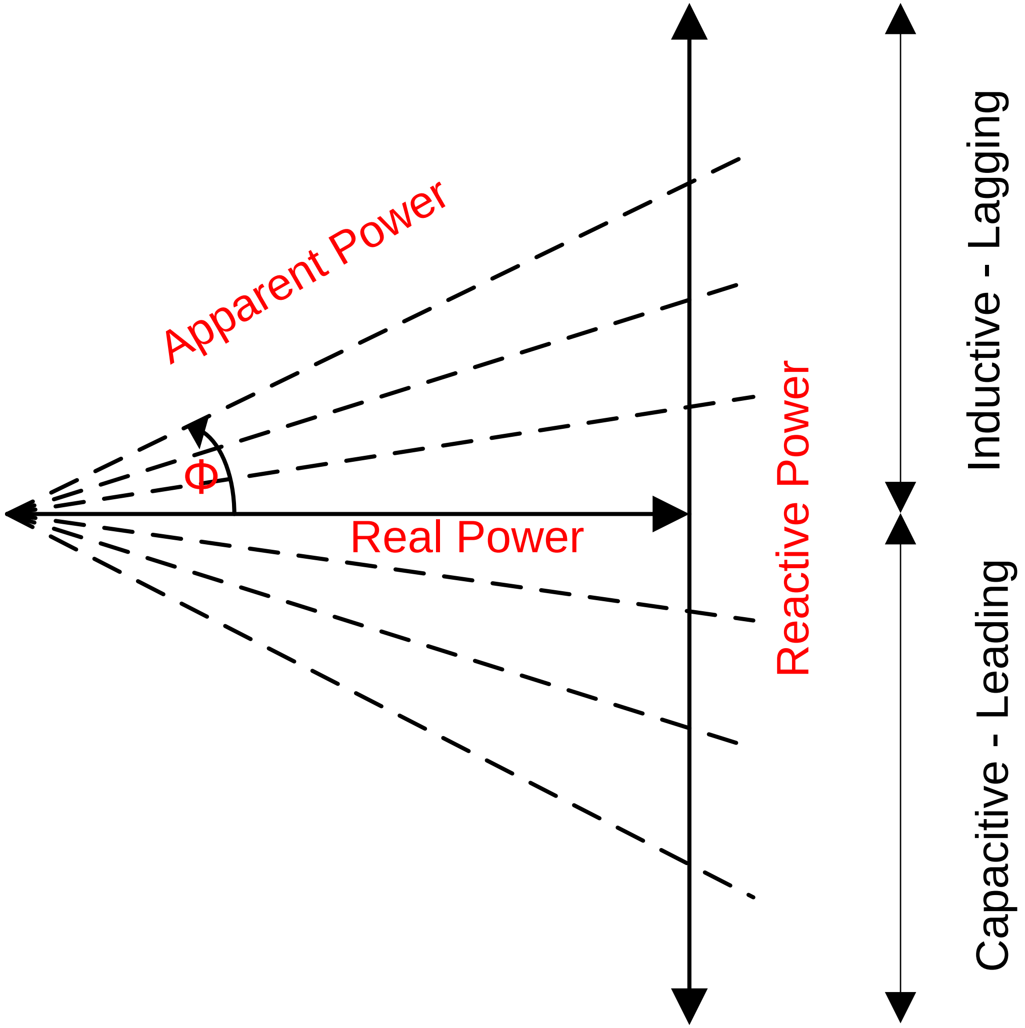


$$PF = \frac{Real\ Power}{Apparent\ Power} = \cos\emptyset$$

Applies for ideal sinusoidal waveforms for both voltage and current

What is Power Factor?

- **Power factor for an AC powered system is defined as the ratio of the real power flowing to the load, to the apparent power in the circuit.**

$$PF = \frac{Real\ Power}{Apparent\ Power}$$

- **PF is a dimensionless number between 0 and 1.**
- **Power Factor is unity (1) when the voltage and current are in phase.**
- **For two systems with the same real power, the system with the lower PF will have higher circulating currents (higher apparent power).**

Examples of PF Degradation

Case 1

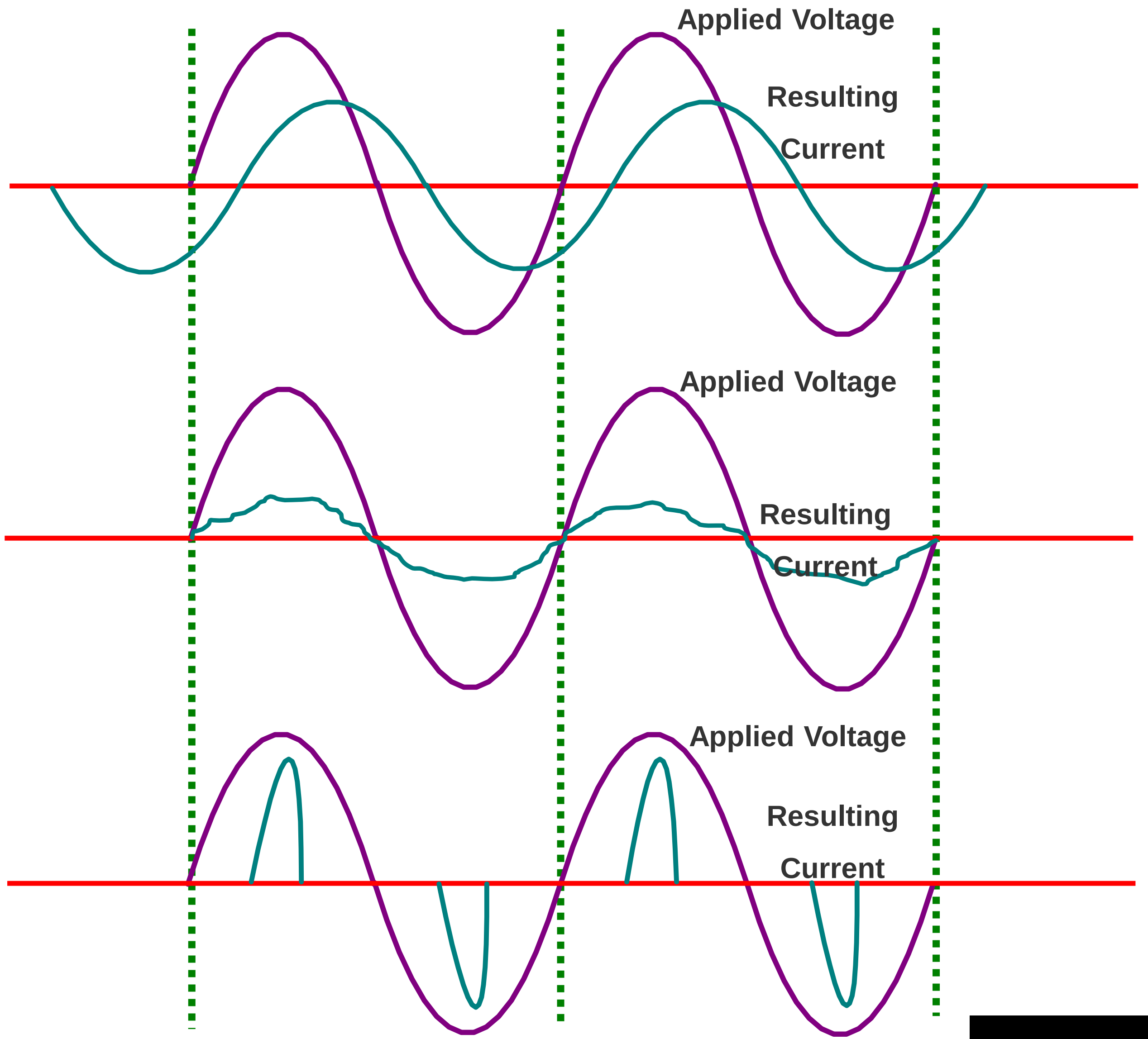
Sinusoidal Current with phase shift

Case 2

Semi-Sinusoidal Current with no phase shift

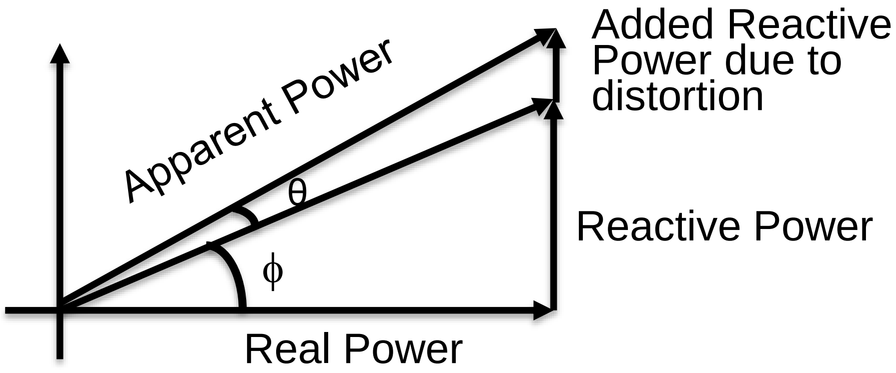
Case 3

Non-Sinusoidal Current with phase shift



Measuring Power Factor

- **Displacement factor = Real Power / apparent power = cos ϕ**



→ Not present when load is linear

- **Distortion Factor accounts for non-sinusoidal currents**

$$\text{Power Factor} = \underbrace{\cos\phi}_{\text{Displacement factor}} * \underbrace{\sqrt{\frac{1}{1 + (I_2 / I_1)^2 + (I_3 / I_1)^2 + \ldots\ldots}}}_{\text{Distortion factor}} = \frac{\cos\phi}{\sqrt{1 + THD^2}}$$

THD: Total Harmonic Distortion

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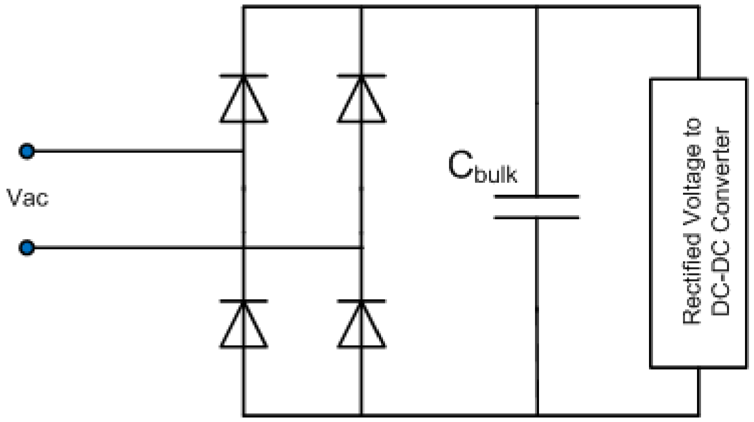
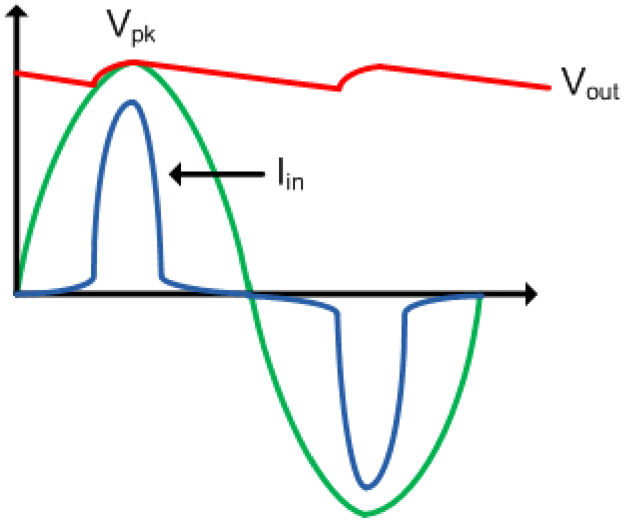
How to Achieve Power Factor Correction

SMPS Without PFC

- **Off-line switch-mode power supply**

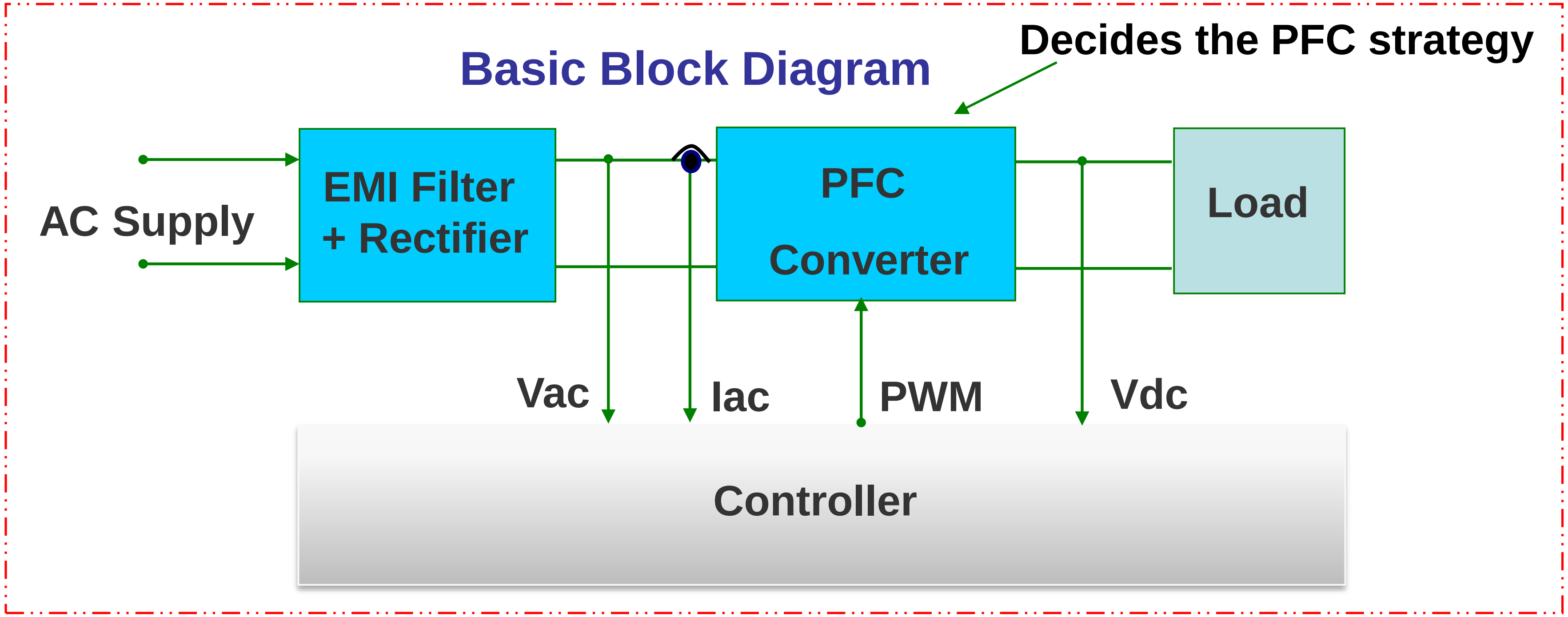




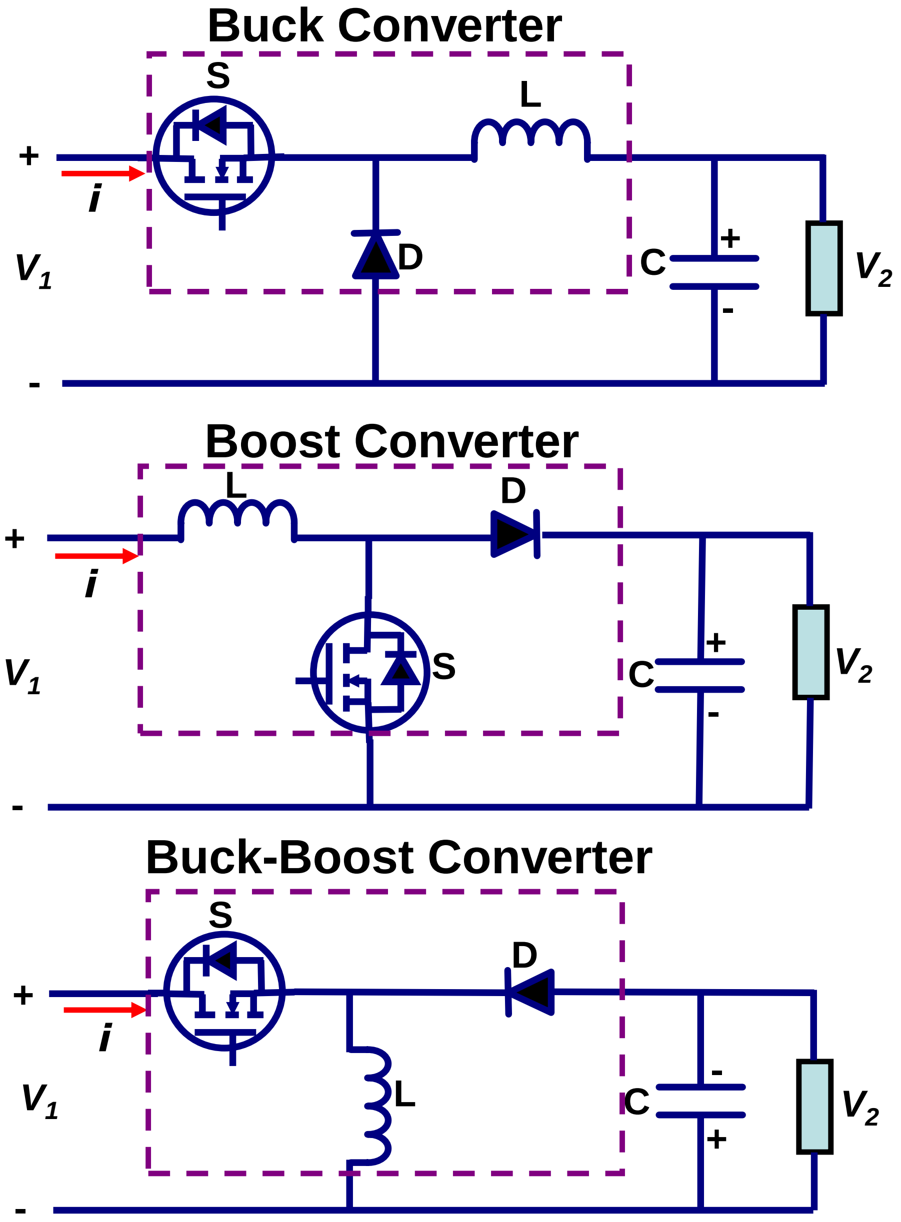
- C_{bulk} must be large enough to reduce voltage ripple and meet specified holdup requirements
- Restoring capacitor current occurs near the peak of AC input ($V_{ac} > V_{out}$), resulting in large current spikes

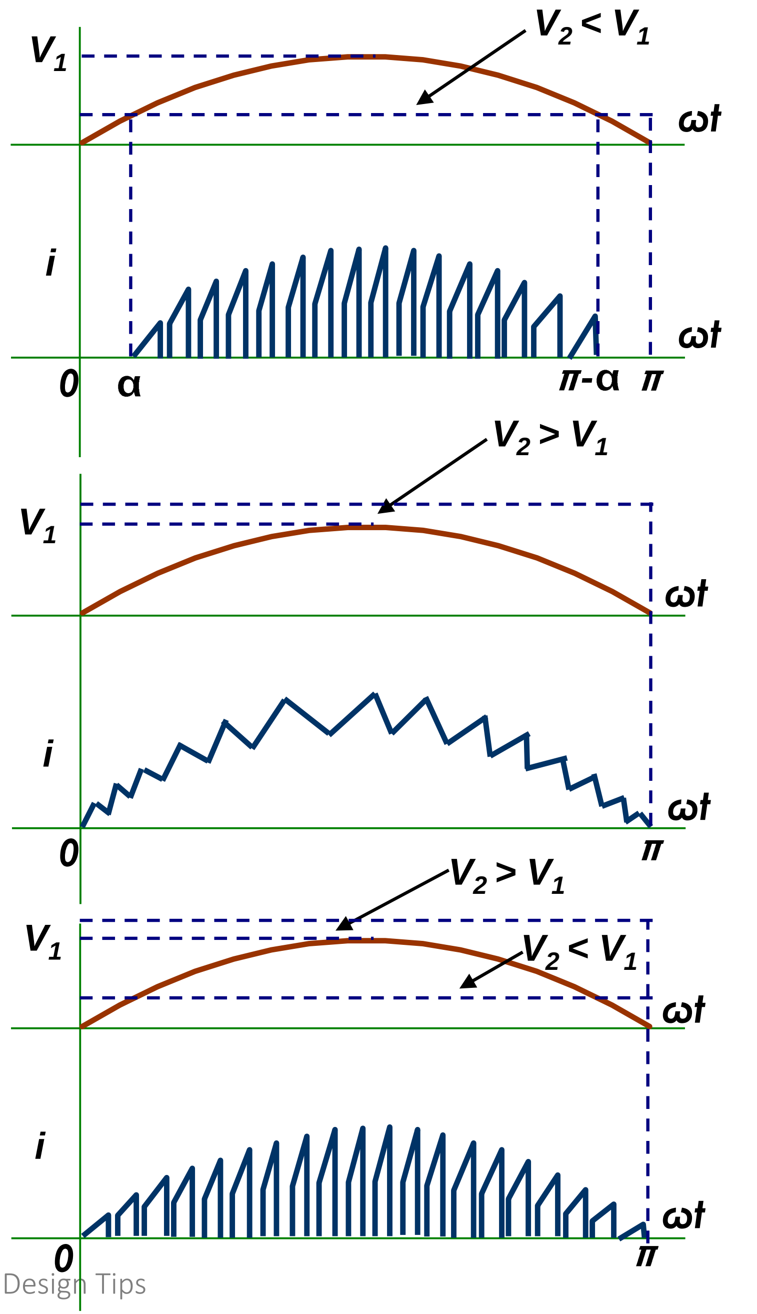
Active PFC Block Diagram

- **Typical Active PFC Requirements:**
  - Feedback Voltage
  - Input Voltage/Current
  - Compensation network (controller)
  - PWM



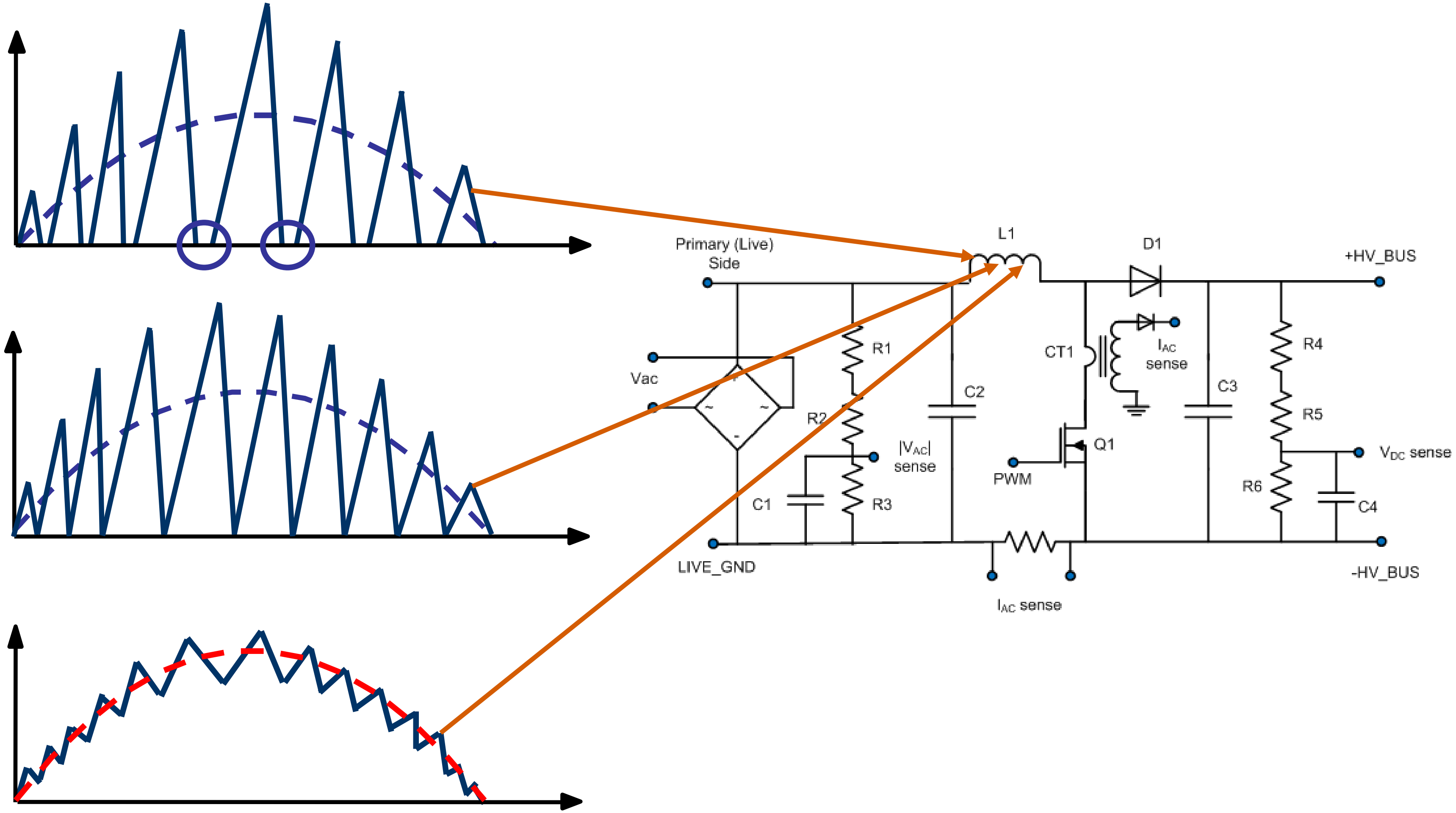
Active PFC Solutions





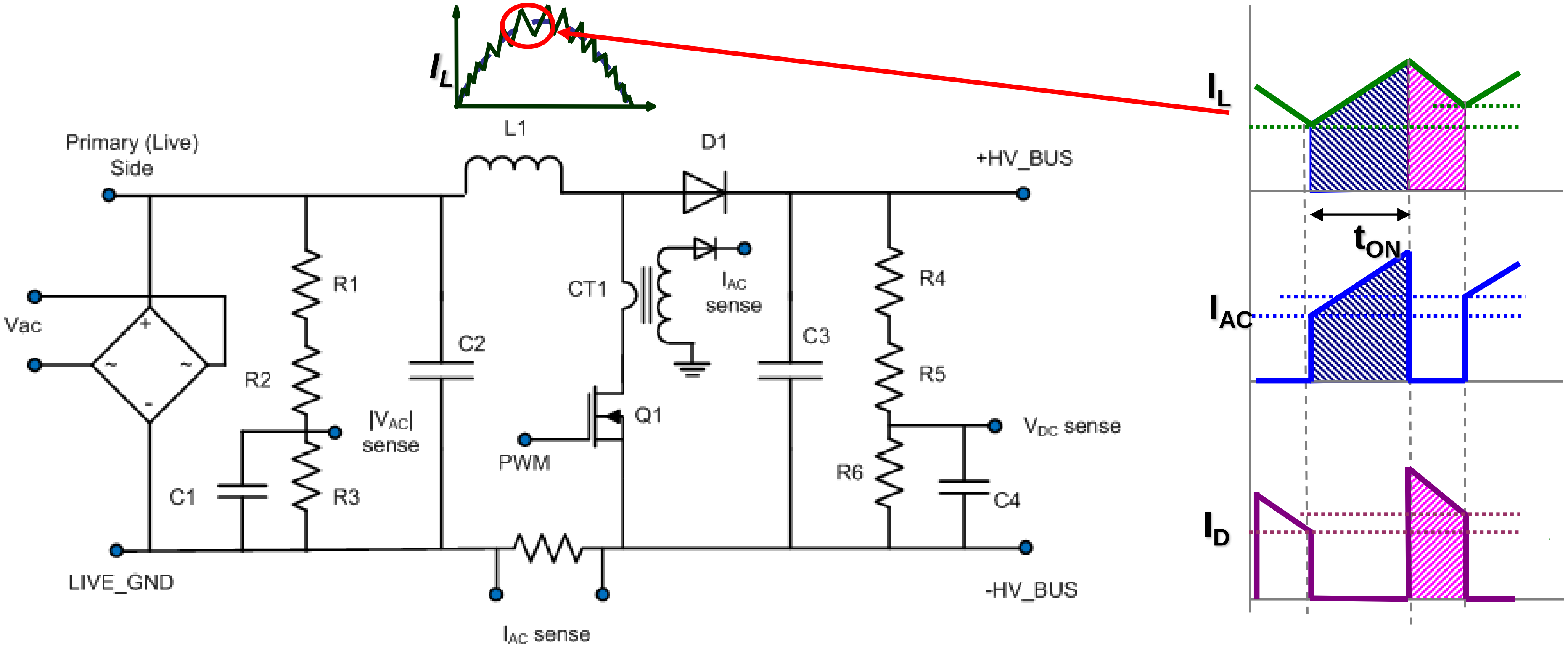
Boost Operating Modes

- **DCM, Discontinuous Conduction Mode**
- **BCM, Boundary (Critical) Conduction Mode**
- **CCM, Continuous Conduction Mode**



Active PFC Example

- **Average Current Mode Control**
  - The average current through the inductor is made to follow the input voltage profile to improve Power Factor and minimize current harmonics



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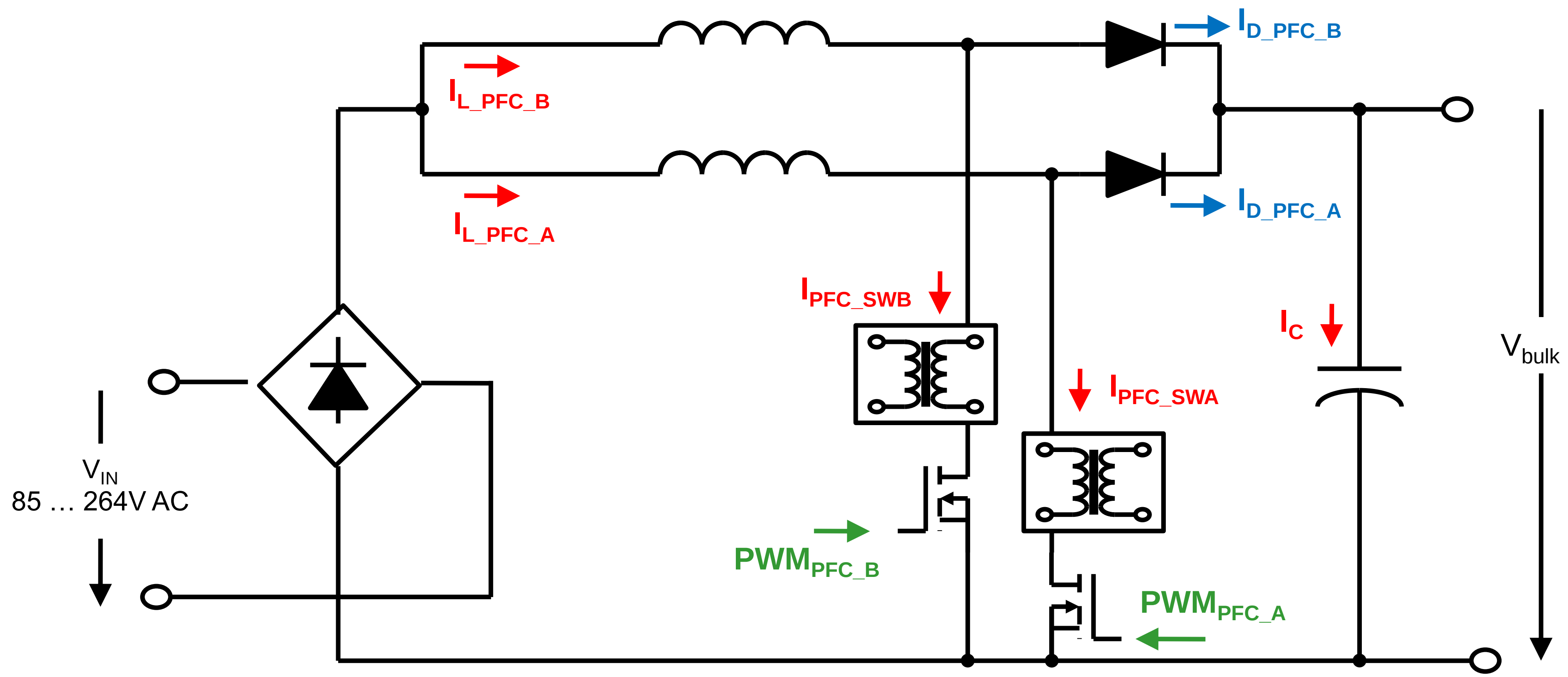
Overview of Different Boost Type PFC Designs

Interleaved PFC

- **Two independent boost converters connected in parallel operating 180° out of phase**
- **Great for high power applications with size constraints**



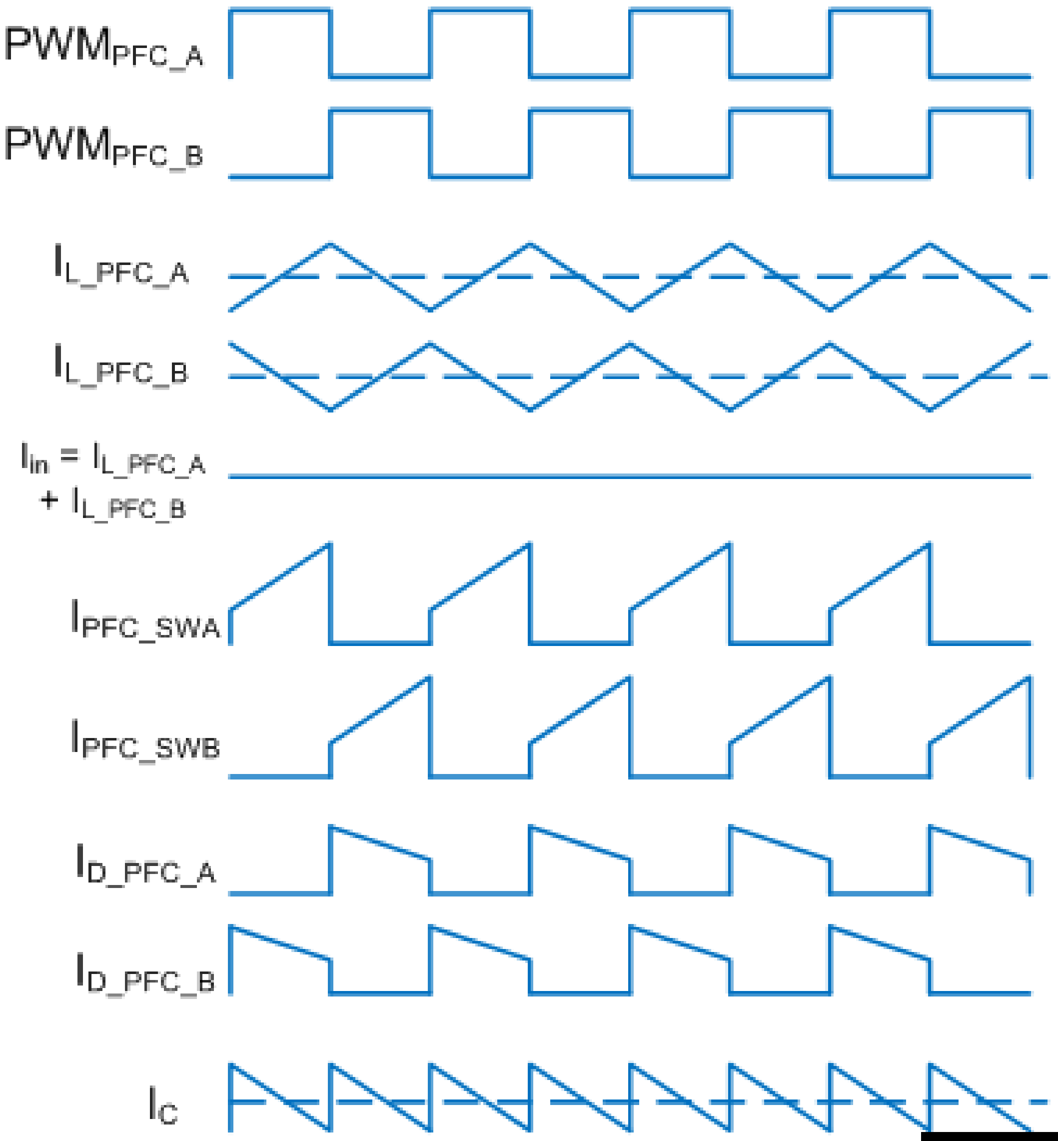
Benefits of IPFC

- **Inductor ripple currents are out of phase and tend to cancel each other out. Best current ripple cancellation occurs at 50% duty cycle.**

- **Inductors stored energy requirement is ½ that of single phase PFC (reduction in magnetic volume)**

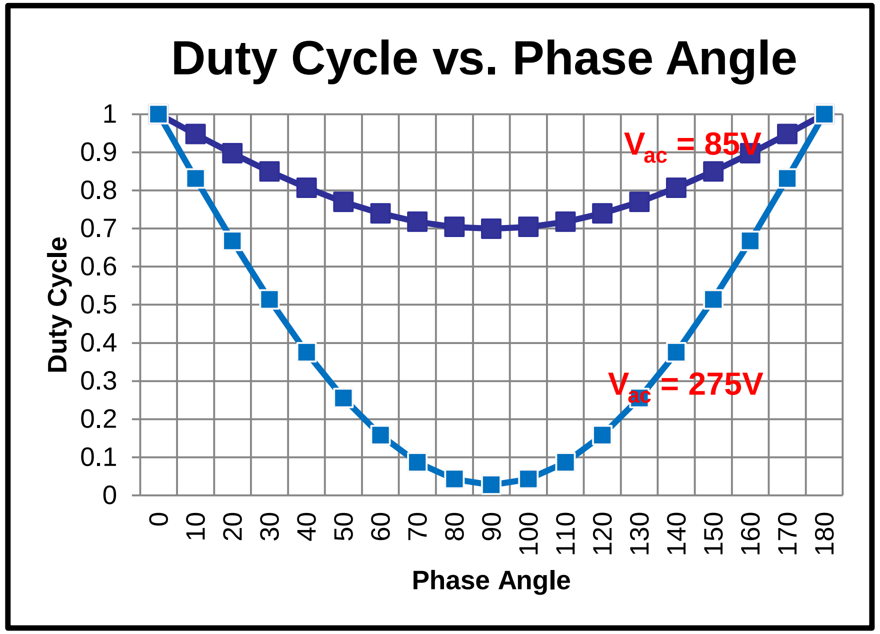
- **Interleaving also reduces the output capacitor ripple current**

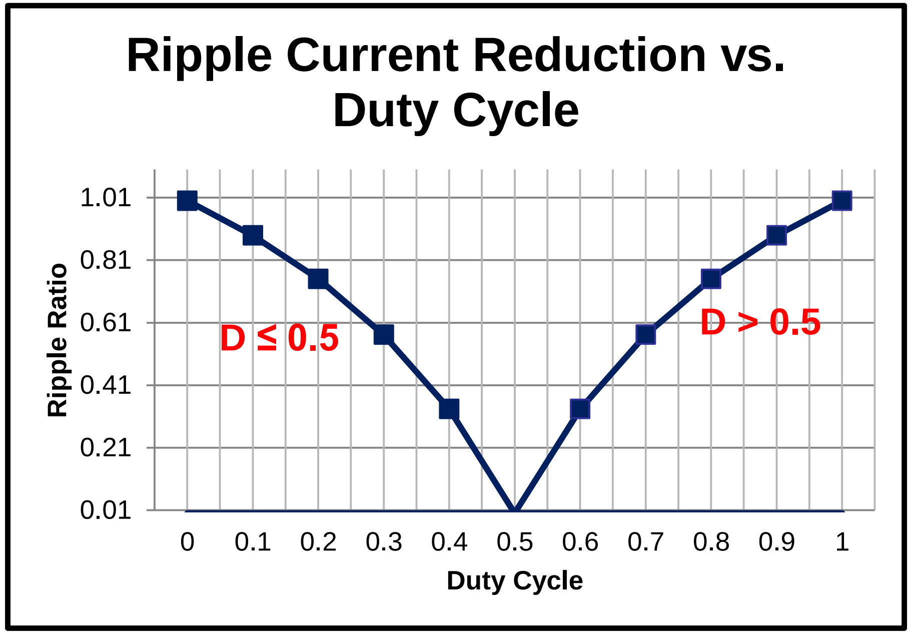
- **Higher efficiency**



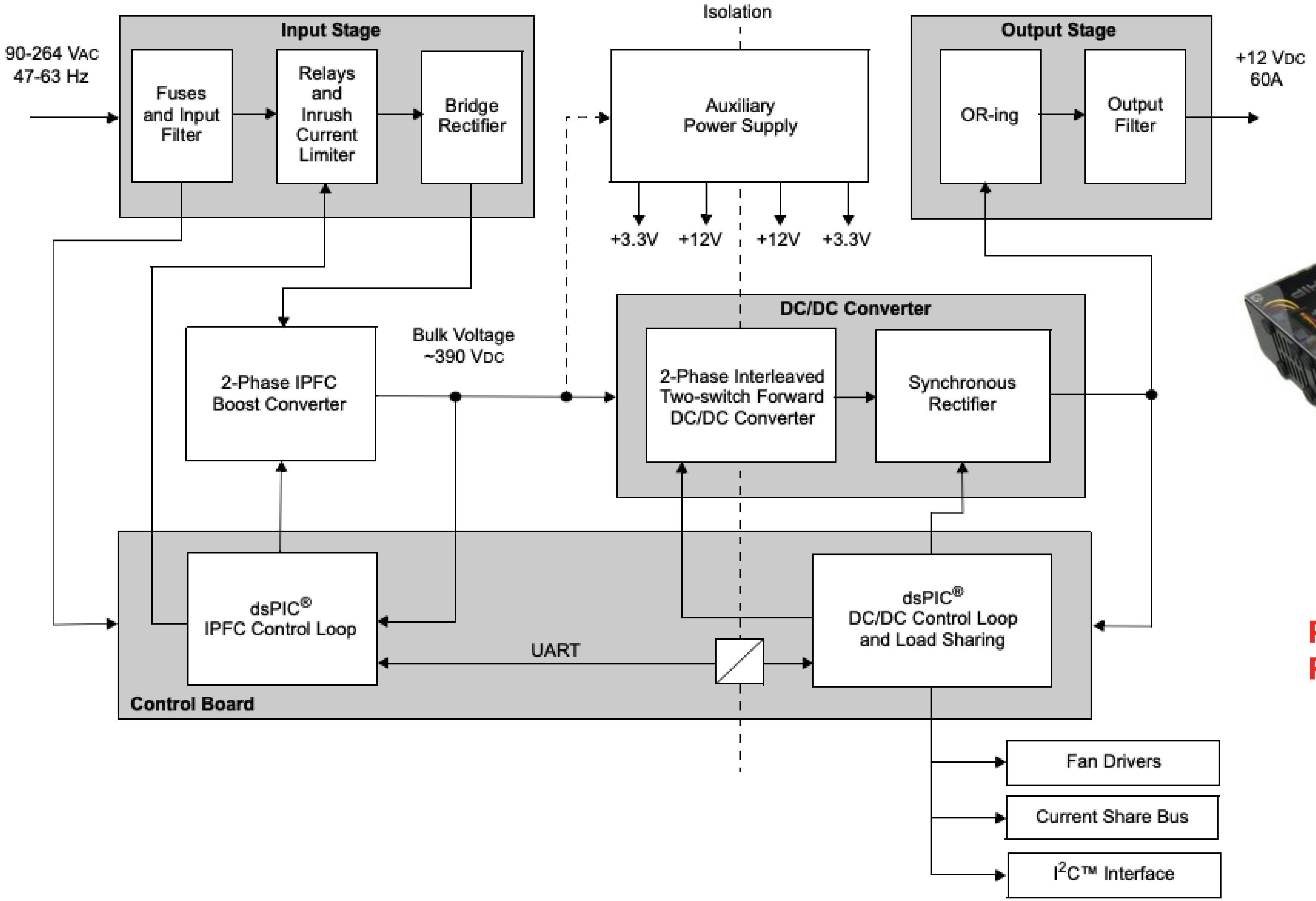
IPFC Ripple Cancellation

- **Maximum ripple current will occur at the peak of the minimum input voltage (85Vac).**
  - Duty Cycle of ~70% yields an input current ripple that is ~60% of the inductor ripple current





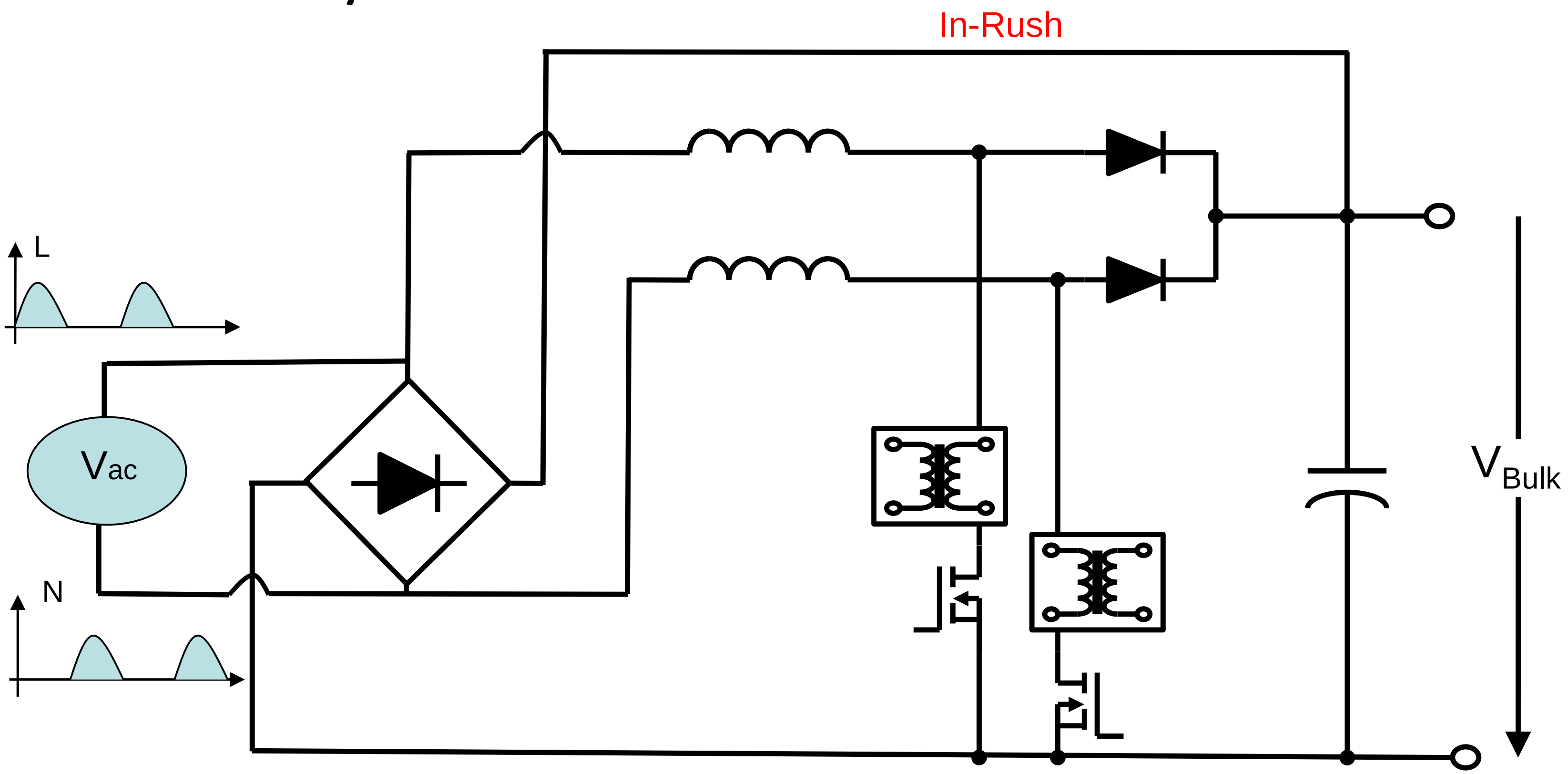
IPFC Reference Design



Platinum-Rated 720W AC/DC Reference Design

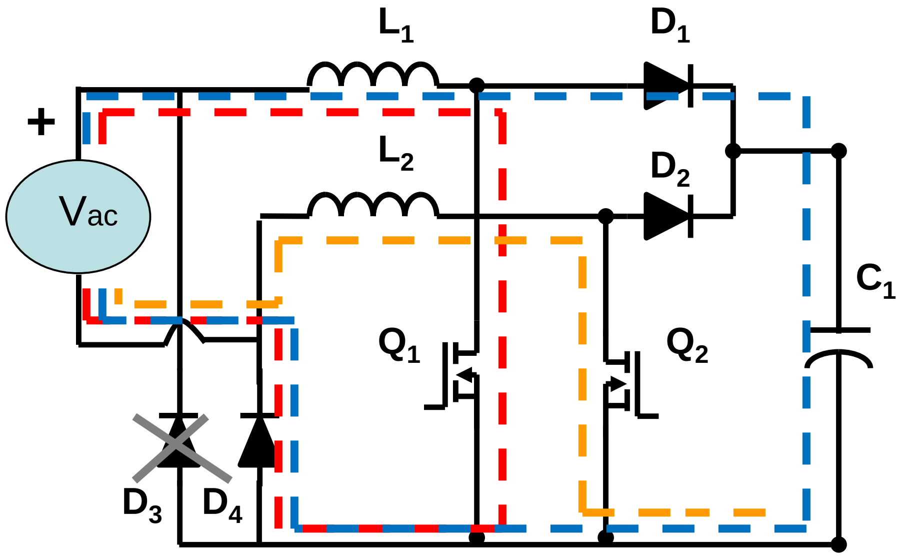
Semi-Bridgeless PFC

- Also known as two/dual phase PFC
- AC input directly connected to Boost Inductors
- Two diodes in bridge rectifier used for In-Rush Current protection at Start-up. Other two diodes link PFC ground to input line
- Both phases can be driven simultaneously or in the case of digital control and to improve efficiency each phase is active when L/N is active

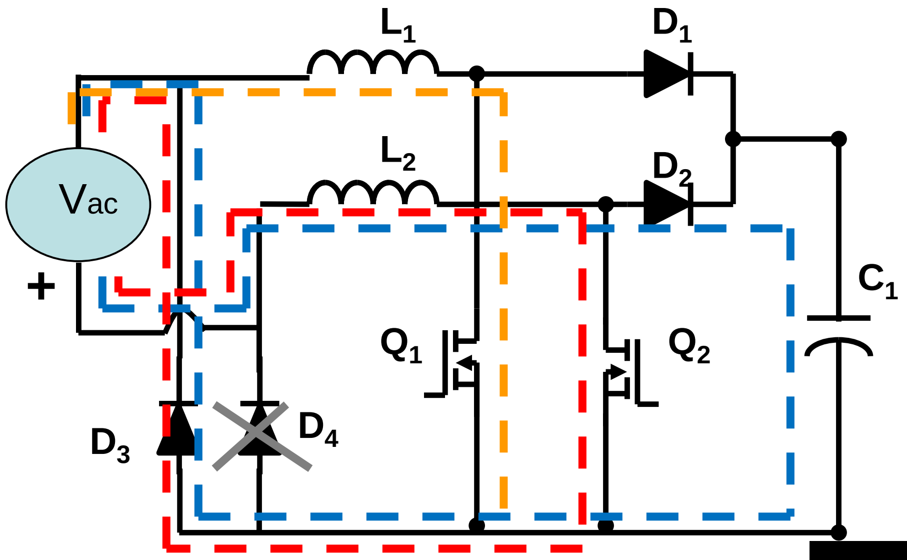


Semi-Bridgeless PFC

- **Case 1: Line Positive**
  - MOSFET Q1 switches
  - Diode D3 Reversed Biased
  - Current returns through D4 **and** through body diode Q2 and L2 (introduces new MOSFET losses)



- **Case 2: Neutral Positive**
  - MOSFET Q2 switches
  - Diode D4 Reversed Biased
  - Current returns through D3 **and** through body diode Q1 and L1



Semi-Bridgeless PFC Efficiency Improvements

- **For universal input voltage range the peak current through the diode bridge occurs at 85Vac.**
- **The total bridge consumes ~2% of the input power at low line and about 1% at high line.**
- **If we eliminate one diode then we could gain ~1% efficiency at low line.**

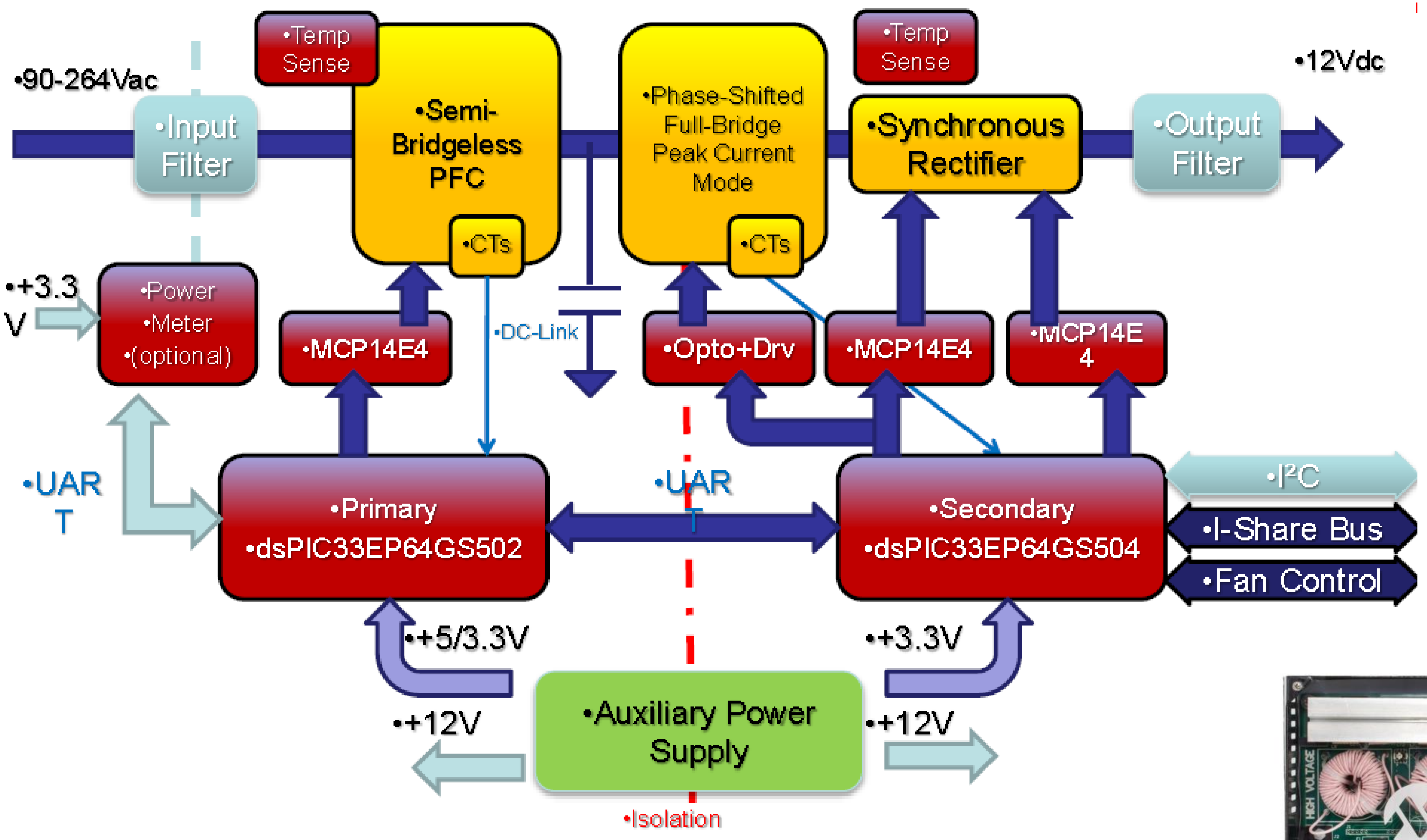
$$I_{D\_avg} = \frac{2}{\pi}\sqrt{2} * I_{line\_rms}$$

$$P_D = \frac{4\sqrt{2} * V_f * P_{out}}{\pi * \eta * V_{line\_rms}}$$

$$I_{line\_rms} = \frac{P_{out}}{\eta * V_{line\_rms}}$$

$$P_D = 2.1\% * \frac{P_{out}}{\eta}$$

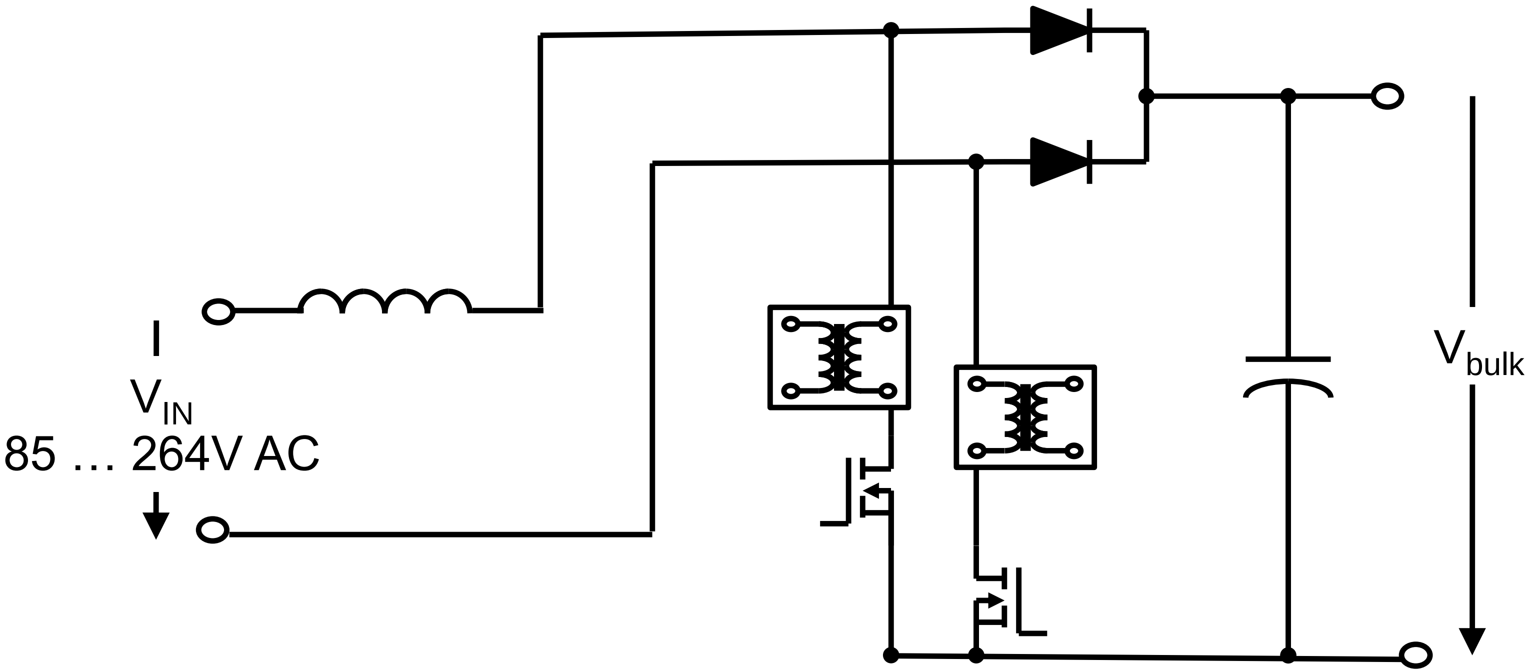
Semi-Bridgeless PFC Reference Design



750W AC/DC Reference Design

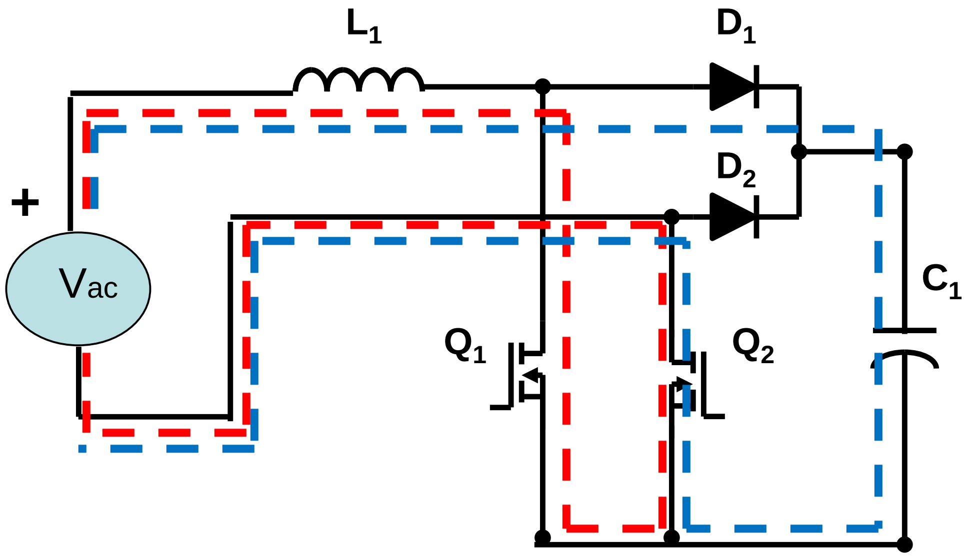
Bridgeless PFC

- **Efficiency is improved as the diode bridge is completely eliminated but MOSFET losses will increase**
- **Line is floating compared to PFC ground so simple circuitry (resistor divider network) to sense the input voltage can not be used. Instead an opto-coupler based circuit or low frequency transformer has to be used.**
- **EMI is difficult to reduce as more parasitic capacitance contribute to common mode noise.**

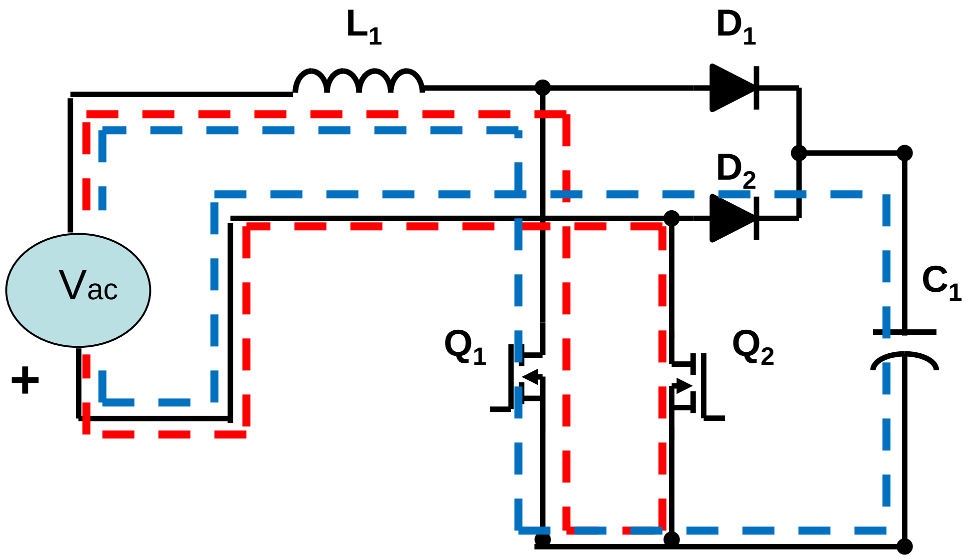


Bridgeless PFC

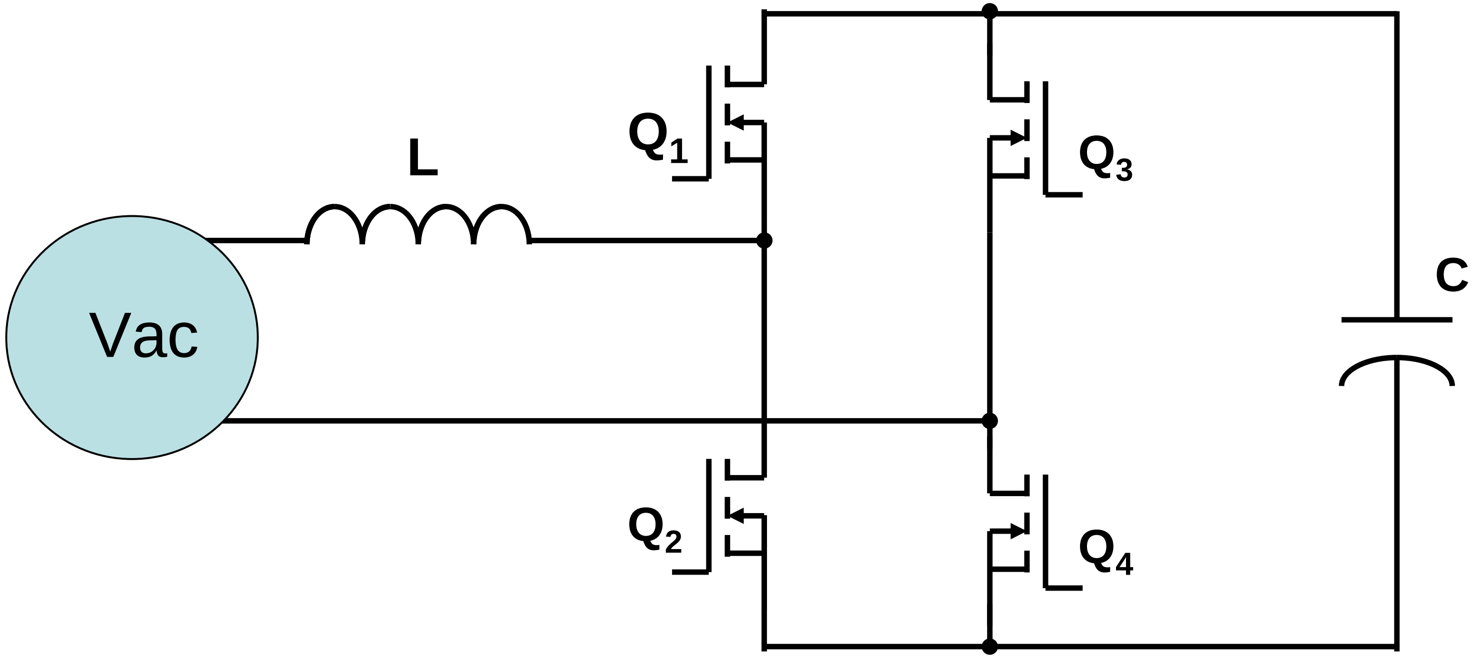
- **Case 1: Line Positive**
  - MOSFET Q1 switches
  - Current returns through Q2



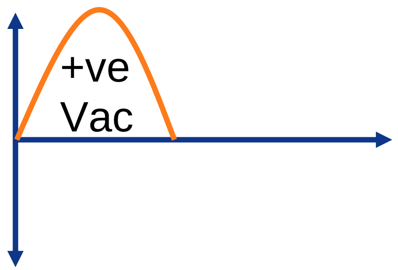
- **Case 2: Neutral Positive**
  - MOSFET Q2 switches
  - Current returns through Q1

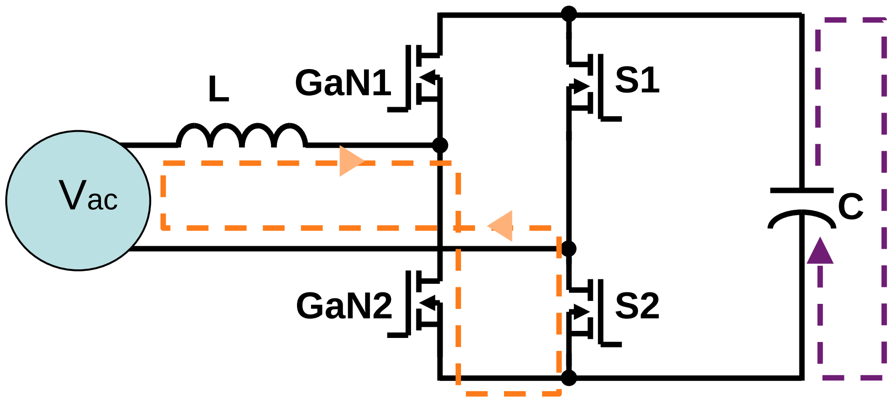


Bridgeless Totem-Pole PFC

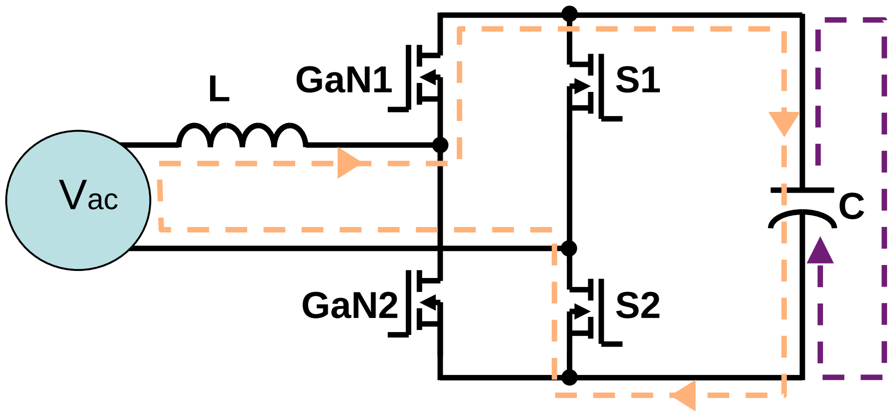


Bridgeless Totem-Pole PFC





Inductor charging
(Duty cycle = D on GaN2, S2 is on for +ve Vac)

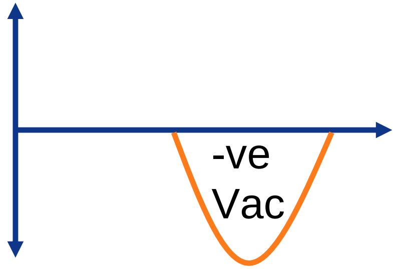


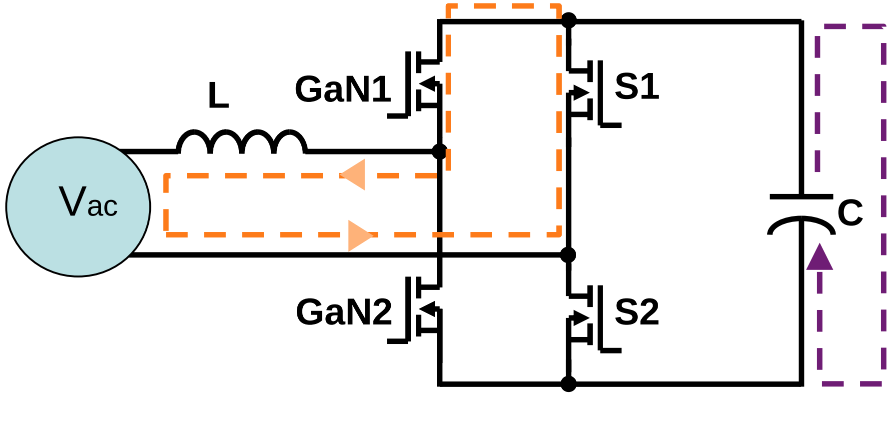
Inductor discharging
(Duty cycle = 1-D on GaN1, S2 is on for +ve Vac)

+ve V_{AC} ½ cycle :-

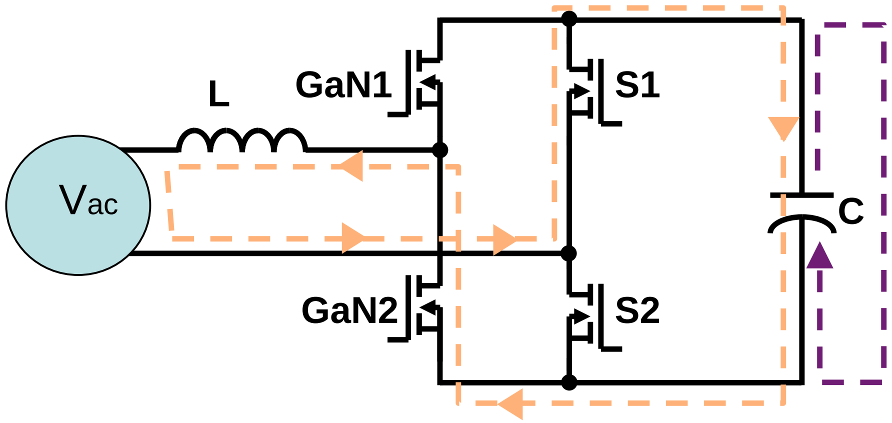
- GaN2 is active switch duty cycle D
- GaN1 is sync switch duty cycle 1-D
- Si MOSFET S2 is ON

Bridgeless Totem-Pole PFC





Inductor charging
(Duty cycle = D on GaN1, S1 is on for -ve Vac)



Inductor discharging
(Duty cycle = 1-D on GaN2, S1 is on for -ve Vac)

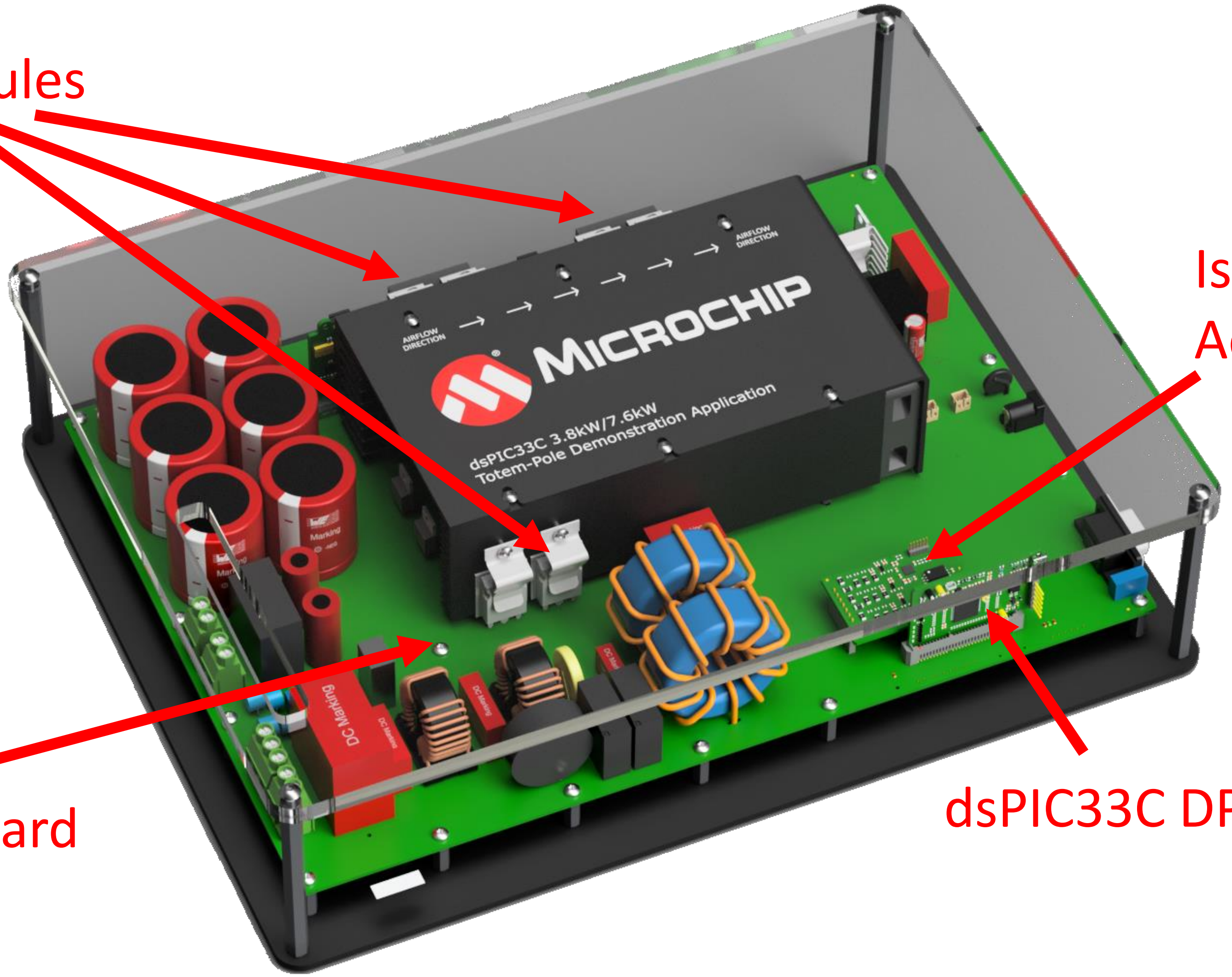
-ve V_{AC} ½ cycle :-

- GaN1 is active switch duty cycle D
- GaN2 is sync switch duty cycle 1-D
- Si MOSFET S1 is ON

dsPIC33C 1PH 3.8kW/7.6kW PFC/Inverter

SiC Plug-in Modules

Isolated Voltage Acquisition Board



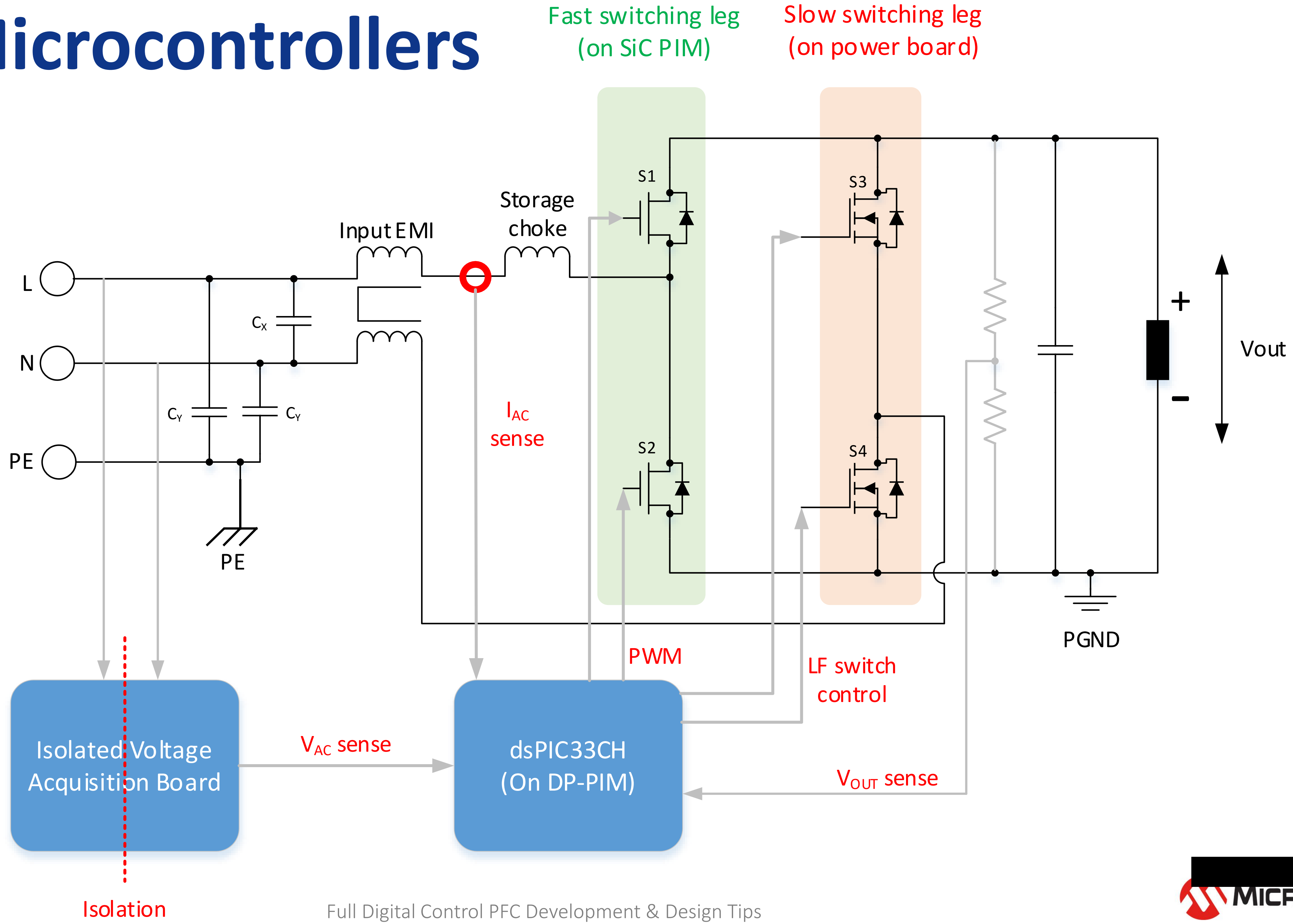
Totem Pole Power Board

dsPIC33C DP-PIM

Key Specifications

Parameter	Min	Typical	Max	Units	Notes
AC voltage	90	230	265	V_{DC}	DC operating mode also supported
AC current			16	A_{RMS}	$32A_{RMS}$ for interleaved operation
DC Bus Voltage	390		420	V	
DC Bus Current			10	A	
Output Power (Non-interleaved)			3.8	kW	High line
Output Power (Interleaved)			7.4	kW	High line
Operating Line Frequency	47	50	65	Hz	
Switching Frequency		100		kHz	Demo operates at 100kHz
Efficiency			98.5	%	
Hold-up time			10	ms	
Inrush current			30	A_{PEAK}	
Start-up time			2	s	
Ambient Operating Temperature	-40		50	°C	

Main Microcontrollers



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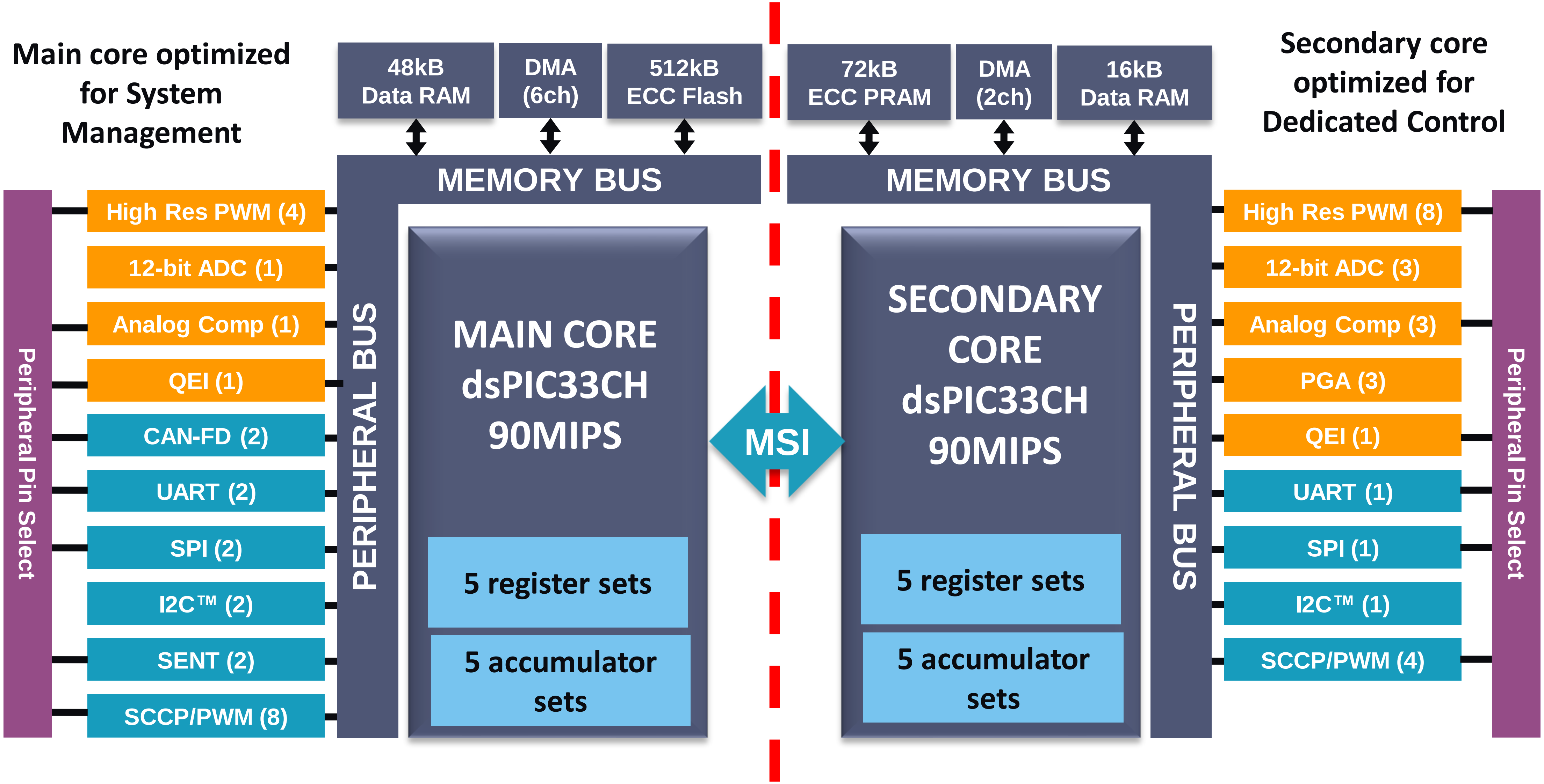
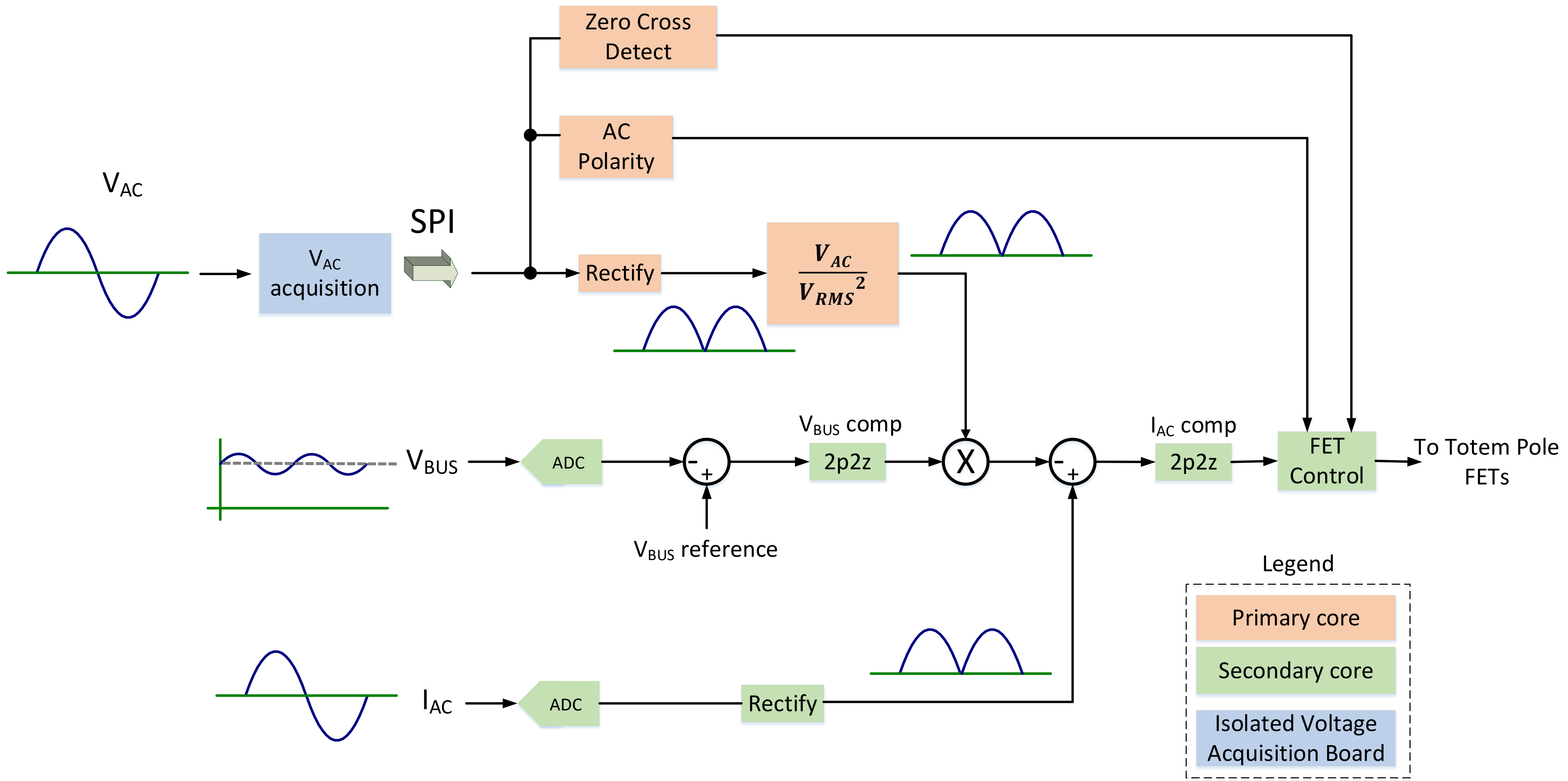
dsPIC33CH (Dual Core)



dsPIC33CH512MP508 Device Shown

PFC Firmware



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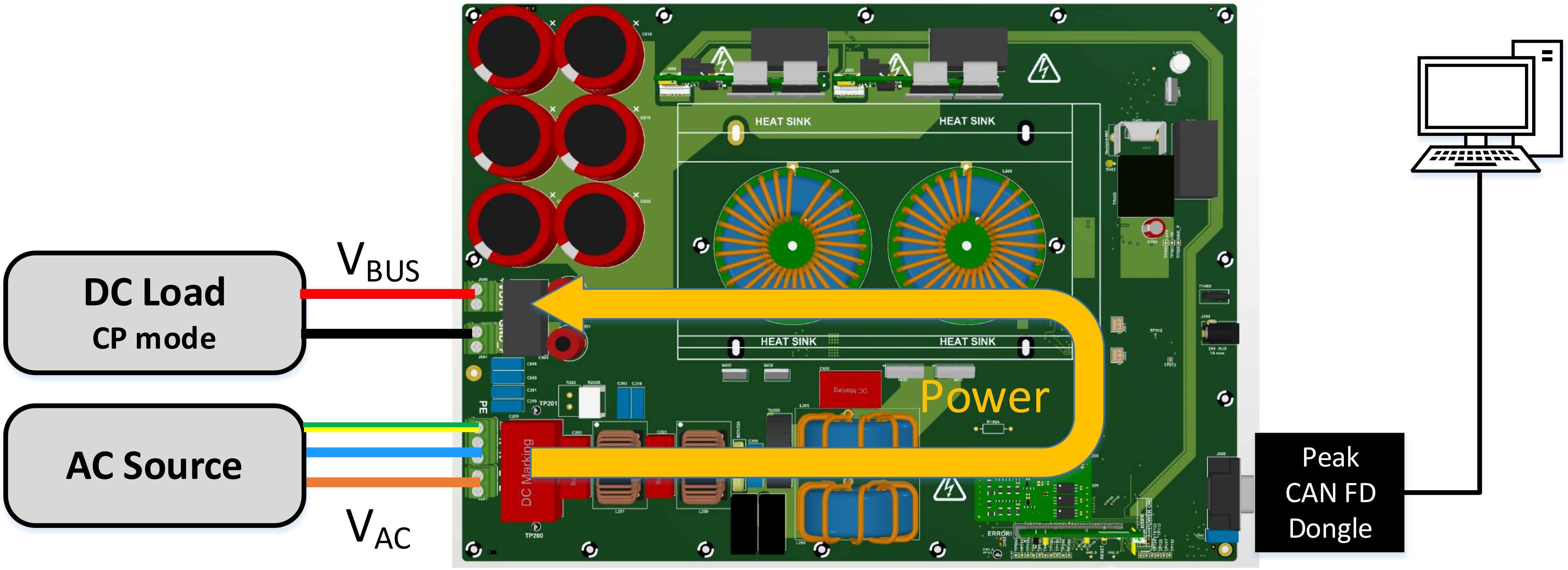
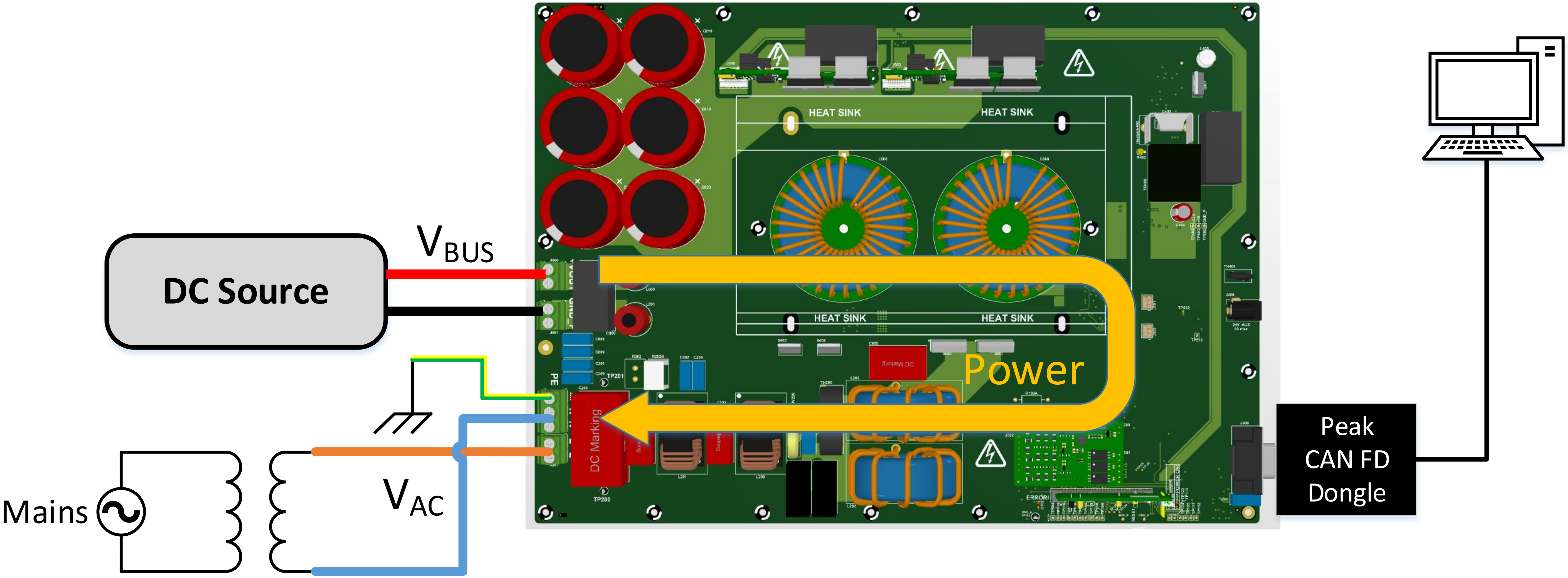
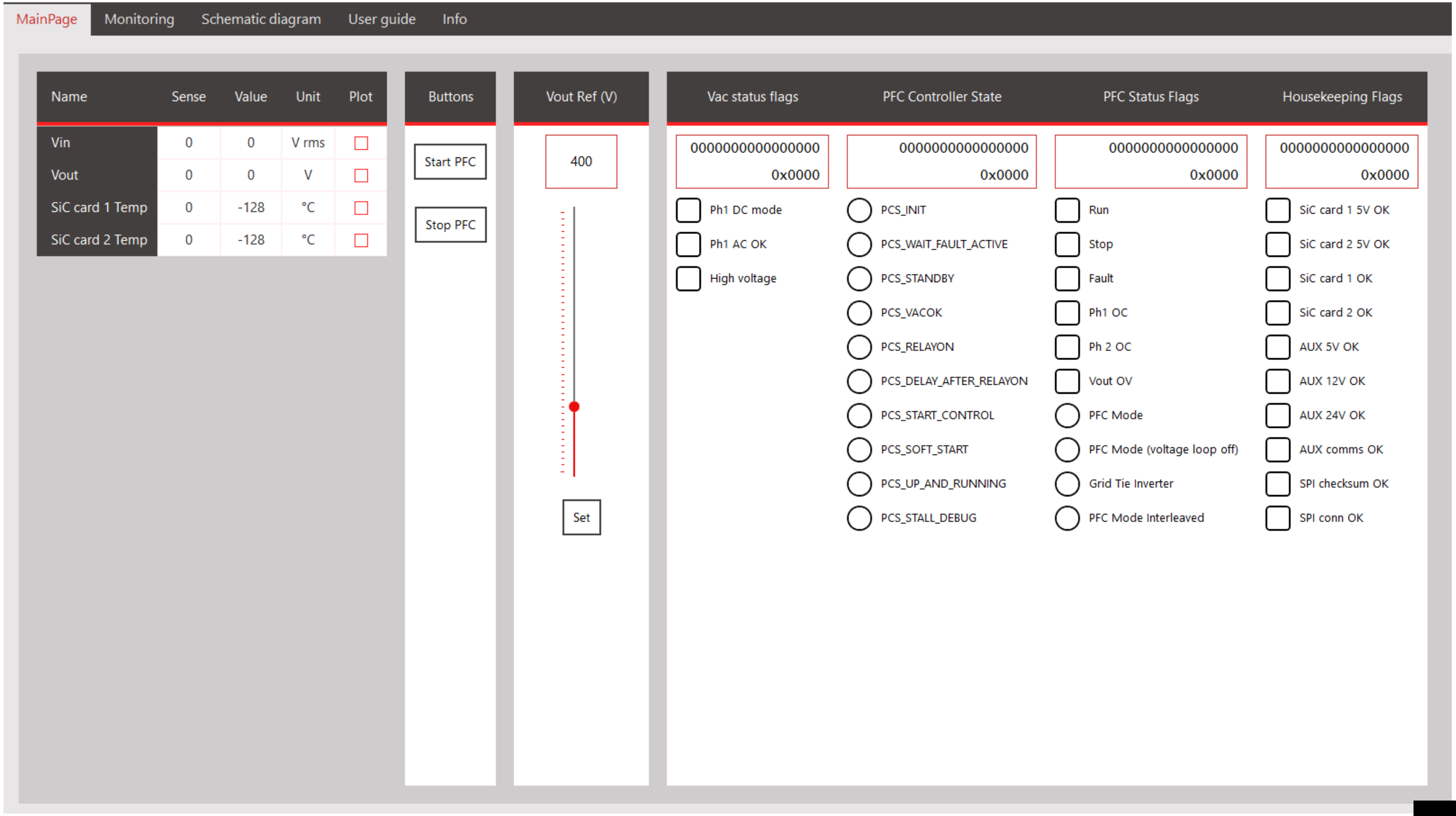
PFC Test Setup



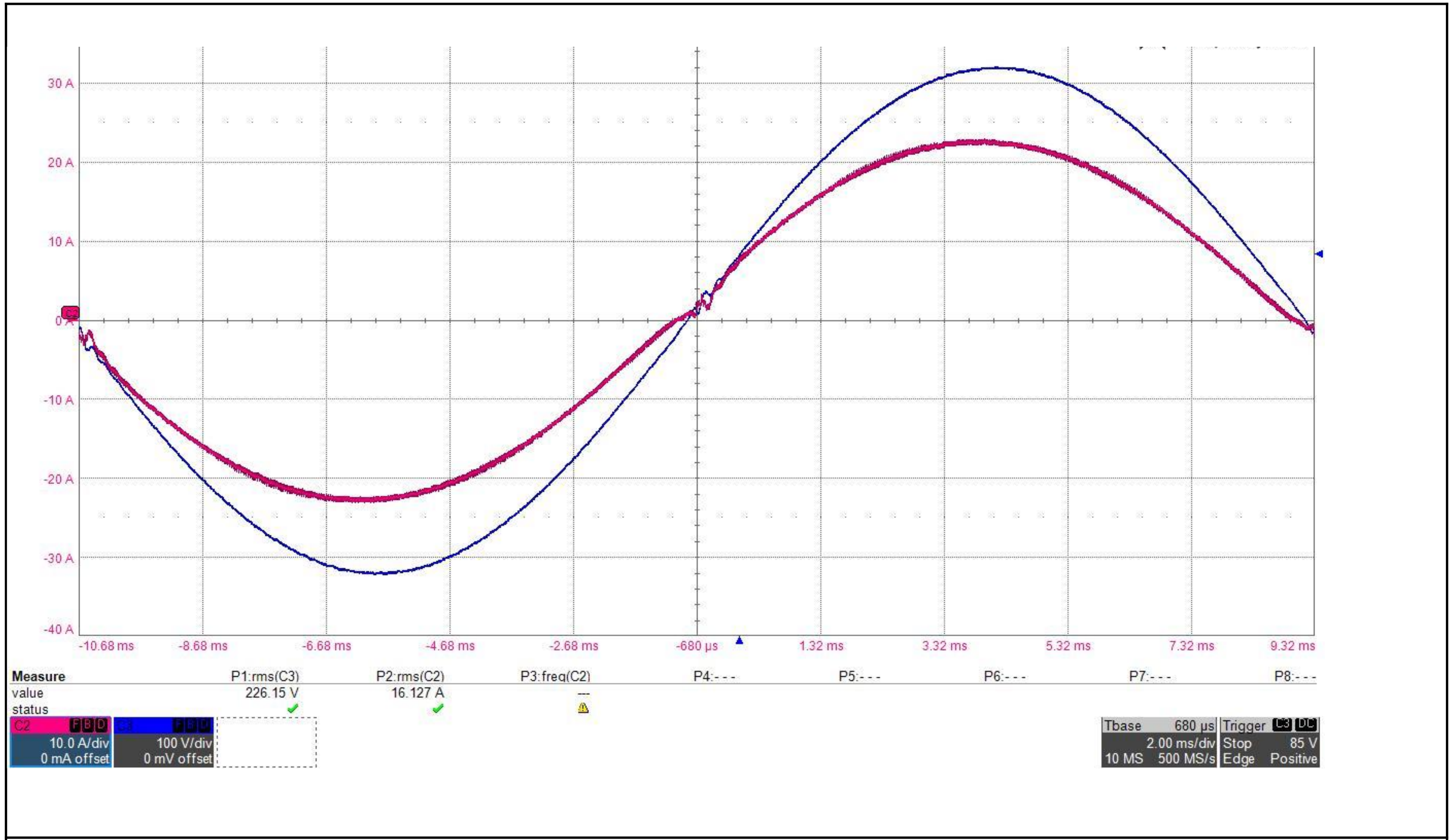
Grid Tied Inverter Test Setup



Power Board Visualizer



PFC: Key Waveforms



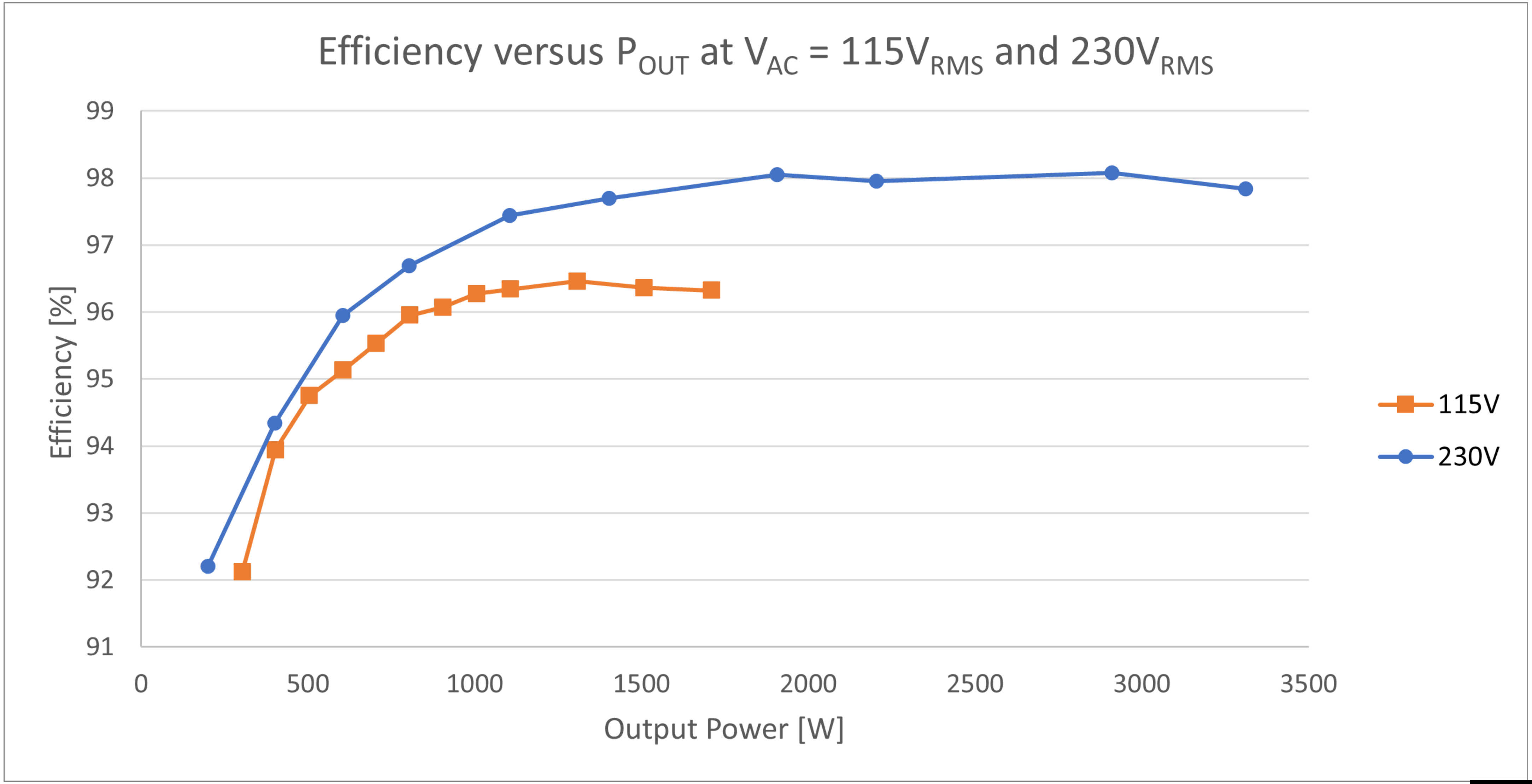
V_{AC} = 230V_{RMS}, I_{AC} = 16A_{RMS} (full load).

V_{AC} generated using AC source.

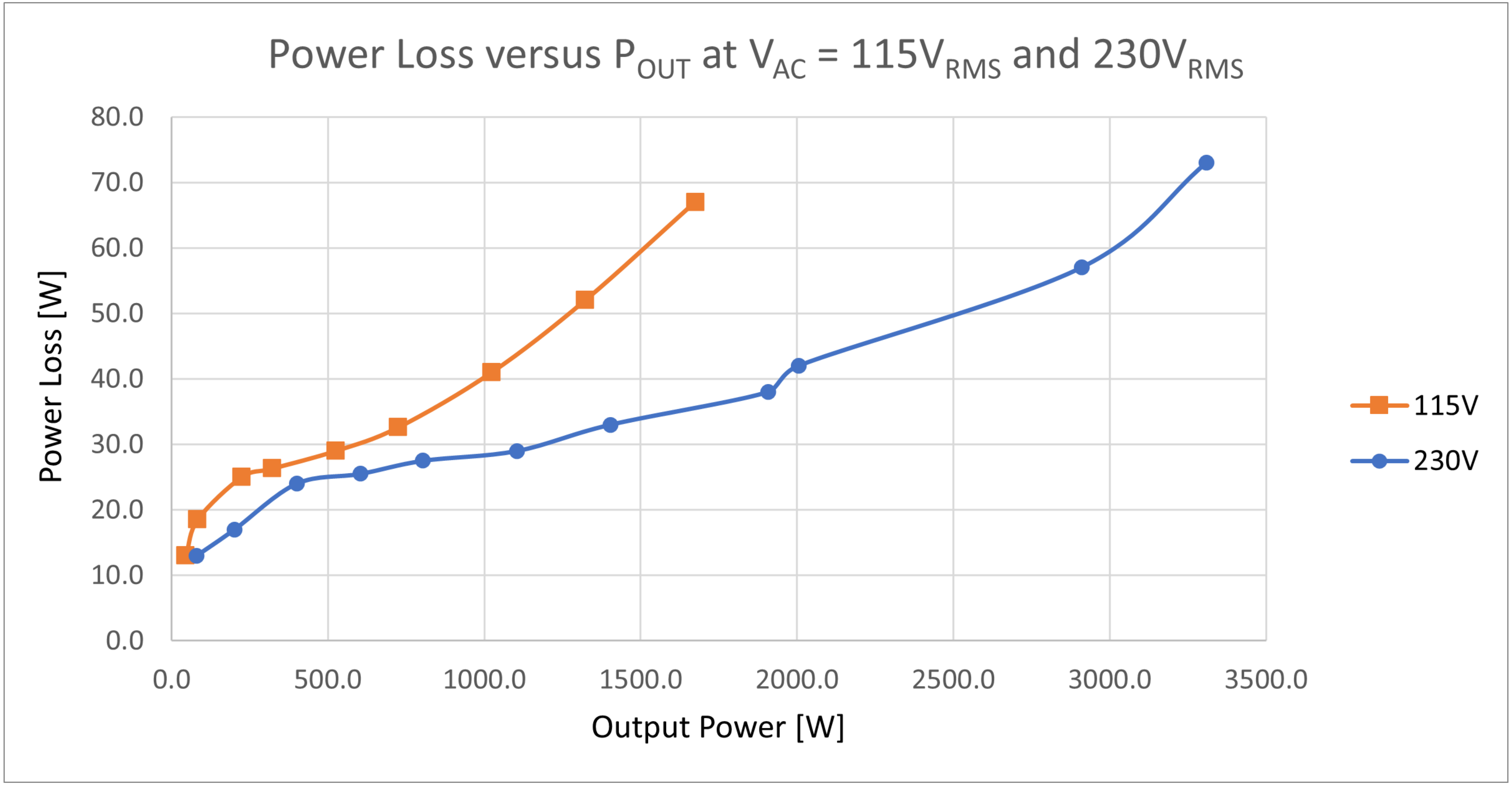
Channel 2 (Purple): Input current (I_{AC}).

Channel 3 (Blue): Input Voltage (V_{AC}).

PFC Efficiency



PFC Power Loss



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Bridgeless Totem-Pole PFC Reference Design

Test Setup and Conditions	
Evaluation Kit	TDTTP4000W066C-KIT
Operating frequency	66 kHz
Input voltage	85 V_{ac} to 265 V_{ac}
Output voltage	387 V_{dc} ±5 V_{dc} (programmable)
Digital power PIM	dsPIC33CK256MP506
GaN device	TP65H035G4WS
Gate resistor	30 Ω
Gate ferrite bead	200 Ω @ 100MHz
Snubber circuit	Not required
Deadtime	Programmable

transphorm

Available at:

Digi-Key CORPORATION

mouser.com

[redacted]

3-Phase Vienna PFC Reference Design

DC-Link Capacitors

dsPIC33CH Control Card

3-Phase AC Input

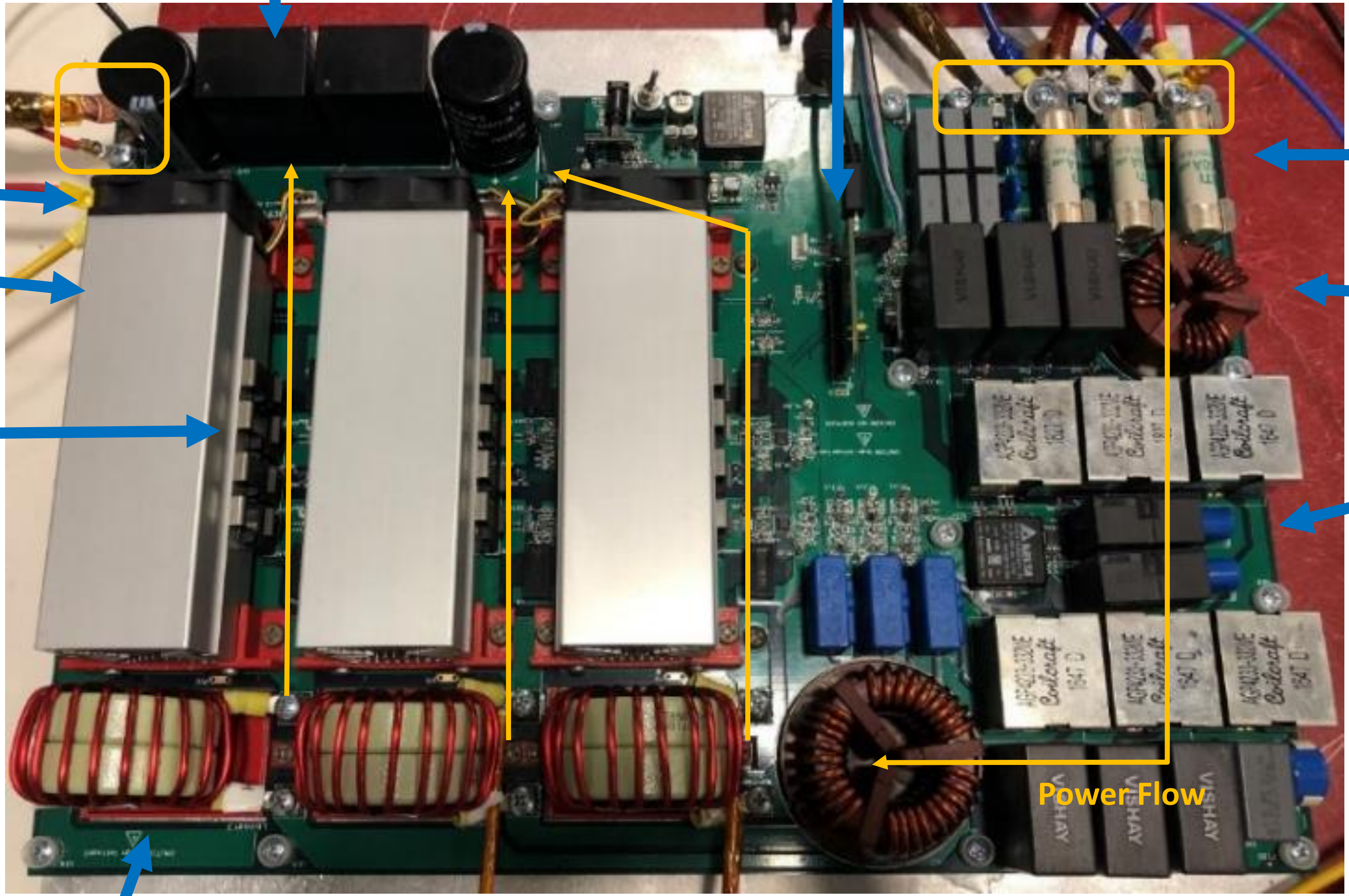
DC Output

Fans

Heatsink

700V, 15 mΩ SiC MOSFETs

1200V, 50A SiC SBDs (on bottom)



50A Fuses

EMI Filters

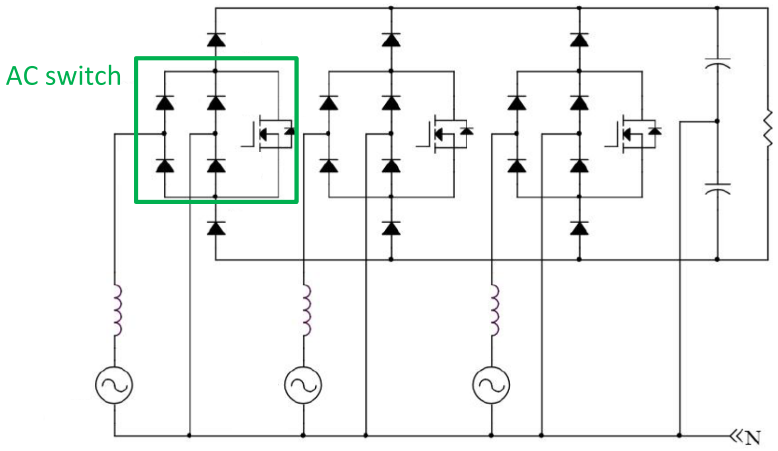
Pre-Charge Circuit

CM Feedback Circuit

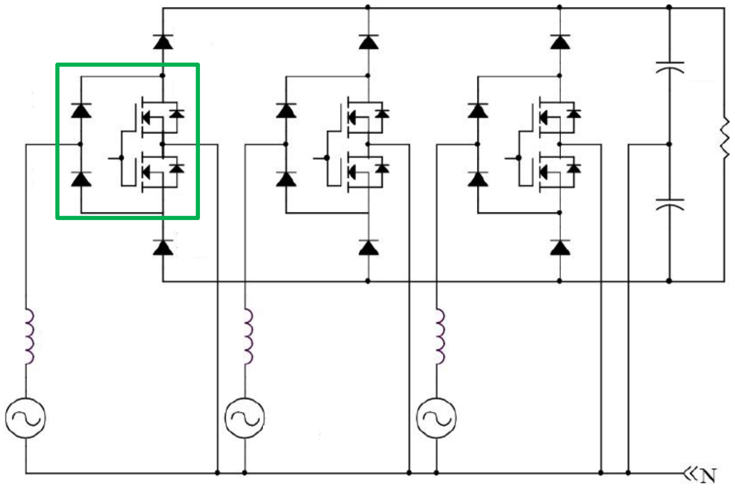
Boost Inductors

Vienna Rectifier Topologies

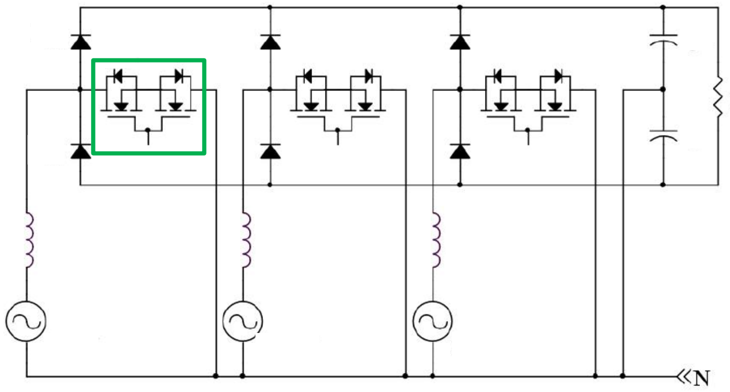
Topology I
Classical Version



Topology II



Topology III
Reference Design (3-wire)

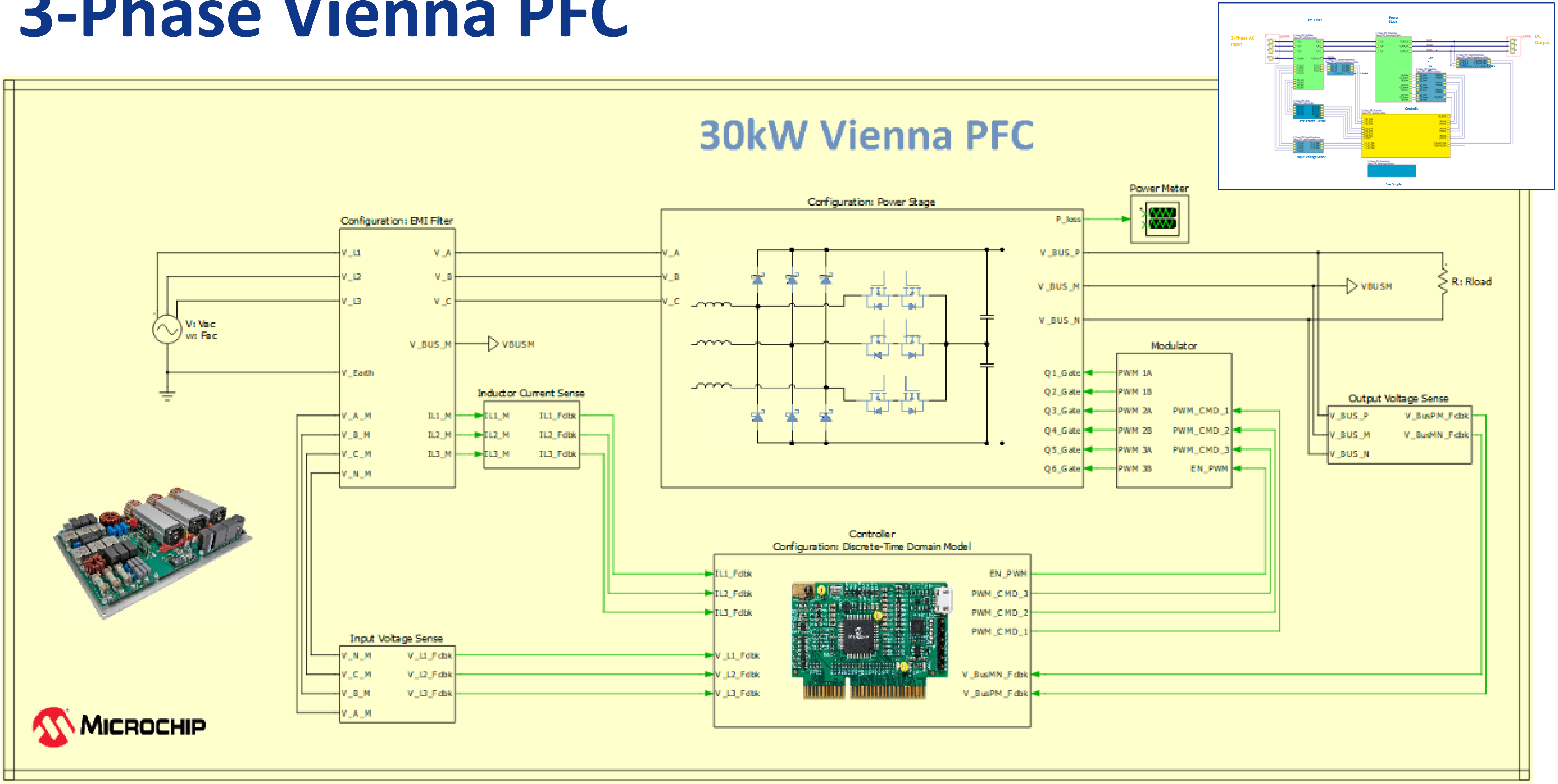


- **3-Level Modulation**
  - Neutral, when MOSFET is on
  - ½ V_{DC} output, when upper FWD is on
  - -½ V_{DC} output, when lower FWD is on

- **Topology I**
  - **Pro's:** single MOSFET per phase, low-cost Si diodes, easy to control
  - **Con's:** MOSFET losses significant
- **Topology II**
  - **Pro's:** two MOSFETs per phase, fewer diodes, easy to control, lower MOSFET losses (on only for half-wave)
  - **Con's:** lower power density than topology III
- **Topology III**
  - **Pro's:** two MOSFETs per phase, no Si diodes, lower MOSFET losses over topology I (no switching losses for one half-wave), fewest components resulting in highest power density
  - **Con's:** difficult to control

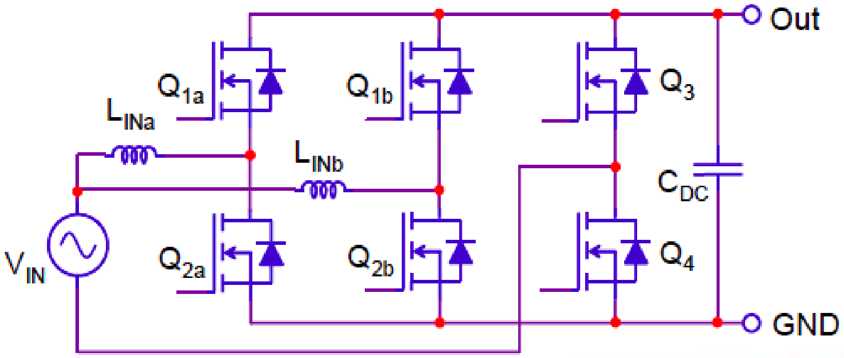
3-Phase Vienna PFC

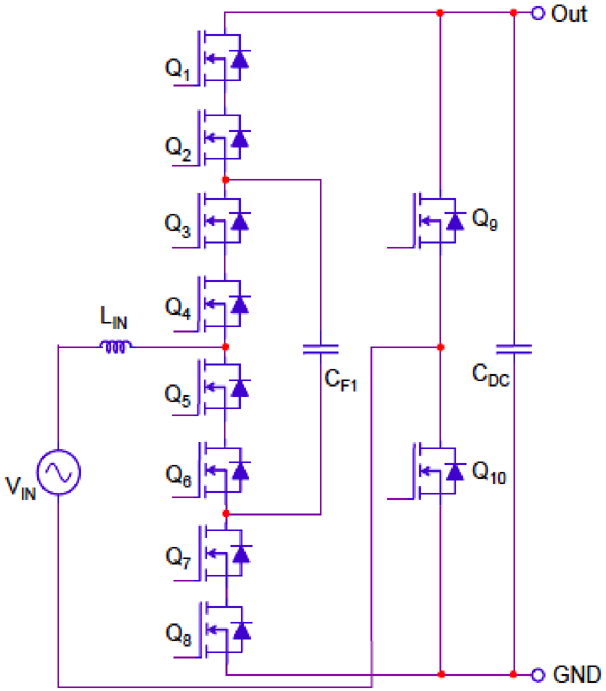
Reference Design Schematic



Techniques to Shrink PFC

- Use GaN FETs → Higher switching frequency
  - Zero Q_{RR}
  - Lower hard-switching loss
  - Smaller size
- Alternative topologies → Reduce passives
  - Interleaved TP
  - Multi-level
  - Cost offset by passive size reduction





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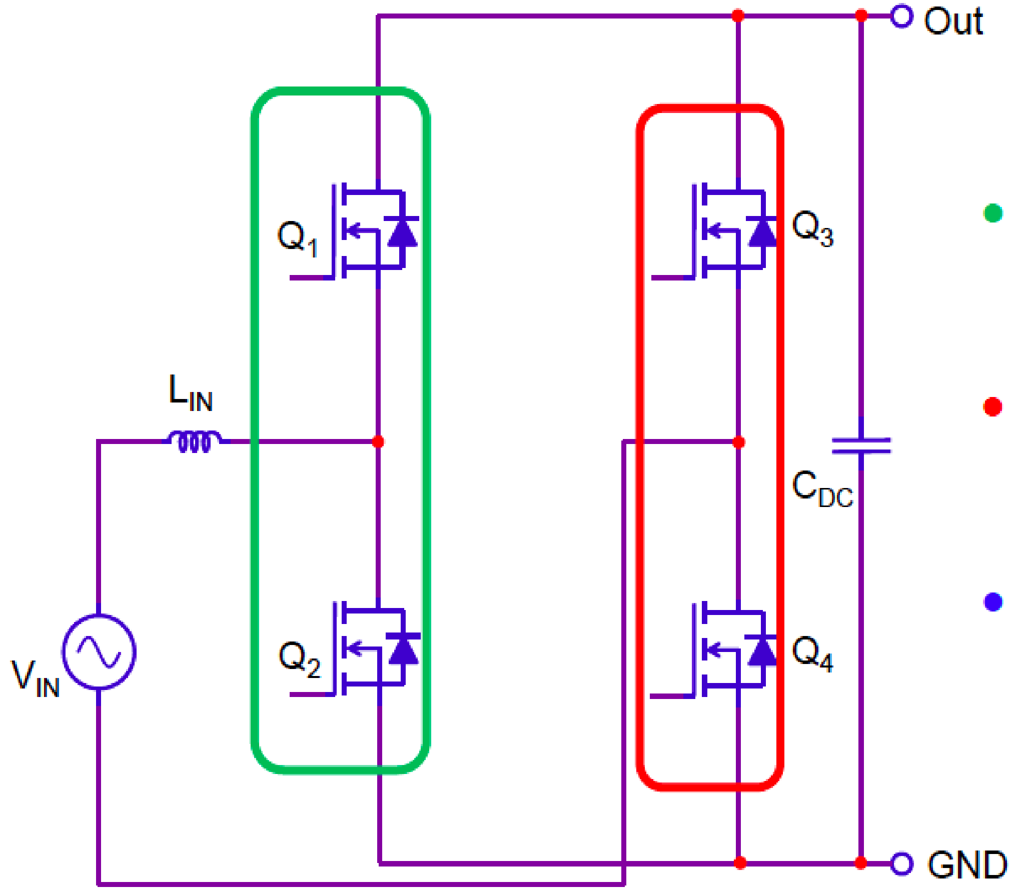
Case for a Multi-level Converter

EFFICIENT POWER CONVERSION

Two-Level Totem-Pole PFC

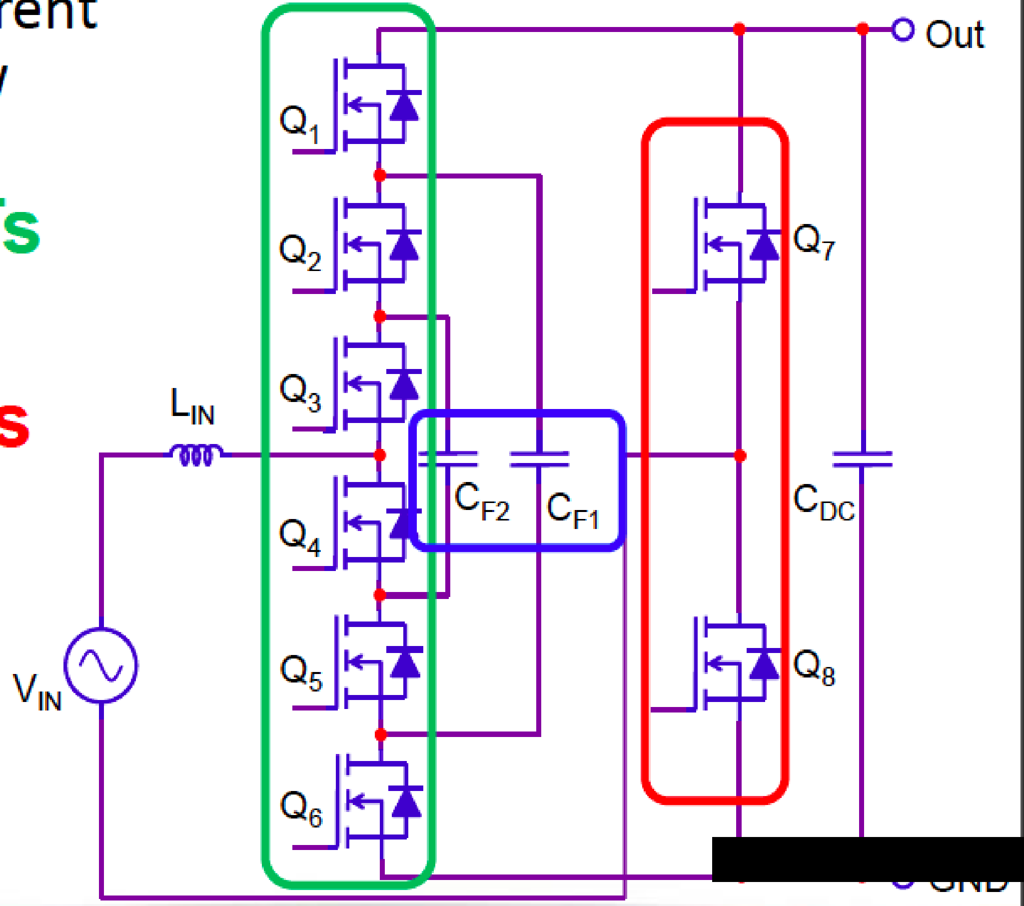
- 1x V_{DC} EMI, 1x I_{Ripple} EMI
- Requires 2-Stage Filter



Four-Level Flying Capacitor Totem-Pole PFC

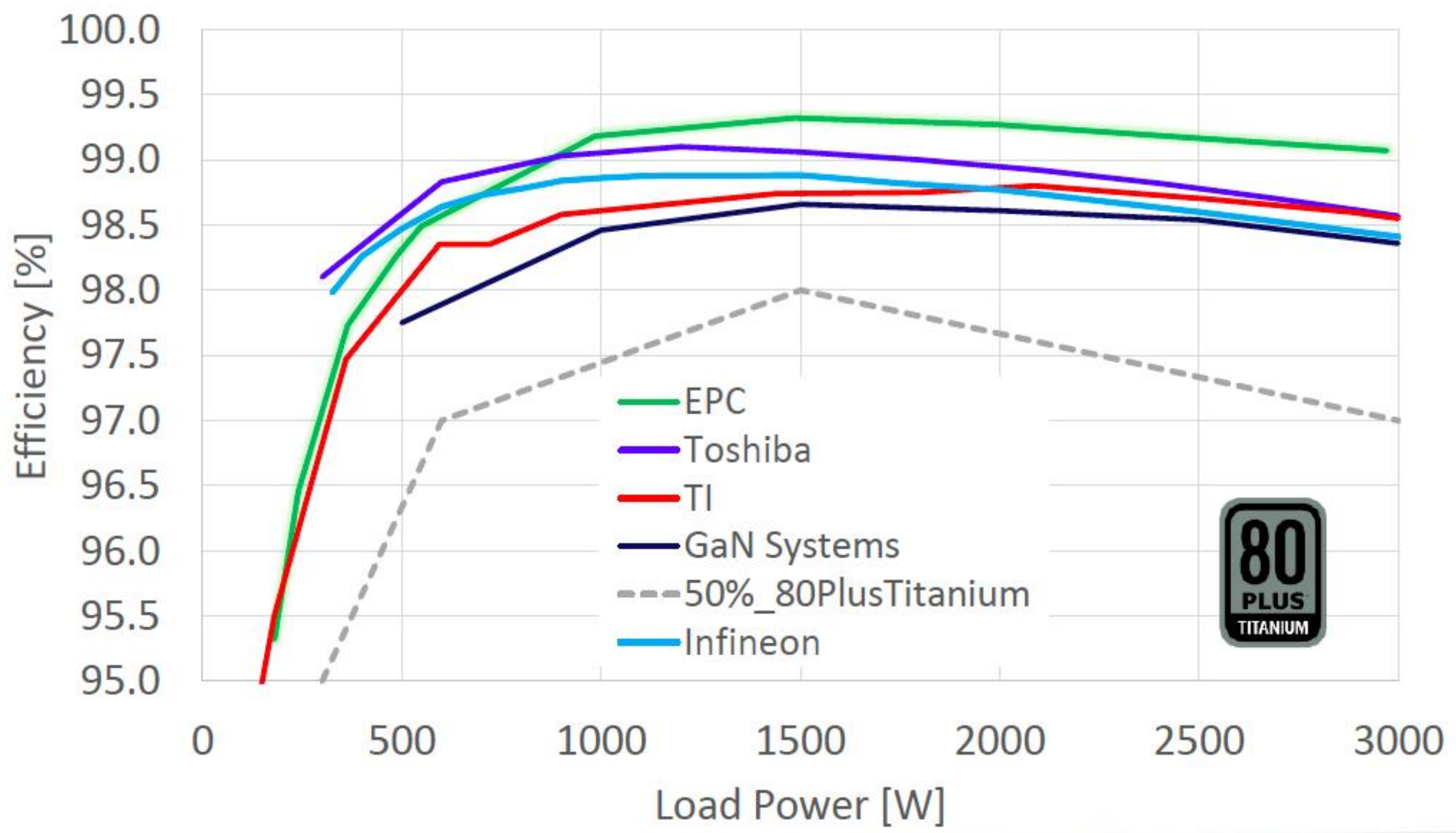
- $^1/_3$x V_{DC} EMI, 1x I_{Ripple} EMI
- Requires Single-Stage Filter
- Higher current control BW

- **Switching FETs (kHz)**
- **Sync Rectifiers (Hz)**
- **Flying Capacitors**



Electrical Performance

EPC design excludes low power optimization; e.g. active dead-time



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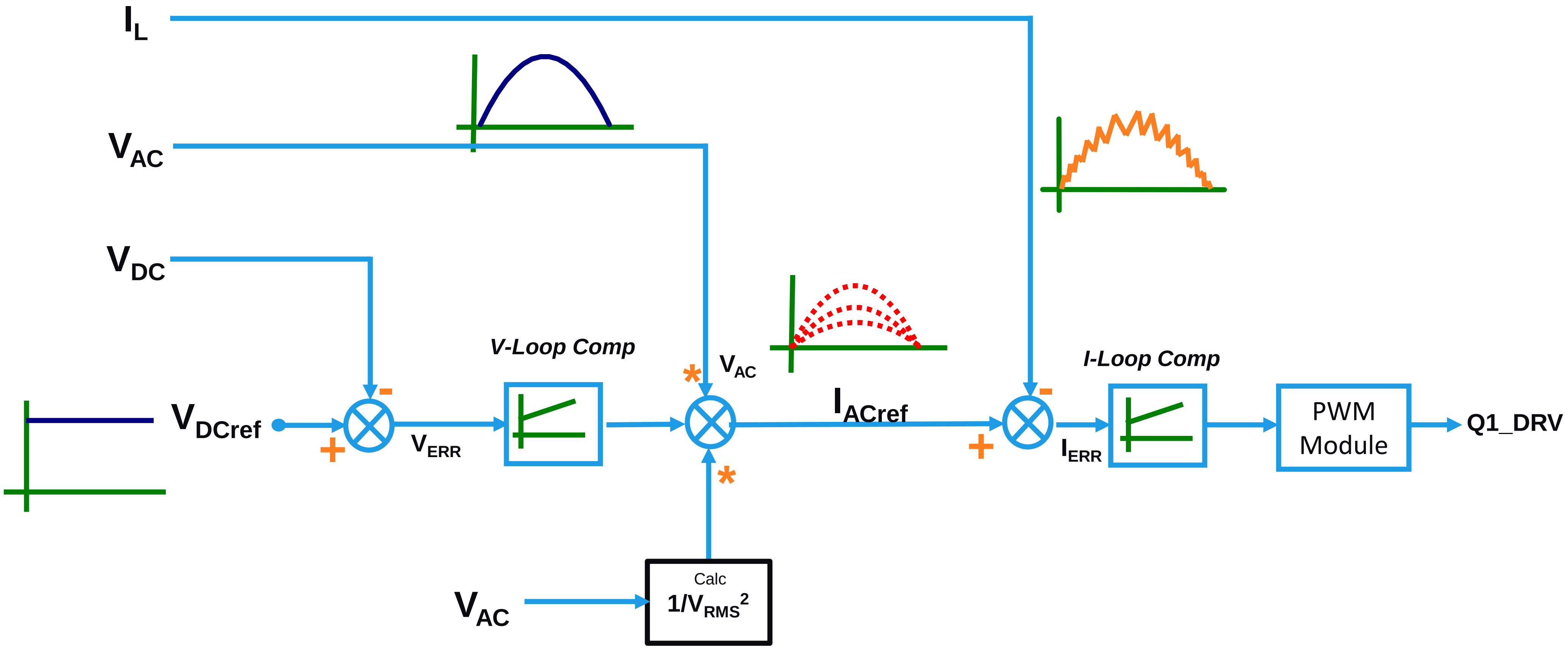
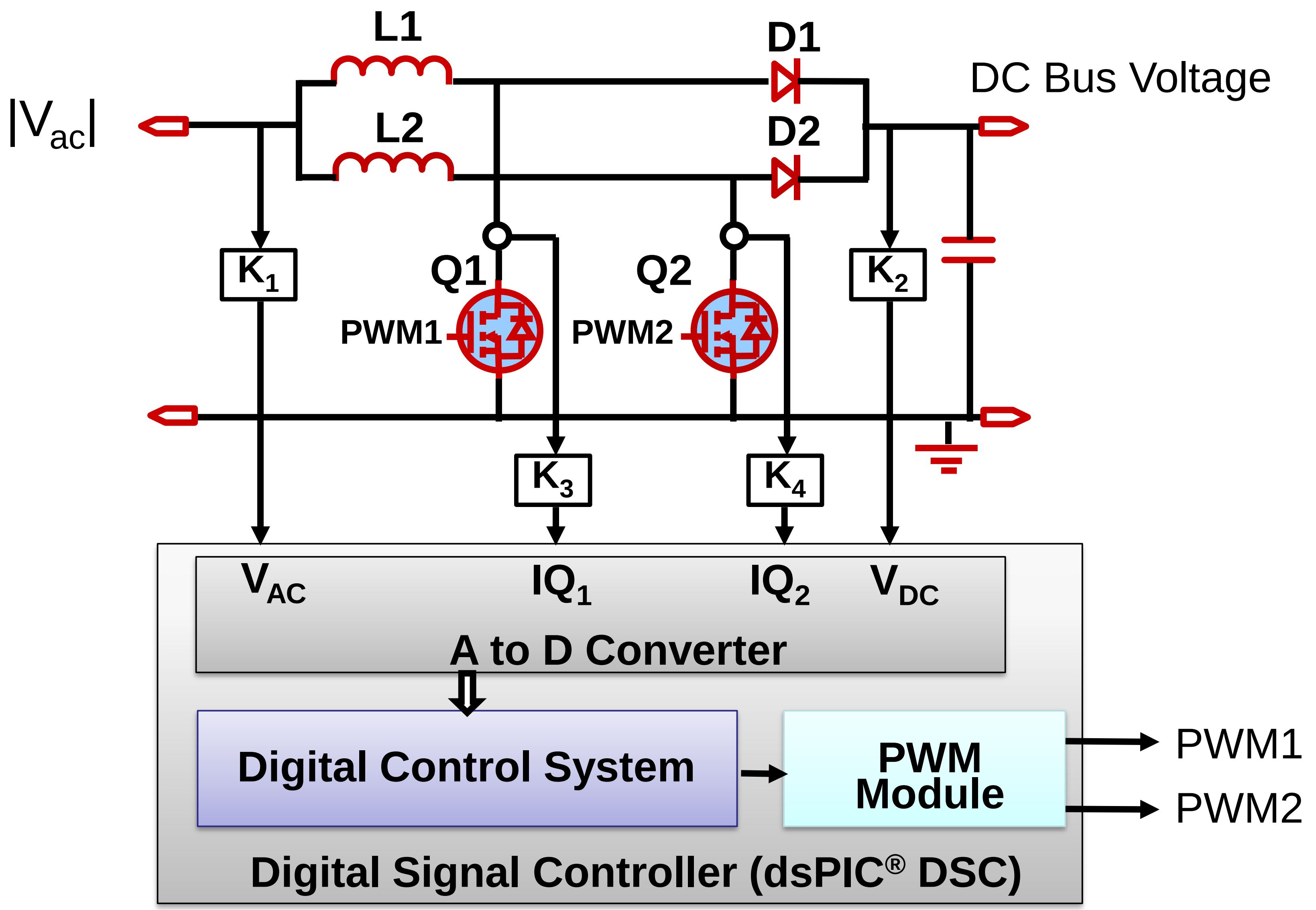
Digital PFC Using the dsPIC® DSC

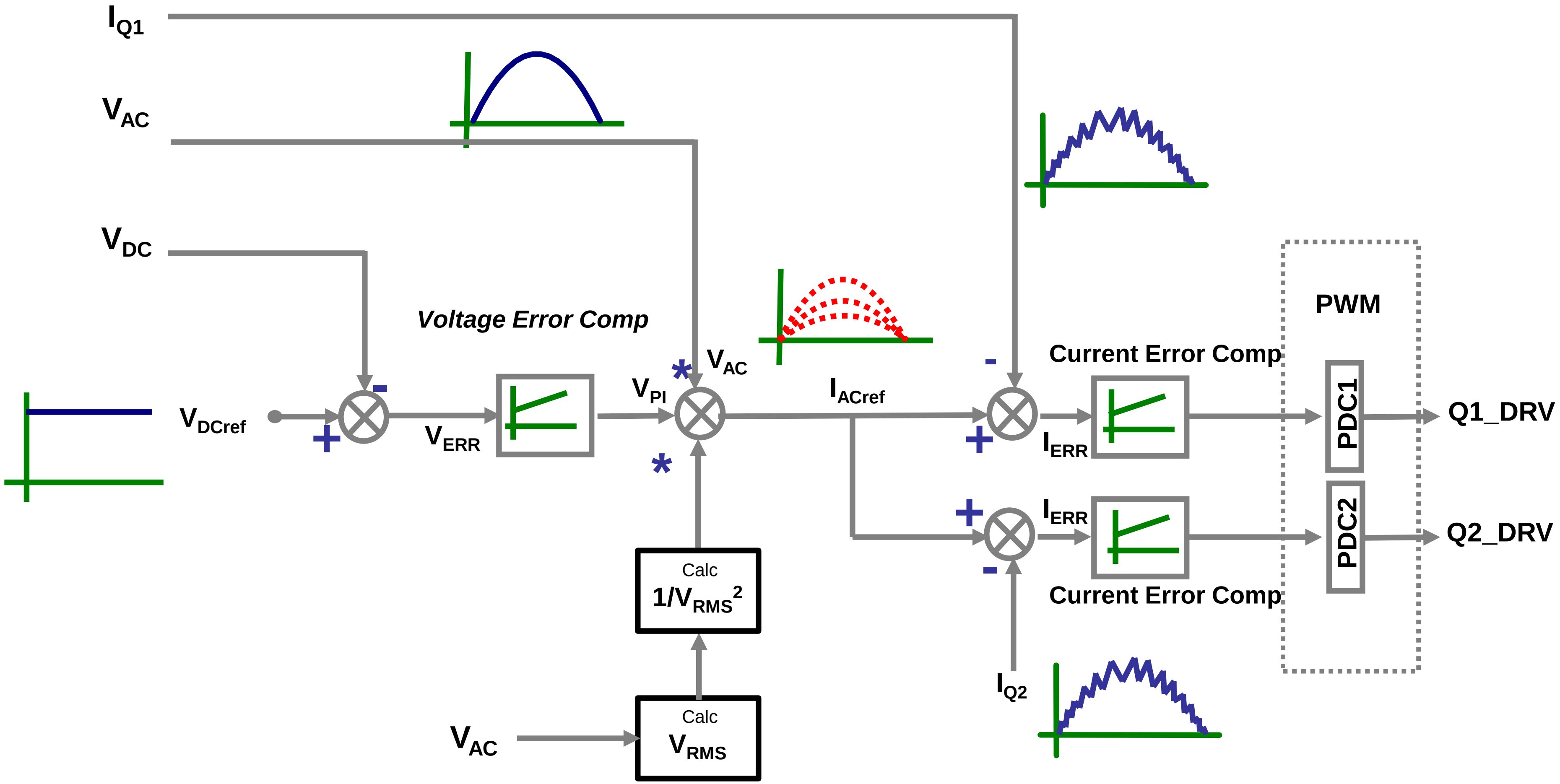
PFC Control Scheme



Digital Implementation - IPFC



PFC Control Scheme

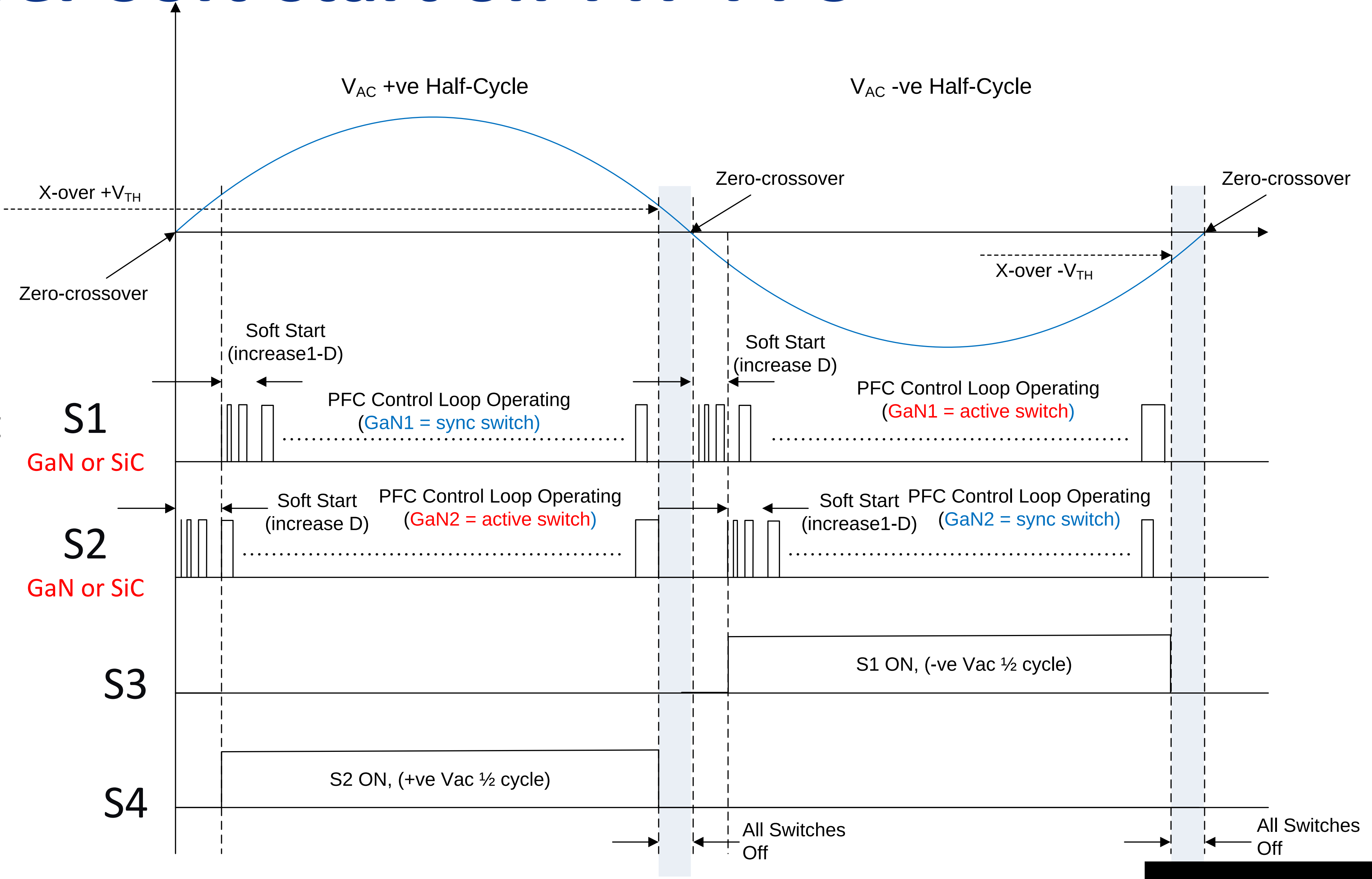


Design Issue and Tips

V_{AC} Zero-xover Soft-start on TTP PFC

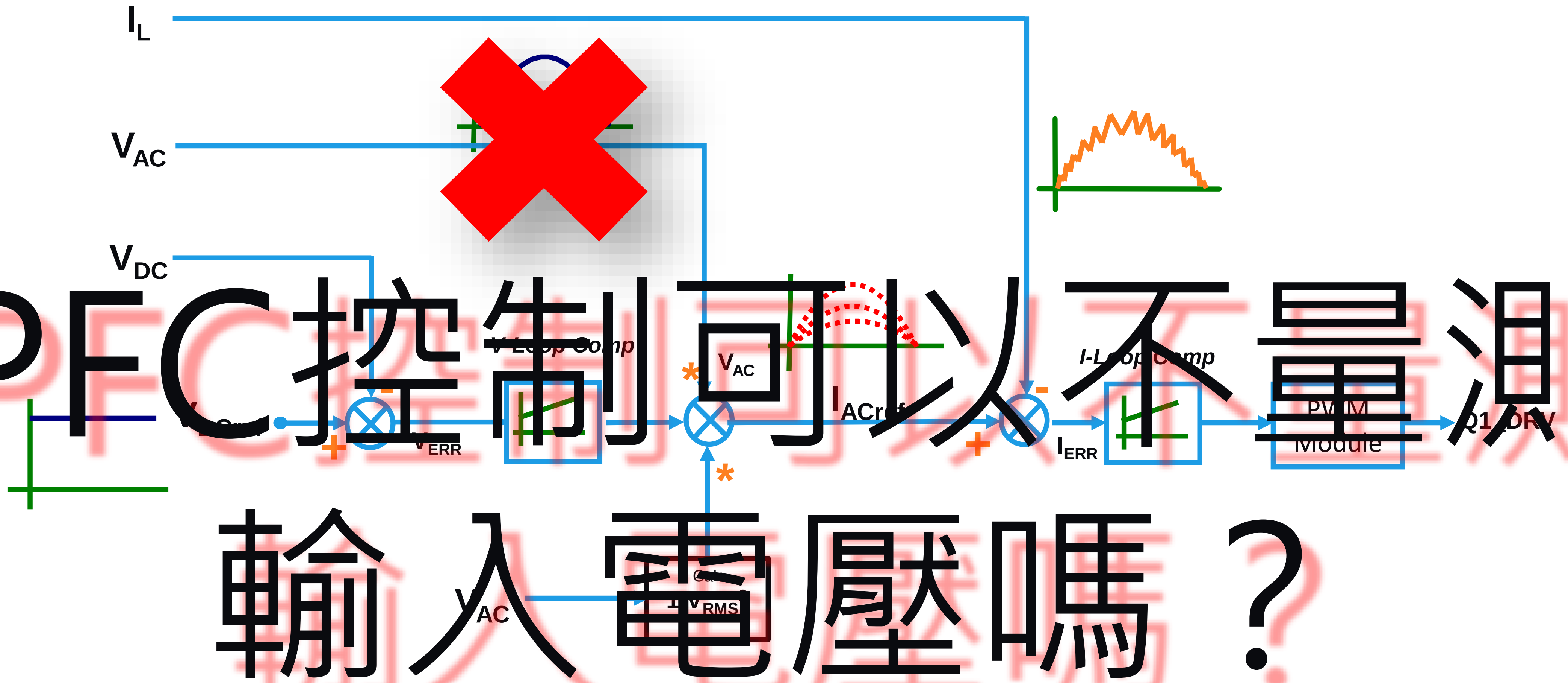
At V_{AC} zero-xover :

- **Potential for large current spikes, if timing is wrong.**
- **Therefore, switching is stopped approaching zero-xover.**
- **Soft-start operation used on the other side of zero-xover.**
  - Duty cycle begins small and is increased over 10-2(cycles
  - Until D_{SS} is the same as D_{loop} calculated from the PFC control loop
  - Then PFC control loop takes over (until the next zero-xover)



MICROCHIP

ACMC PFC

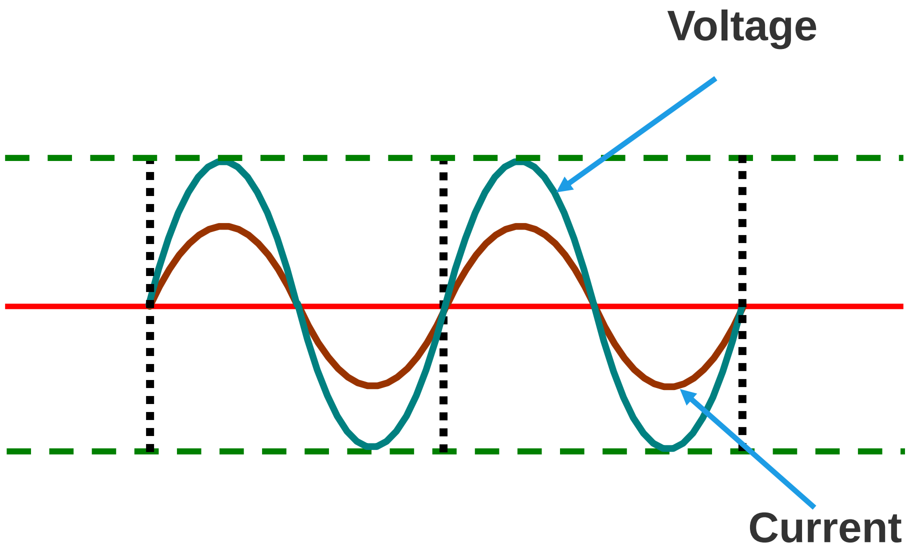


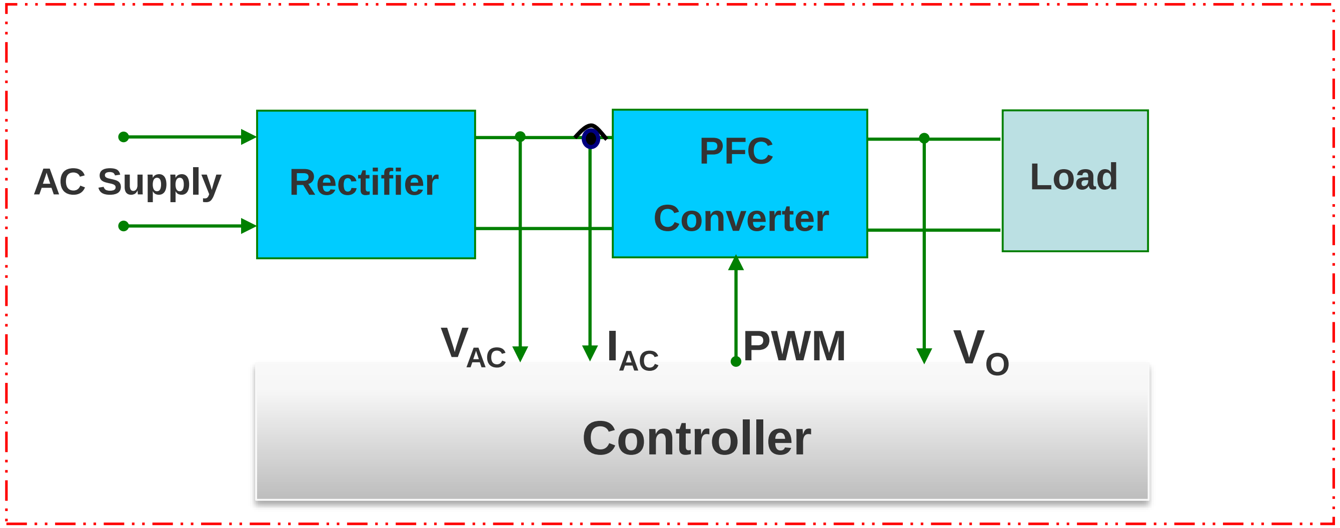
PFC控制可以不量測輸入電壓嗎？

[redacted]

When Power Factor = 1

$$PF = \frac{Real\ Power}{Apparent\ Power} = \cos\emptyset$$

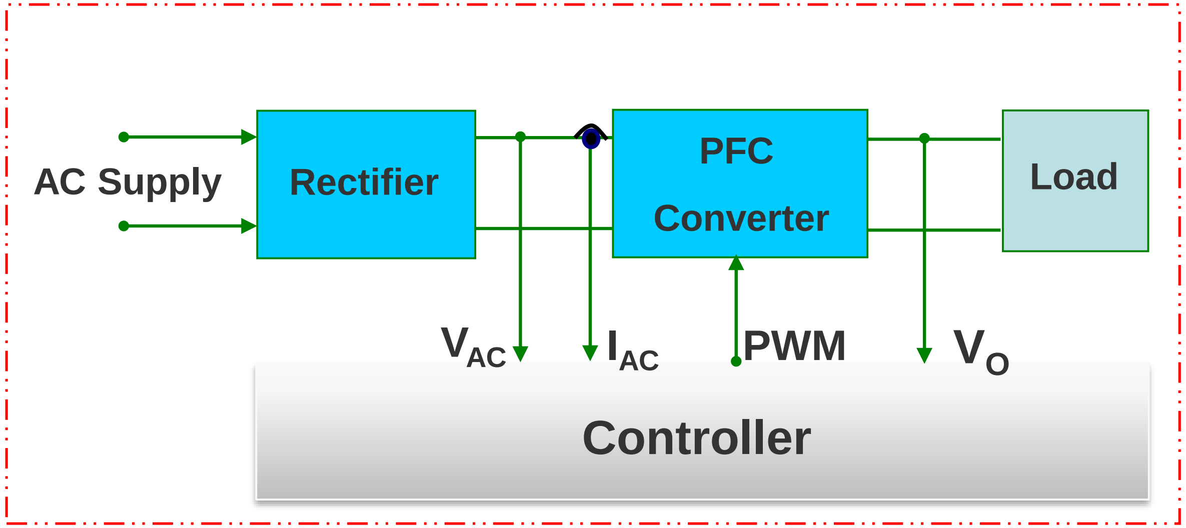


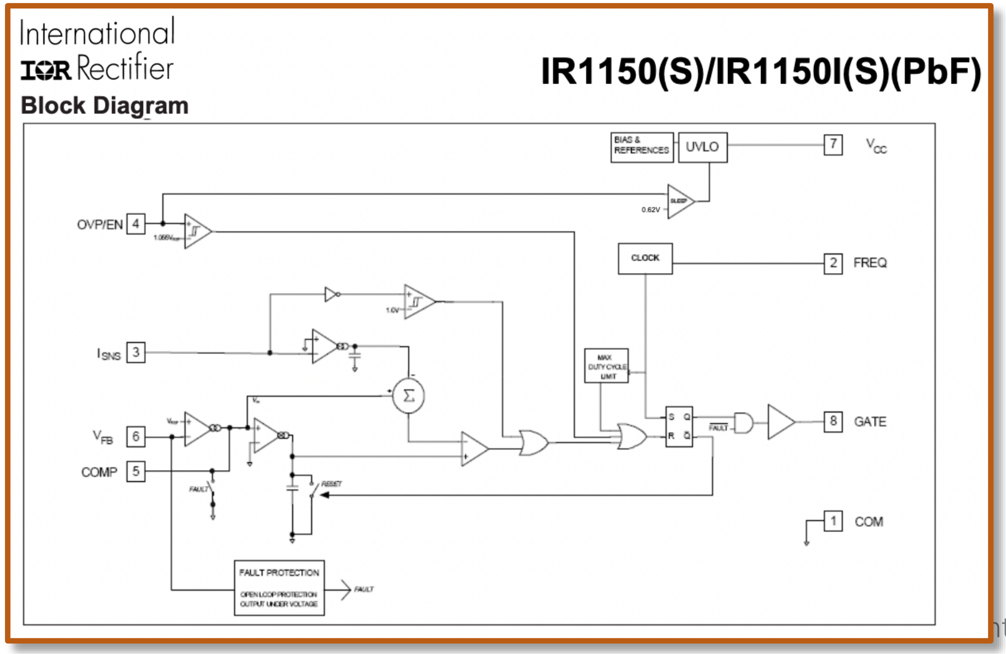


$V_{AC} = I_{AC} * R_e$

R_e = PFC等效電阻

OCC(One Cycle Control) PFC

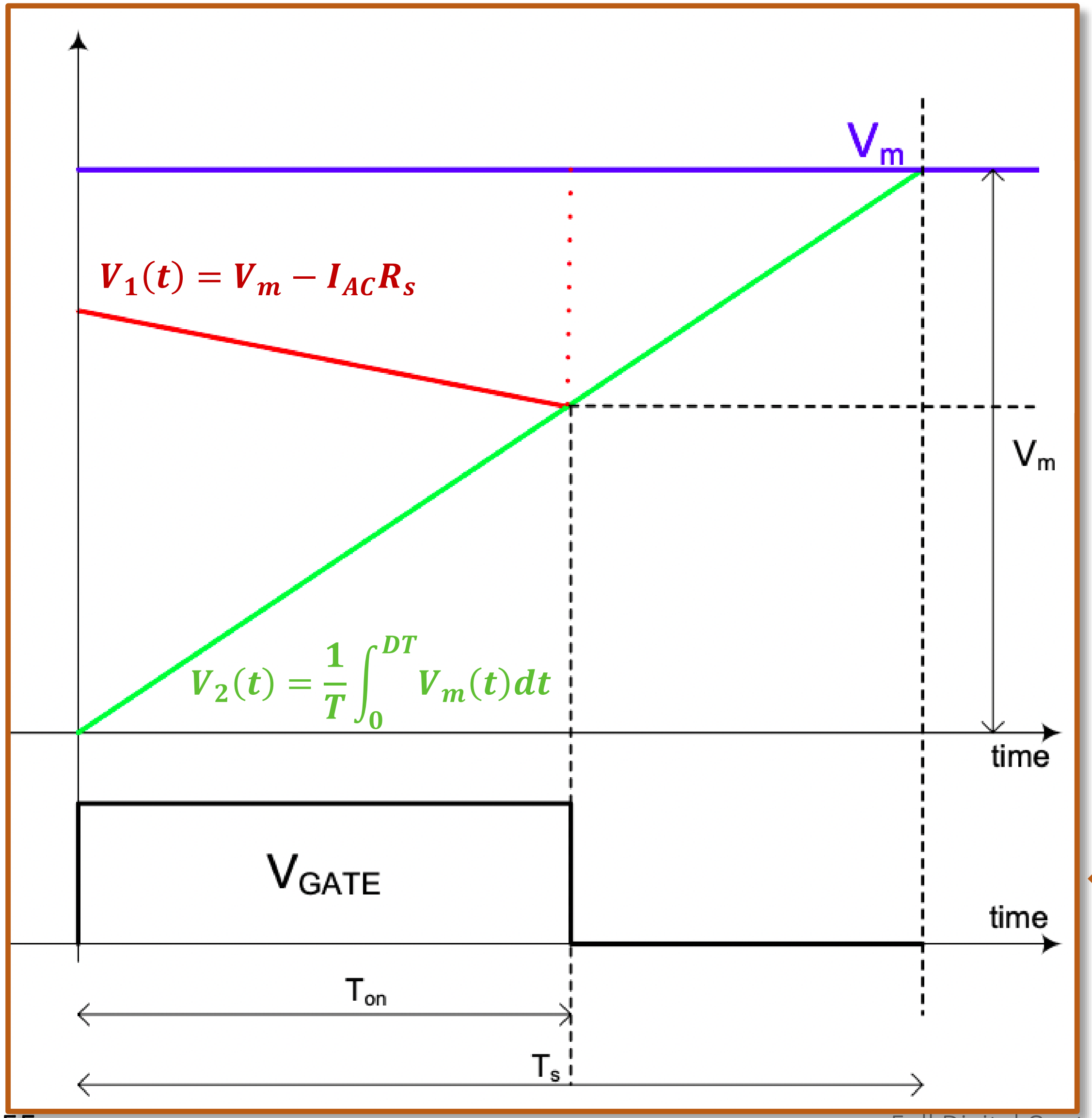




- $V_{AC} = I_{AC} * R_e$, R_e = PFC等效電阻
- CCM Boost Converter:
  - $V_{AC} = V_O * (1-D)$, D = Duty Cycle
  - $I_{AC} = (1-D) * V_O / R_e$
  - $I_{AC} * R_s = (1-D) * V_O * R_s / R_e$, R_s = 電感電流採樣電阻(增益)
  - $I_{AC} * R_s = (1-D) * V_m$, $V_m = V_O * R_s / R_e$
  - $V_m - I_{AC} * R_s = D * V_m = \frac{1}{T}\int_0^{DT} V_m(t)dt$
- 定義：
  - T_s為PWM週期時間
  - $\begin{cases} V_1(t) = V_m - I_{AC}R_s \\ V_2(t) = \frac{1}{T}\int_0^{DT} V_m(t)dt \end{cases} \quad 0 < t < T_s$

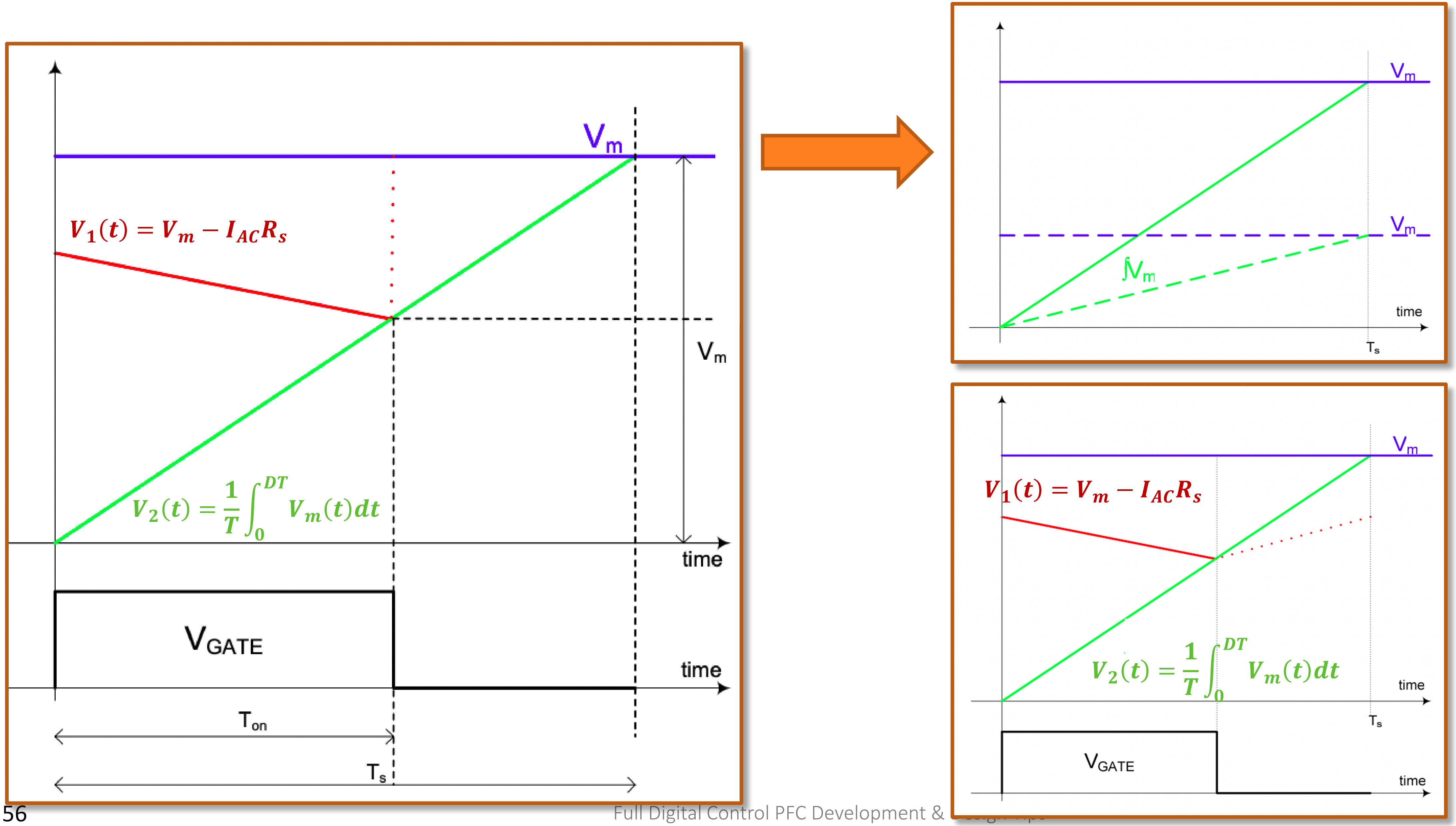
[redacted]
MICROCHIP

OCC(One Cycle Control) PFC



- $V_{AC} = I_{AC} * R_e$, R_e = PFC等效電阻
- CCM Boost Converter:
  - $V_{AC} = V_O * (1\text{-}D)$, D = Duty Cycle
  - $I_{AC} = (1\text{-}D) * V_O / R_e$
  - $I_{AC} * R_s = (1\text{-}D) * V_O * R_s / R_e$, R_s = 電感電流採樣電阻(增益)
  - $I_{AC} * R_s = (1\text{-}D) * V_m$, $V_m = V_O * R_s / R_e$
  - $V_m - I_{AC} * R_s = D * V_m = \frac{1}{T}\int_0^{DT} V_m(t)dt$
- 定義：
  - T_s為PWM週期時間
  - $$\begin{cases} V_1(t) = V_m - I_{AC}R_s \\ V_2(t) = \frac{1}{T}\int_0^{DT} V_m(t)dt \end{cases} \quad 0 < t < T_s$$

OCC(One Cycle Control) PFC

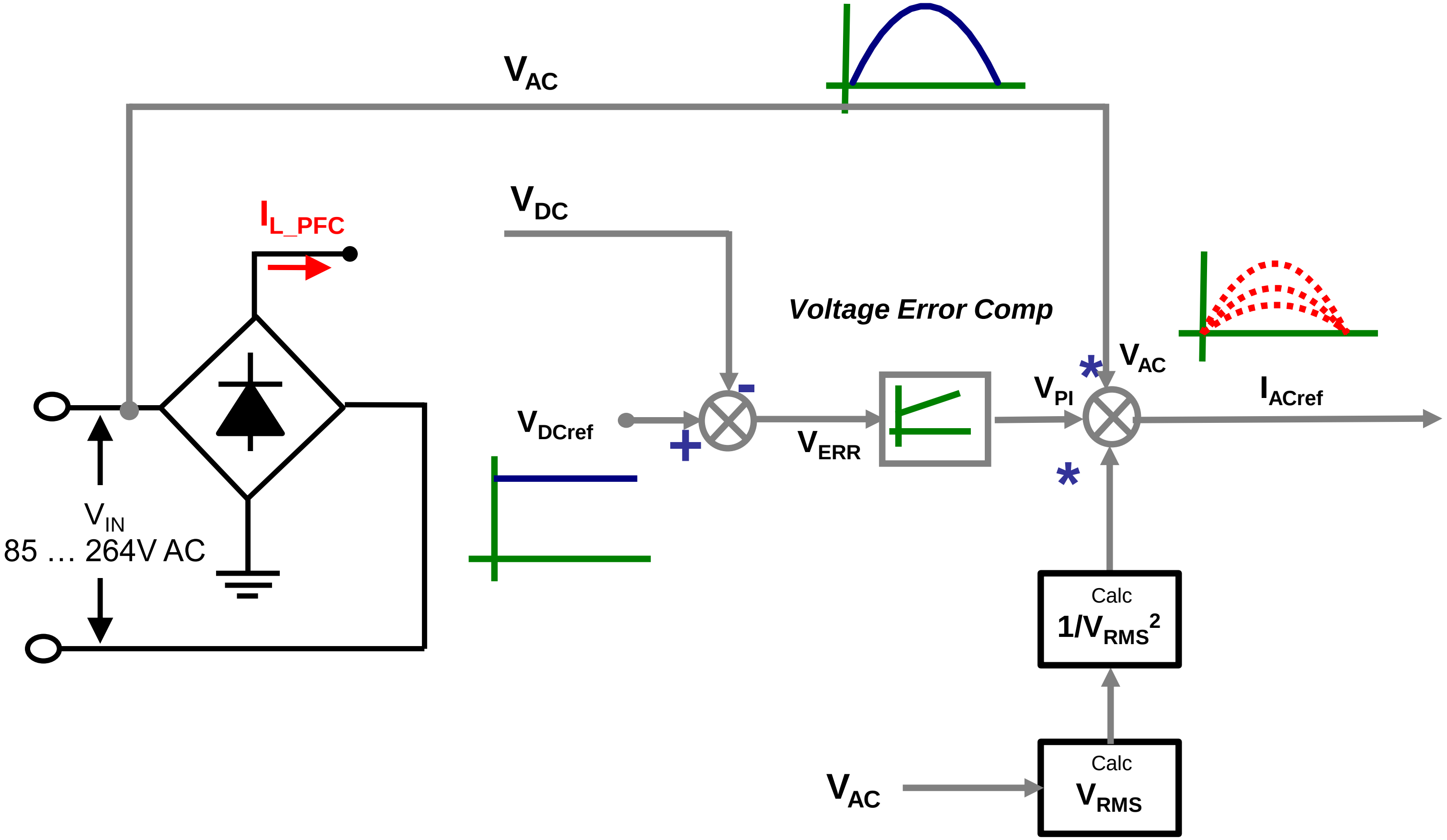


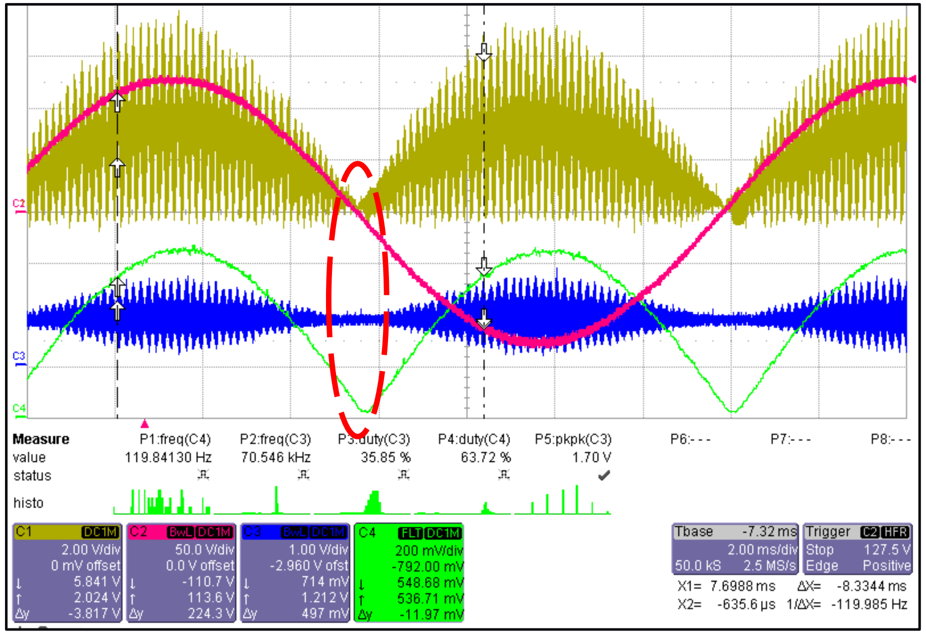
OCC(One Cycle Control) PFC

- 透過單週期控制法，**PFC**不需要量測輸入電壓也能控制**PFC**

- 單週期控制法是延伸基本電感公式所開發出來，其適用範圍不侷限於**PFC**，其他架構也能使用。

Vac Feedback Signal Distortion



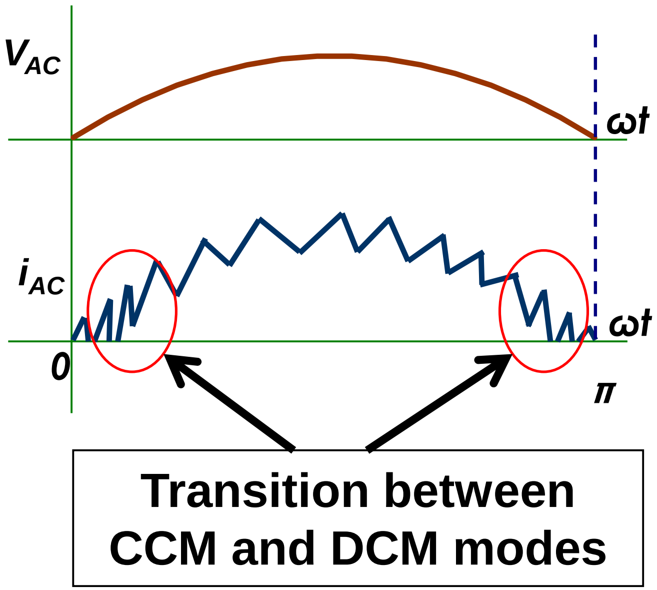


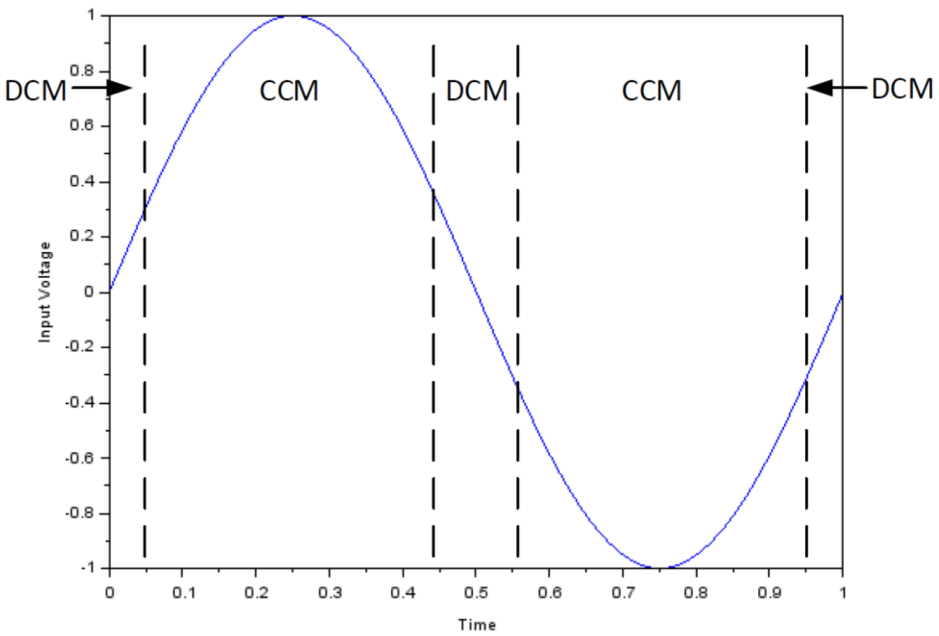
C1 (yellow):	IL
C2 (red):	VAC_IN
C4 (green):	Vac Reference (DAC Output)

Time Base: 2 ms/div

Discontinuous Mode of Operation

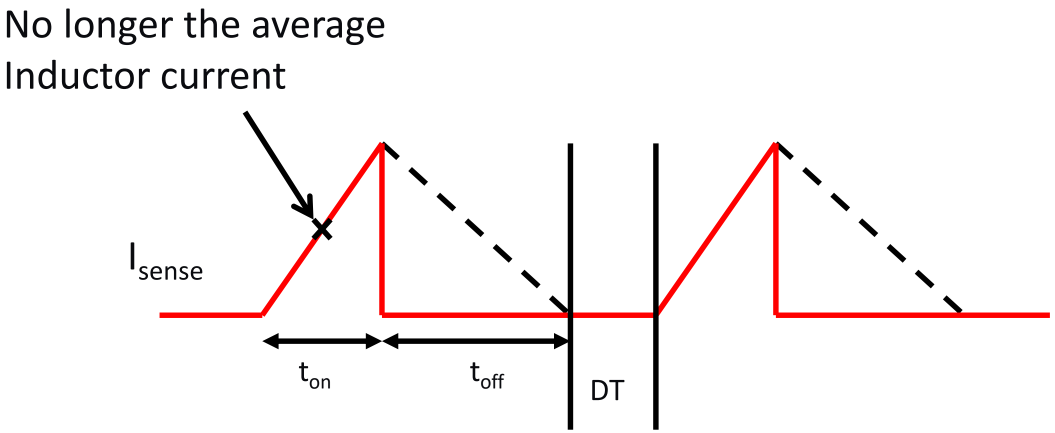
- **VAC varies from 0V to VAC(PK) on every sine wave cycle causing boost converter to operate in DCM (occurs near zero crossings and depends on load)**
- **The Boost Converter will operate in DCM when:** $i_{AC} < \dfrac{\left(V_{AC} \cdot D \cdot T_S\right)}{2L}$





Discontinuous Mode of Operation

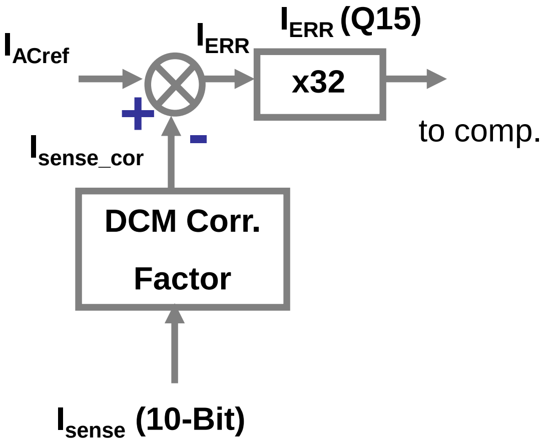
- **When inductor current becomes discontinuous the current sampling point (PDC/2) is no longer the average inductor current**
- **With the CT in series with boost MOSFET, we only see ton current. Additional circuitry is needed to see when inductor current reaches zero to determine t_{off}**



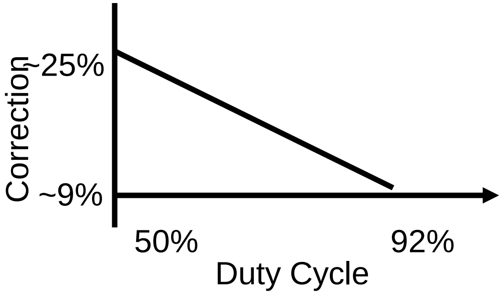
$$I_{sense\_avg} = \frac{I_{sense\_pk}}{2} * (t_{on} + t_{off}) f_s$$

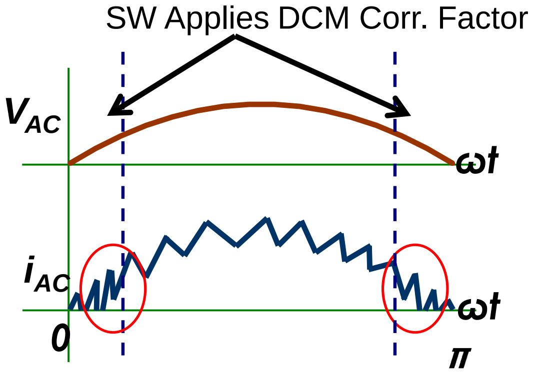
DCM Correction - I

- **Add a correction factor in the current control algorithm to account for the measured inductor current not being the average.**
- **Proposed solution is to modify the sense current (I_{sense}) with respect to the V_{ac}, V_{out}, and compensator output.**



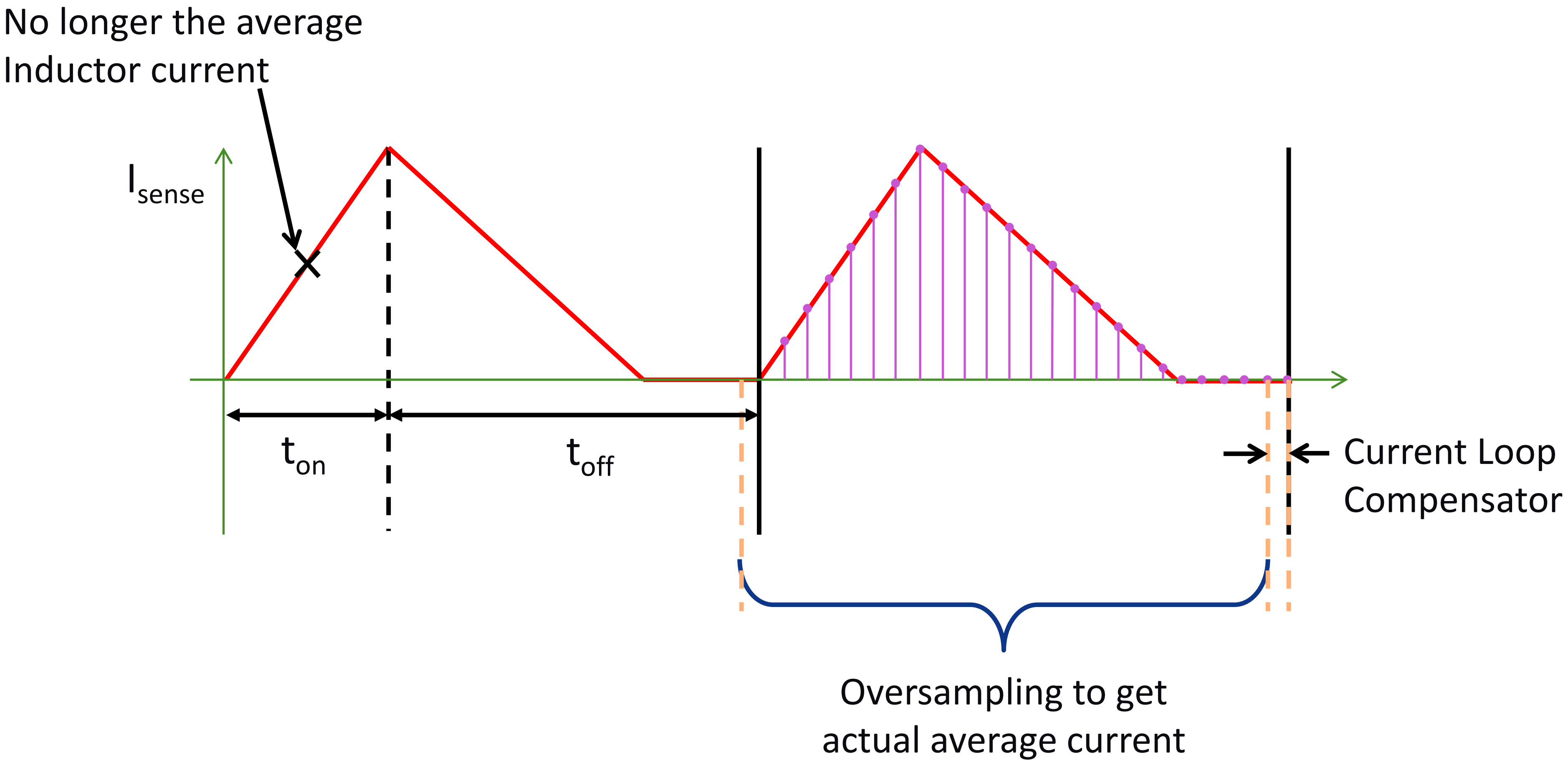
$$I_{sense\_cor} = \frac{V_{out}}{V_{out} - V_{AC}} * Comp_{out} * I_{sense}$$





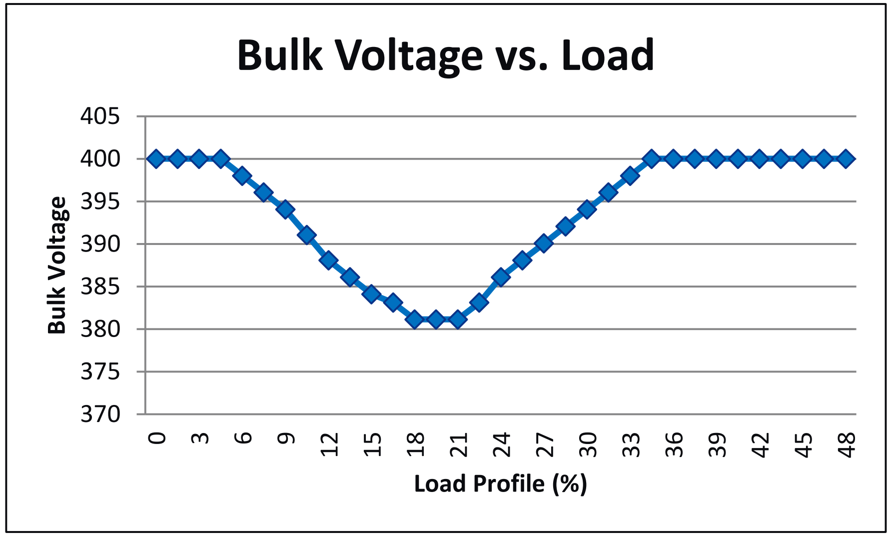
DCM Correction - 2

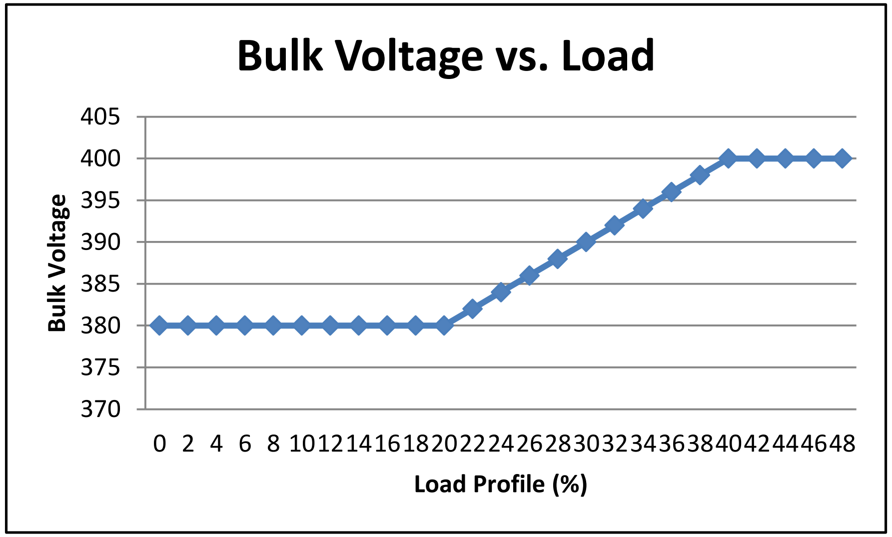
- **Using Over-sampling Feature**



Adaptive Bulk Voltage

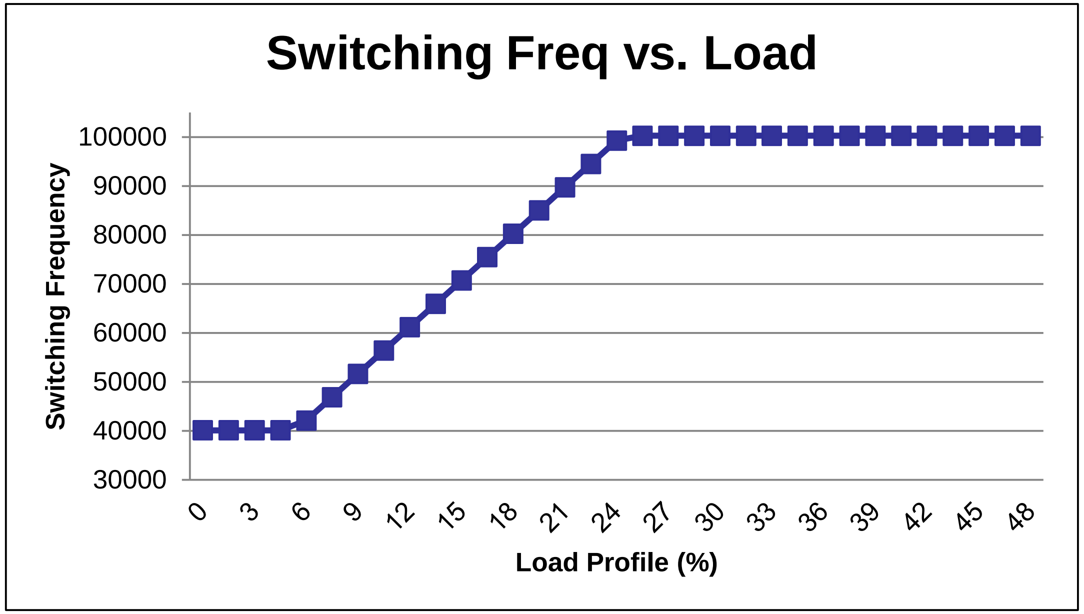
- **At light loads the bulk voltage is reduced to improve efficiency by reducing the switching losses**
- **Output bulk voltage reference can be increased as soon as a load transient is detected**
- **For large load transients, bulk voltage "boost" can be added to improve transient response – control loop coefficients are modified**





Adaptive Switching Frequency

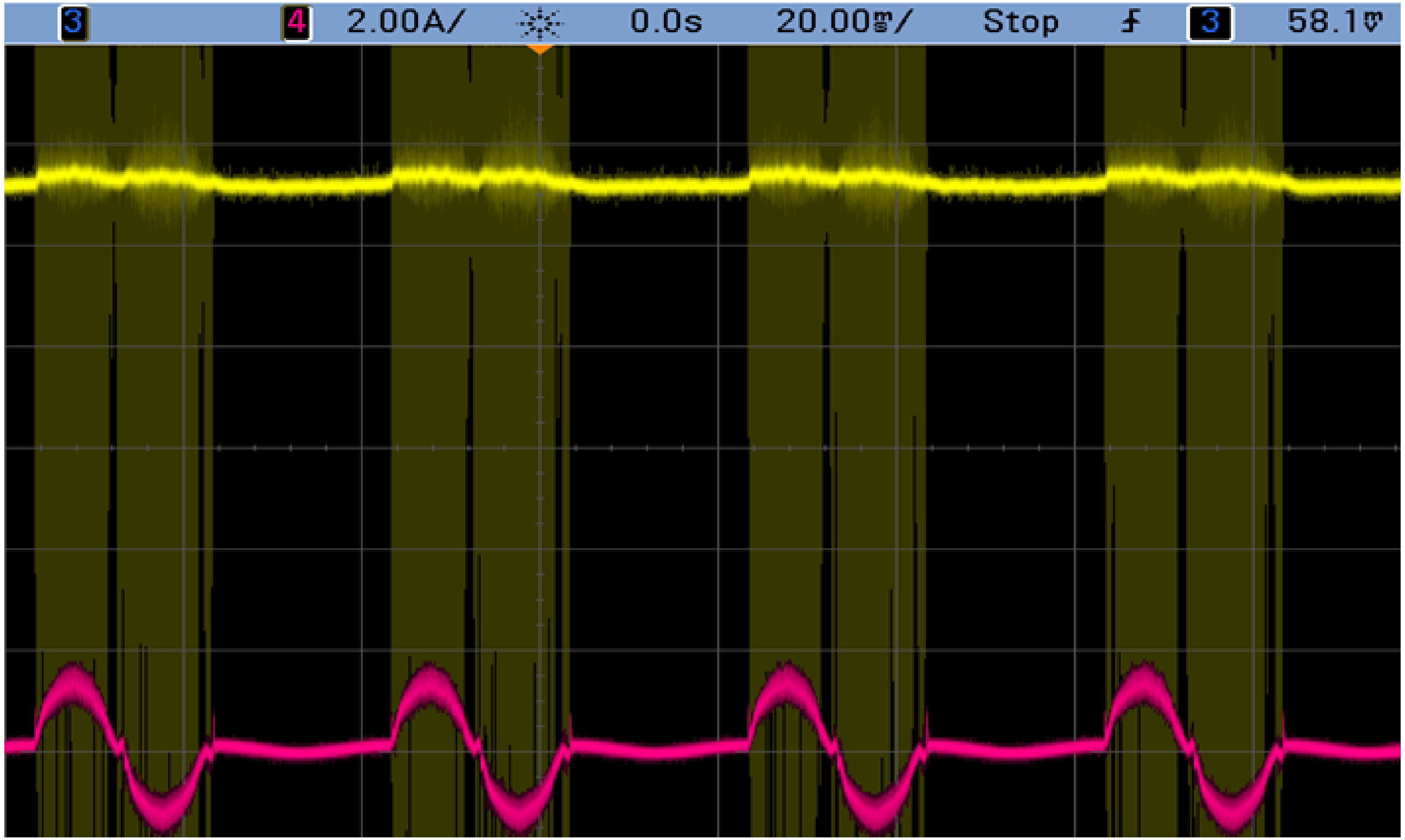
- **To improve system efficiency even further at light load conditions, the switching frequency can be reduced**
- **When a load transient is detected, frequency is instantly increased to nominal frequency to maintain good response**
- **Additional algorithms are required for handling frequency change**



Burst Mode

Voltage Loop compensator output

AC current



Test condition: Low line and less than 5% load

Light Load Current iTHD

- **In very light load conditions majority of the input current goes into the X-capacitors in the EMI filter**
  - Because we used a CT in the switch path, we do not see this current drawn from the source and as a result our THD will suffer
  - We can add a routine that compensates for this current
    - We know the capacitance, input frequency, and input voltage
    - We can calculate in real time how much current is going into the X-caps and compensate (add) this to our current reference
- **Might also find that certain harmonics are being drawn by the system and again the control loop is not accounting for them**
  - Can add current harmonic injection routine into the current loop compensator that will the reduce the percentage of current drawn at these harmonics

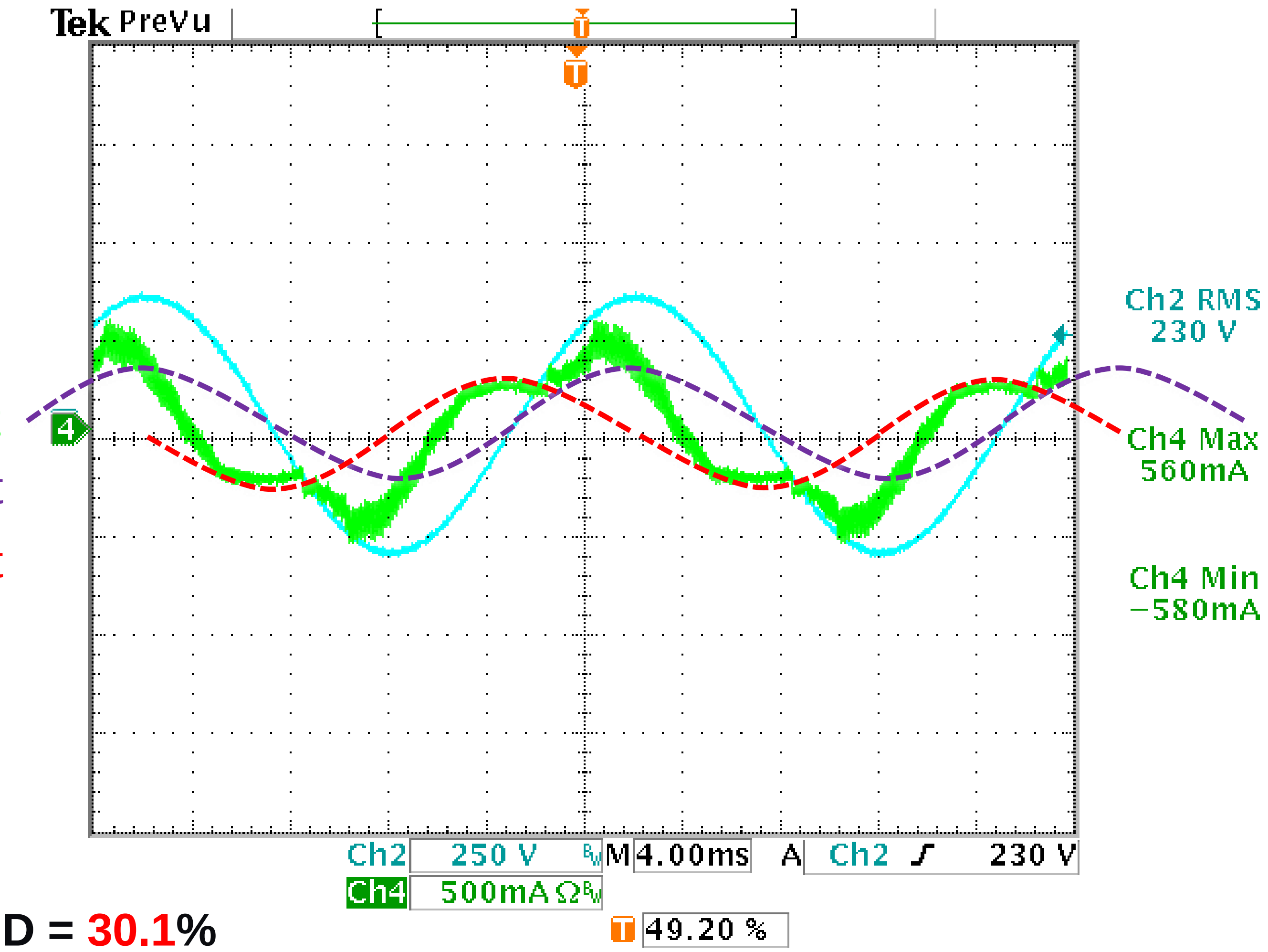
Light Load Current iTHD

Input Voltage

Input Current

Inductor Current

EMI Filter Current



P.F = 0.701, iTHD = 30.1%

X Cap. = 2x 0.47uF + 1x 1.5uF = 2.44uF

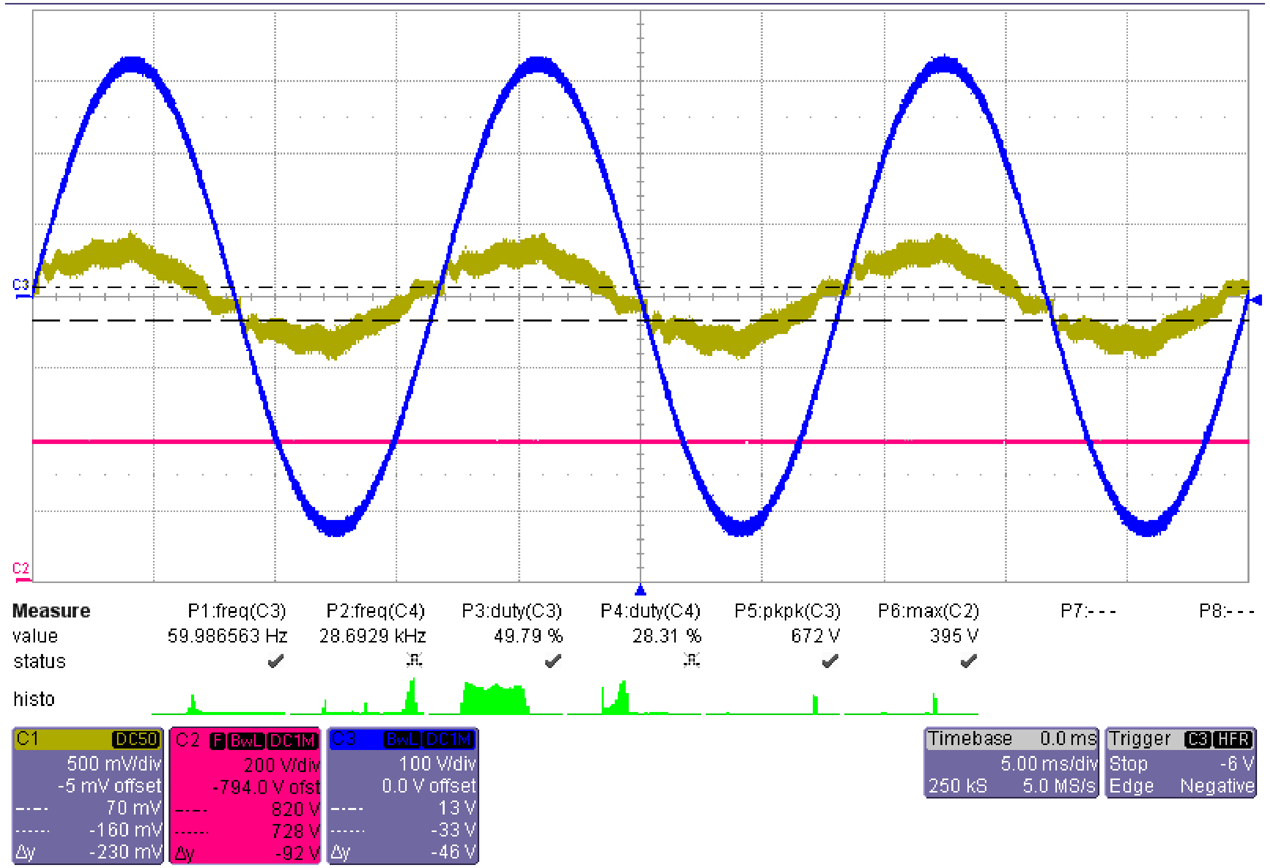
MICROCHIP

Light Load Current iTHD

Input Voltage

Input Current

DC Bus



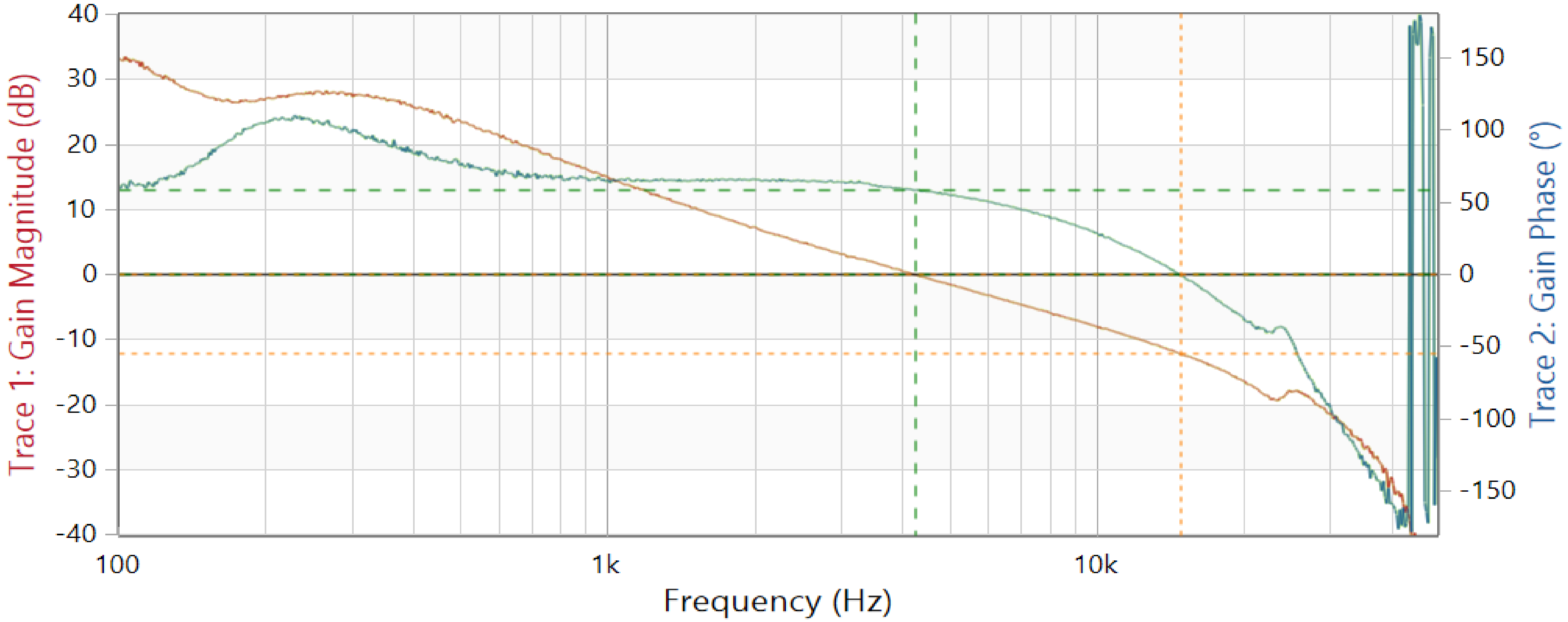
P.F = 0.936, iTHD = 10%

X Cap. = 2x 0.47uF + 1x 1.5uF = 2.44uF

[redacted]

What if impedance of PFC is not zero?

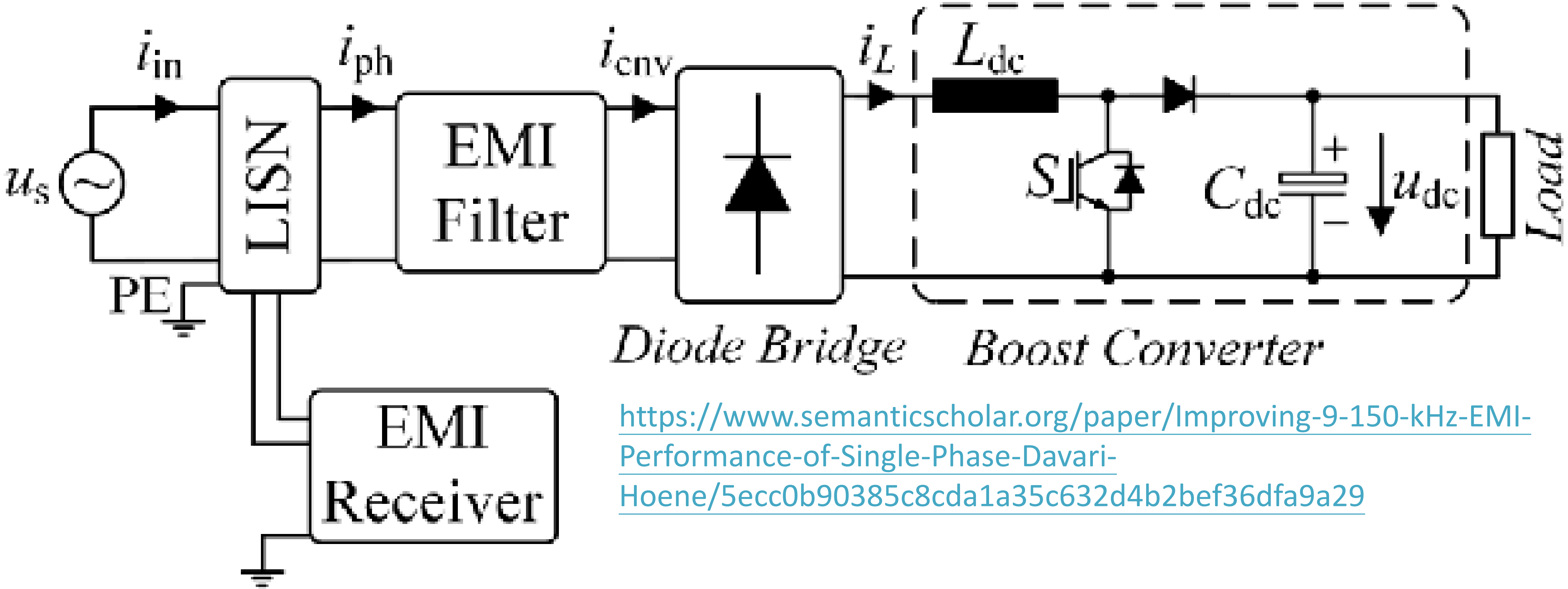
- **PFC-Inner Loop measurement**



[redacted]

What if impedance of PFC is not zero?

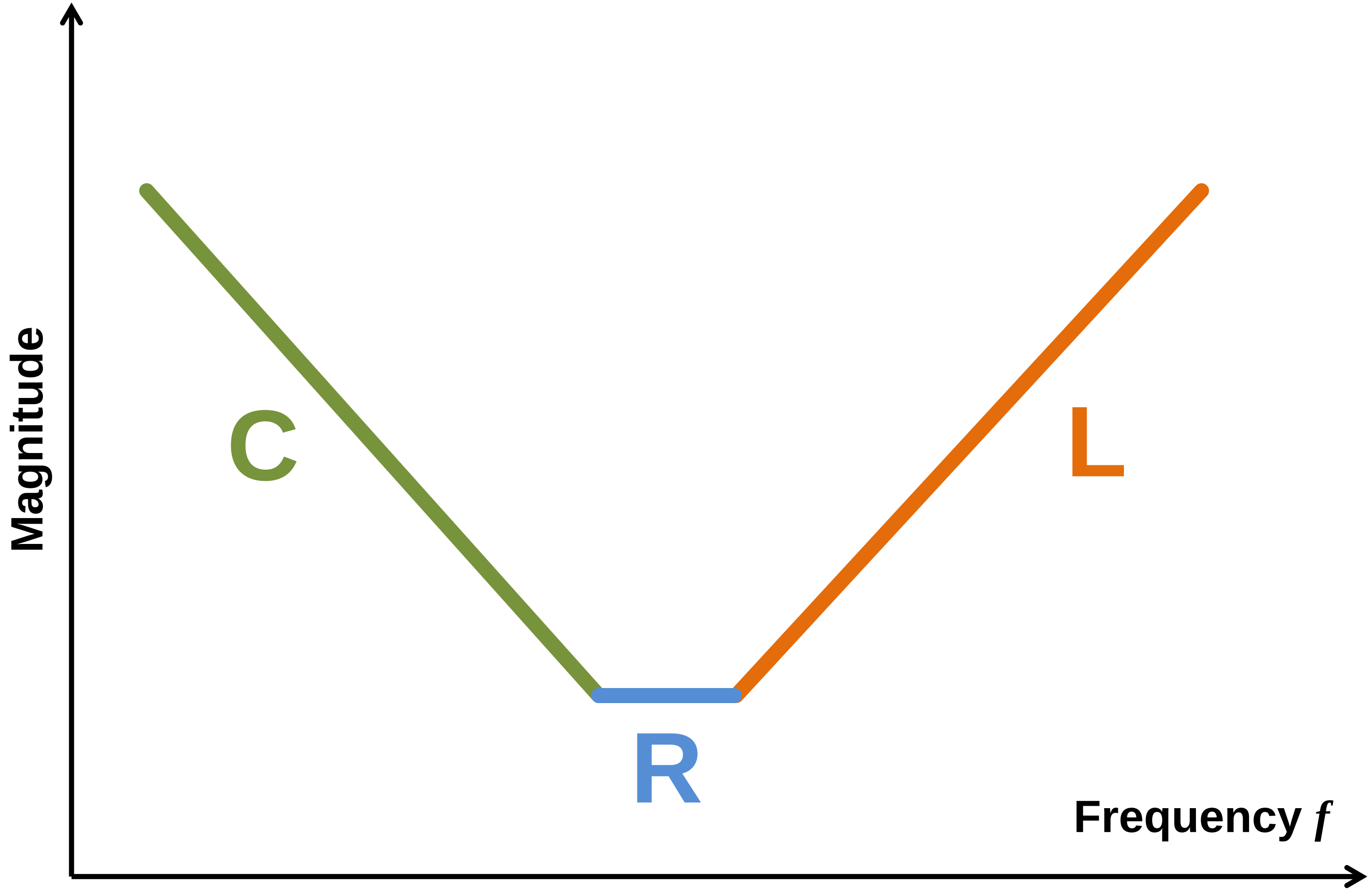
- **Block diagram of a single-phase boost PFC converter including LISN and EMI receiver.**



https://www.semanticscholar.org/paper/Improving-9-150-kHz-EMI-Performance-of-Single-Phase-Davari-Hoene/5ecc0b90385c8cda1a35c632d4b2bef36dfa9a29

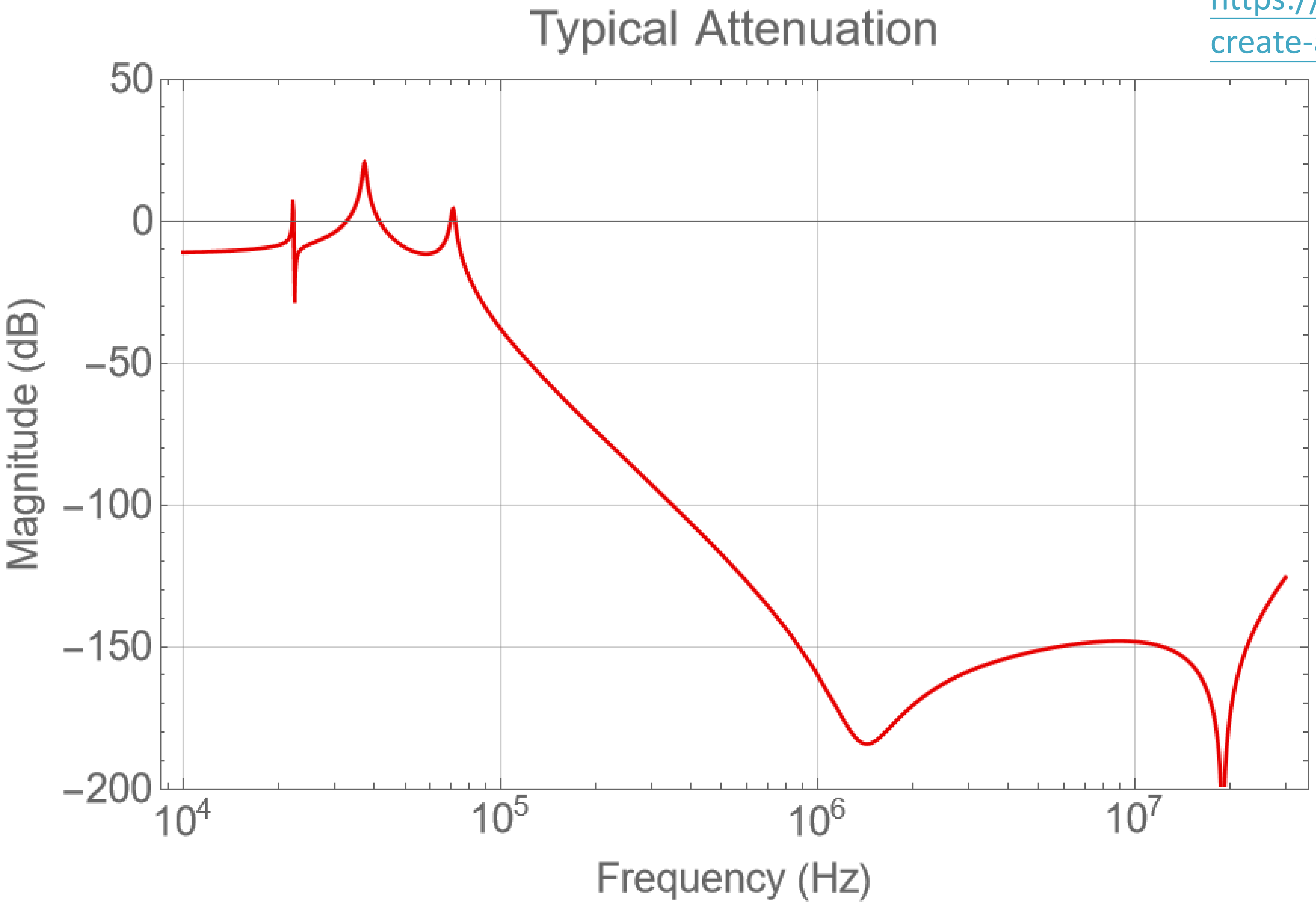
Impedance

Impedance is a combination of capacity, resistance and inductance where the absolute value is determined by the frequency



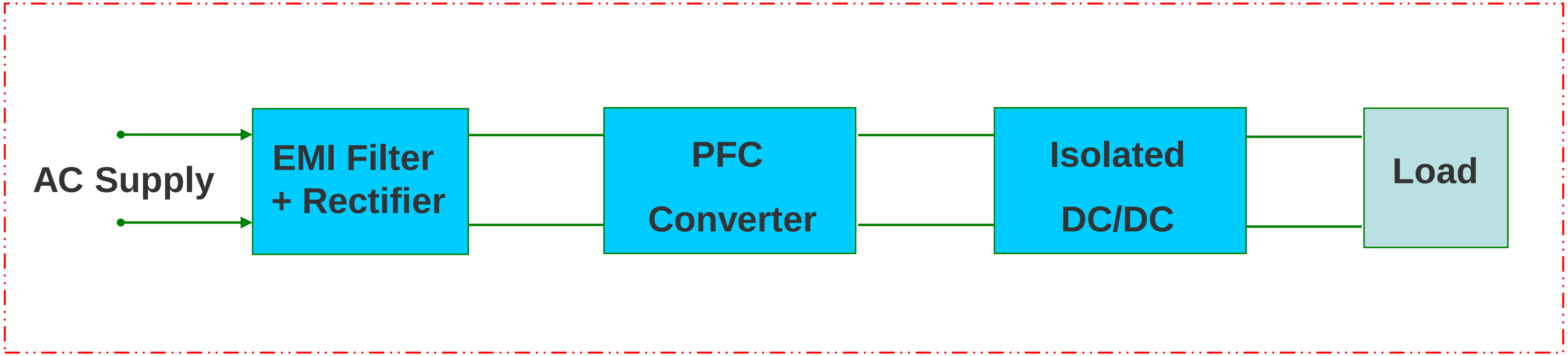
Typical EMI filter attenuation

https://www.ednasia.com/how-parasitics-create-an-unexpected-emi-filter-resonance/



Input Ripple Rejection

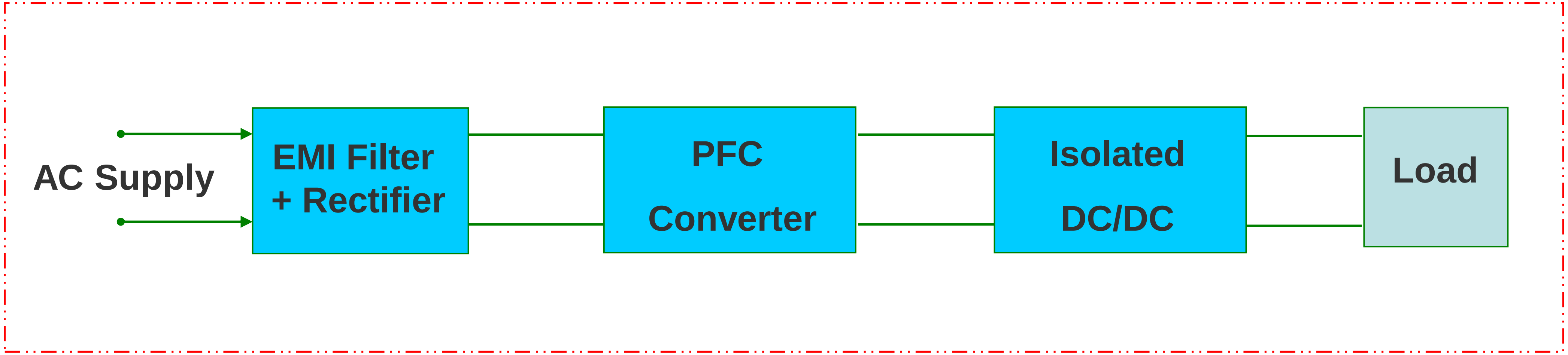
- **General power supply block diagram:**



- **The questions:**
  - Can the DC/DC converter reject the ripple from PFC output?
  - How to calculate the ripple reduction with DC/DC converter?

Input Ripple Rejection

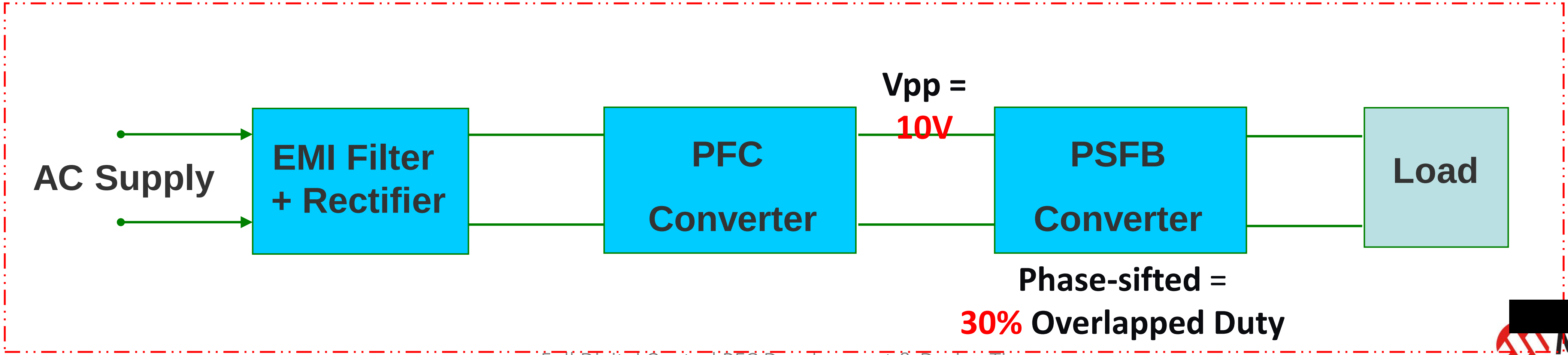
- **Can the DC/DC converter reject the ripple from PFC output?**
  - Yes, but… not to ZERO.



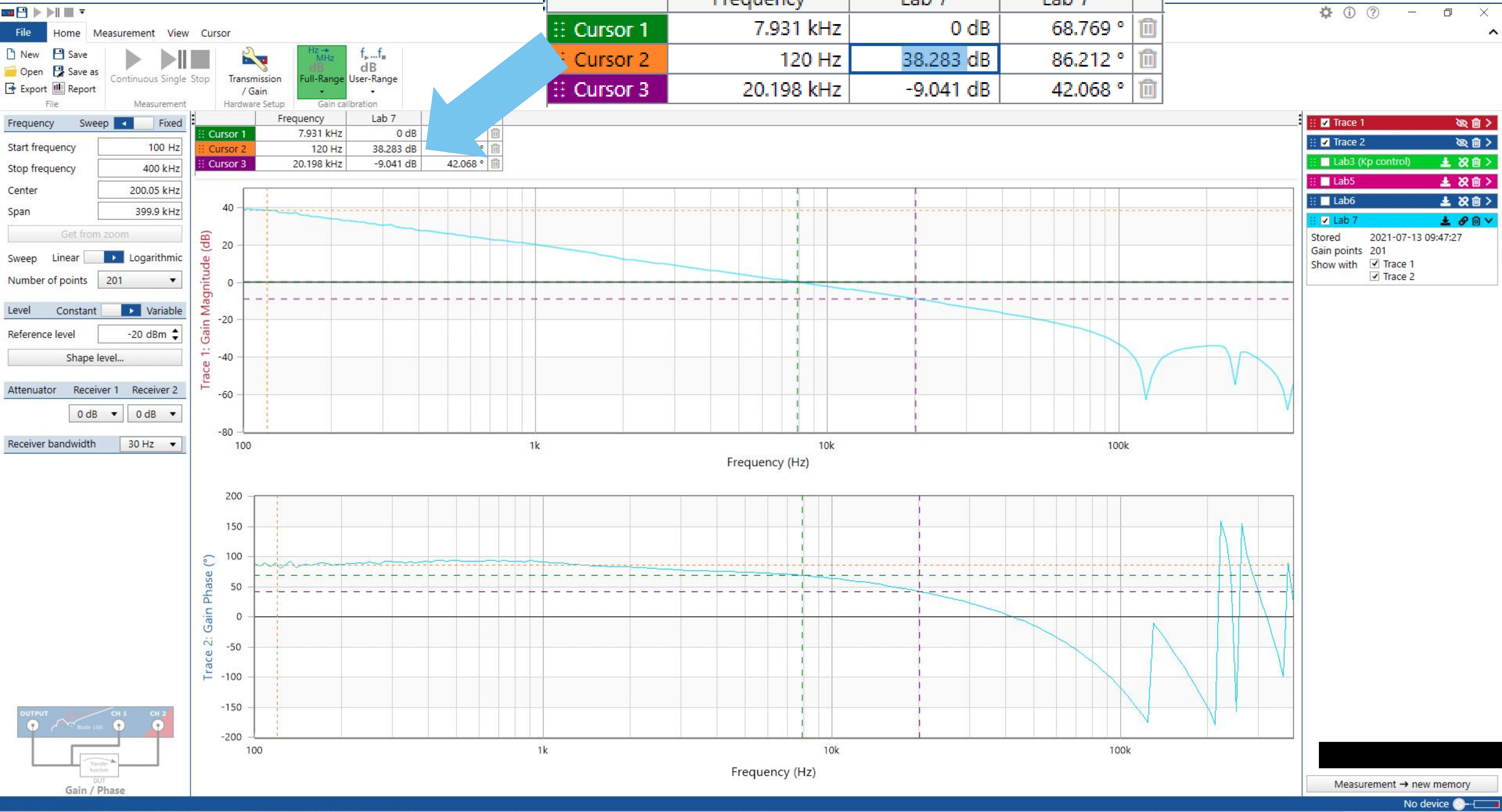
Input Ripple Rejection

- **How to calculate the ripple reduction with DC/DC converter?**
  - For example: PFC + Phase-sifted Full Bridge DC/DC
    - Input ripple: 100Hz or 120Hz **Vpp = 10V**
    - **30% Overlapped Duty** **=>** Duty cycle gain = 20 x $\log_{10}$ (30%) = 10.5dB
    - **Turn ratio Np : Ns = 20 : 1** **=>** Turn ratio gain = 20 x $\log_{10}$ (1/20) = 26dB
    - **Total reduction gain** = 10.5+26 = 36.5dB
    - Output ripple WITHOUT loop compensator

      = 10V / **Total reduction gain** = 10V / 66.8 = **150mV**

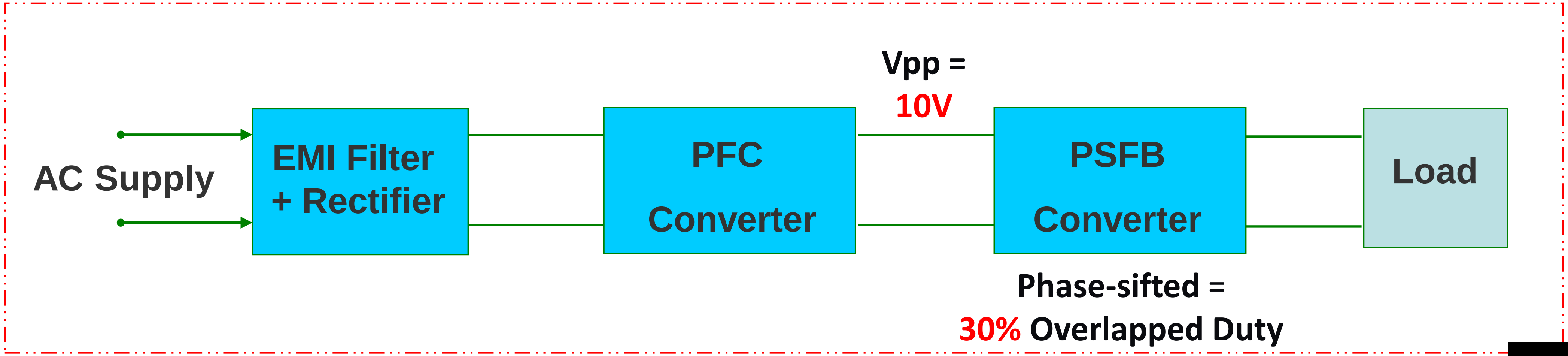


	Frequency	Lab 7	Lab 7
Cursor 1	7.931 kHz	0 dB	68.769 °
Cursor 2	120 Hz	38.283 dB	86.212 °
Cursor 3	20.198 kHz	-9.041 dB	42.068 °



Input Ripple Rejection

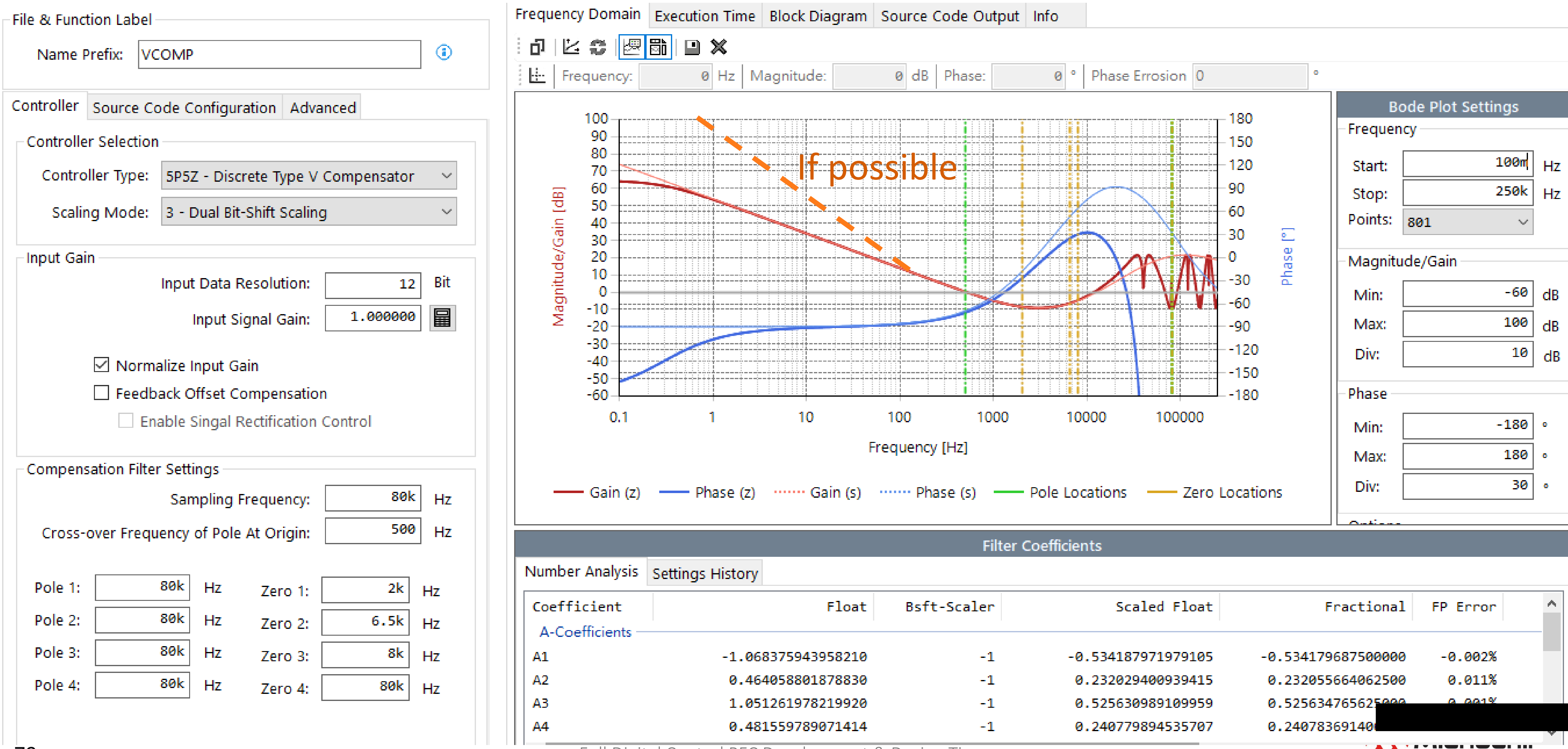
- **How to calculate the ripple reduction with DC/DC converter?**
  - For example: PFC + Phase-sifted Full Bridge DC/DC
    - **Total reduction gain** = 10.5+26+38.283 = 75dB
    - Output ripple WITH loop compensator
      = 10V / **Total reduction gain** = 10V / 5623 = **1.78mV**
    - Ripple improvement:
      - **150mV => 1.78mV**



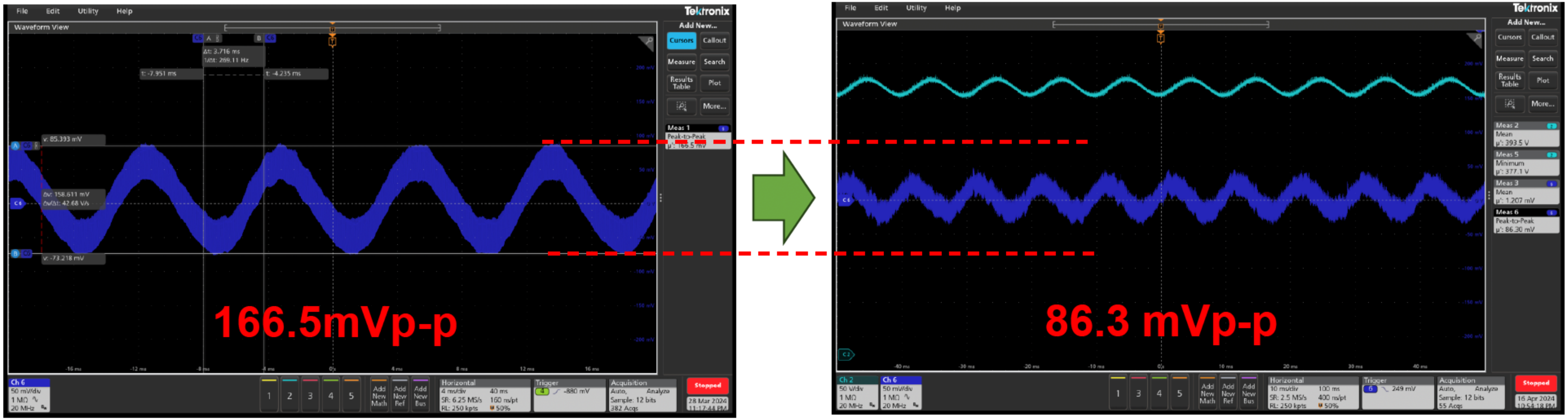
Not The End

- **150mV => 1.78mV is not the end because of more conditions:**
  - Duty Cycle Gain would not be fixed
  - Component tolerance => Gain tolerance
  - PWM resolution
  - Feedback resolution
  - Compensator resolution
  - etc…
- **A question for you…**
  - Can control-loop of DC/DC converter ask for more?

Low Freq Gain Improvement



Input Ripple Rejection Improvement @ Full Load



3P3Z Controller at 100%Load

Gain about **10db** (100~500hz)

6P6Z Controller at 100%Load

Gain increase about **35db** (100~500hz)

Microchip
Digital Power Solutions

[redacted]

PIC16(L)F176X/177X Family

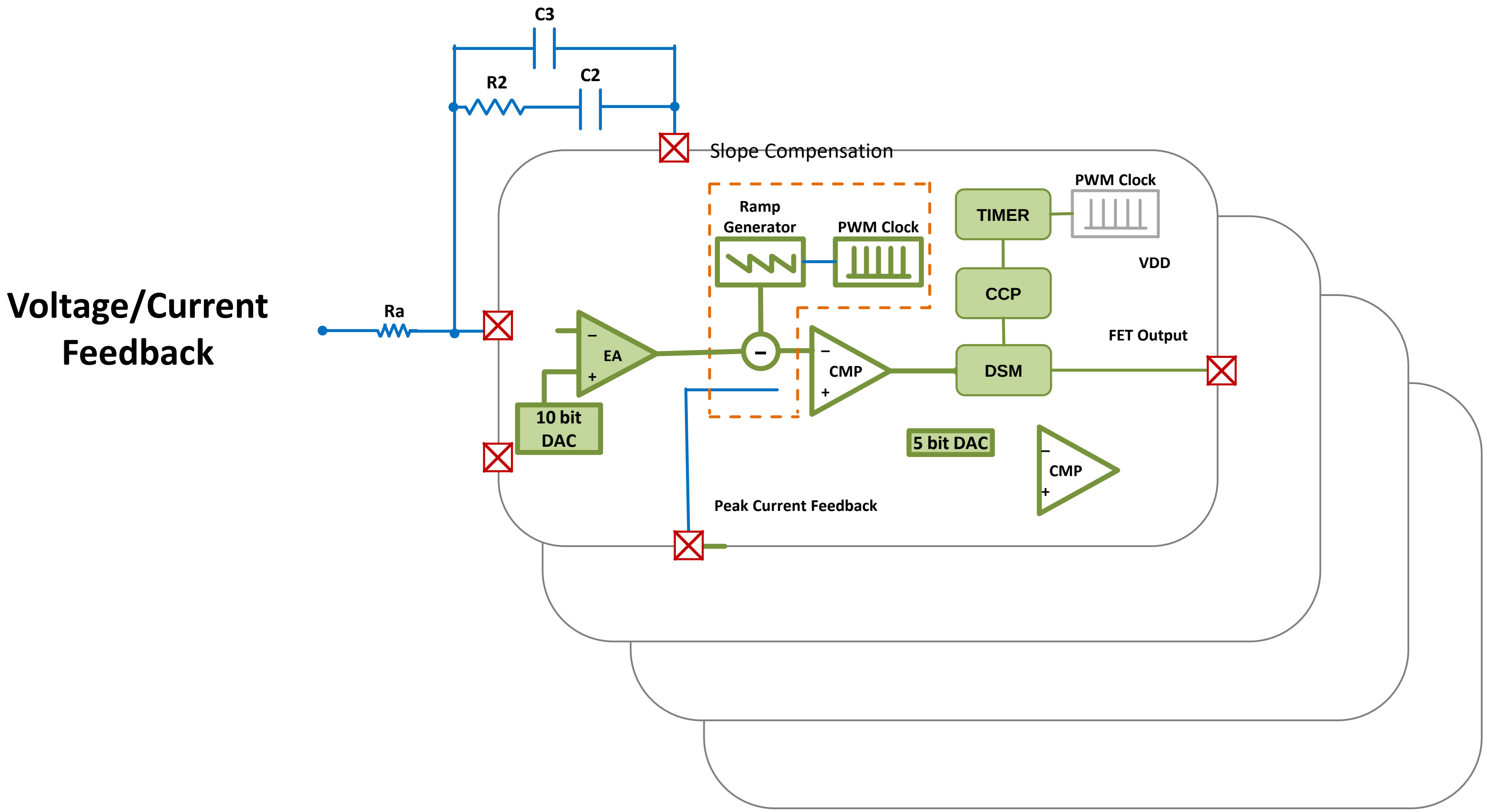
Intelligent Analog Integration with XLP

Features / Memory

	Single String	Dual String/ Dual Converter	Quad String/ Quad Converter
			PIC16F177x 28KB / 2048B / 512EE 16x10-bit A/D 3/4x SMPS & Lighting Peripheral Set, ZCD, CLC
	PIC16F1765 14KB / 1kB / 128EE 8x10-bit A/D 1x SMPS & Lighting Peripheral Set, ZCD, CLC	**PIC16F1769** 14KB / 1kB / 128EE 12x10-bit A/D 2x SMPS Lighting Peripheral Set, ZCD, CLC	**PIC16F177x** 14KB / 1024B / 128EE 16x12-bit A/D 3/4x SMPS & Lighting Peripheral Set, ZCD, CLC
	PIC16F1764 7KB / 512B / 128EE 8x10-bit A/D 1x SMPS & Lighting Peripheral Set , ZCD, CLC	**PIC16F1768** 7KB / 512B / 128EE 12x10-bit A/D 2x SMPS Lighting Peripheral Set, ZCD, CLC	**PIC16F177x** 7KB / 512B / 128EE 16x12-bit A/D 3/4x SMPS & Lighting Peripheral Set, ZCD, CLC
	14 Pin	20 Pin	44 Pin

[redacted]

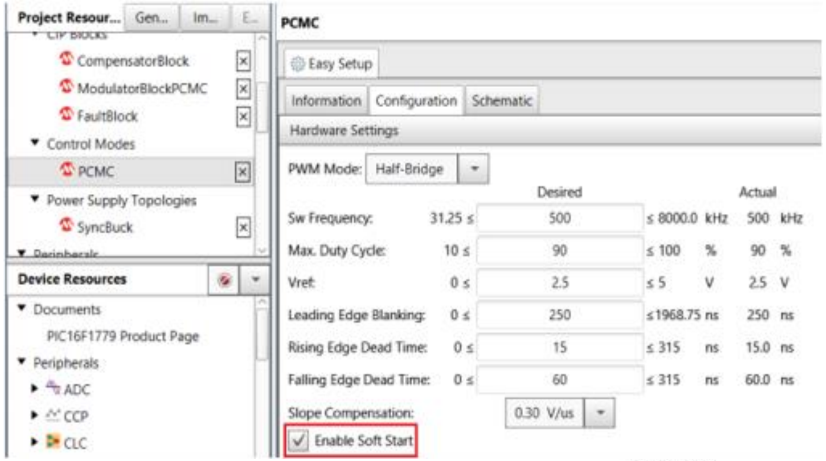
1,2,3 and 4 Channel Drive

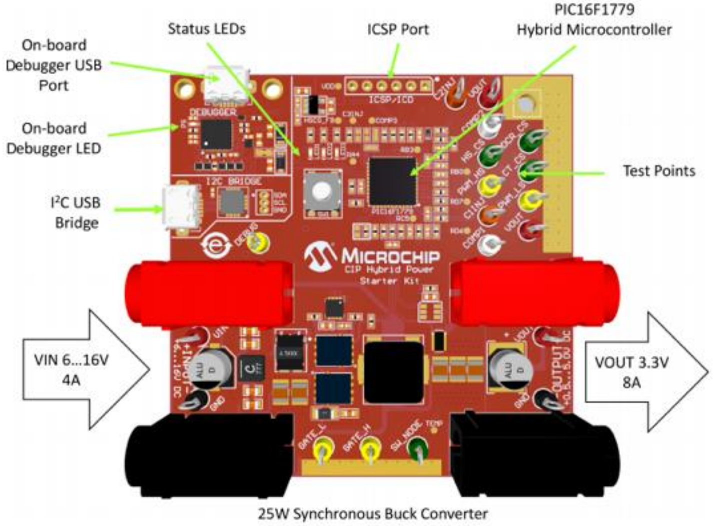


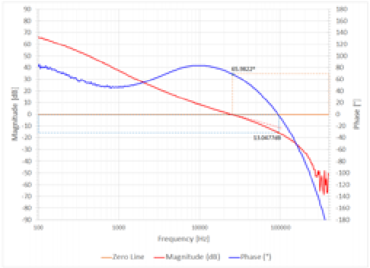
PIC16(L)F176X/177X Family

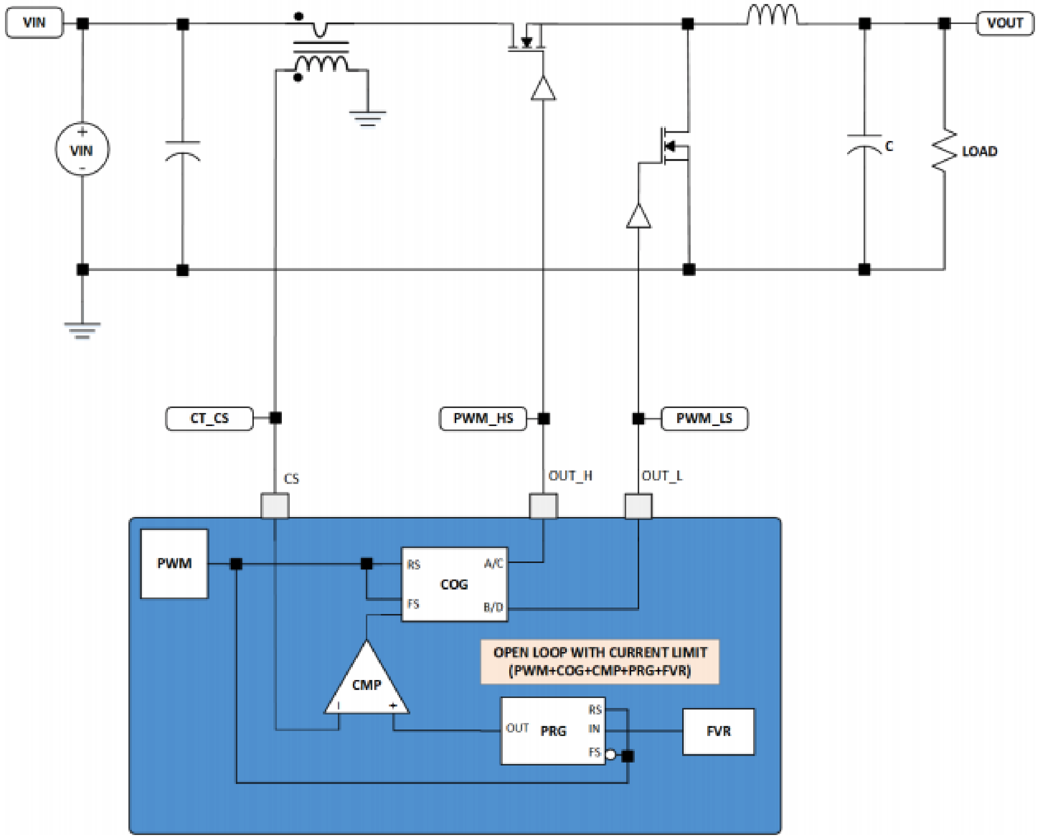
Development Tools

25W CIP Hybrid Power Starter Kit









Automotive Exterior Lighting

15W SEPIC LED Driver

- **Technical Data:**
  - V_{IN}: 6…45V
  - V_{OUT}: 3…50V
  - I_{OUT}: 100 … 700 mA
  - P_{MAX}: 15 W
  - f_{SW}: 350 kHz
  - f_{DIMM}: 200 … 2,000 Hz

- **Special Features:**
  - Binning
  - Temperature Monitoring
  - Over Temperature Power Derating & Shut Down
  - High Resolution Weber-Fechner Dimming
  - Progressive Spread Spectrum Modulation
  - Enhanced Diagnostics & Fault Handling
  - Active, independent Fault States

Generic Automotive Exterior Lighting Signaling LED Driver for Daytime Running Lights, Turn Signals, Fog Lights and Signatures in Headlights

Part-No.: ***APP-EDF19-1***

Automotive Exterior Lighting

15W SEPIC LED Driver

http://ww1.microchip.com/downloads/en/Appnotes/AN3343-MCC-SMPS-Lib-Config-for-SEPIC-LED-Driver-Demo-Board.pdf

AN3343

MICROCHIP AN3343

MCC SMPS Library Configuration for SEPIC LED Driver Demo Board

Introduction

Author: Kristine Angelica Sumague, Microchip Technology Inc.

The Single-Ended Primary Inductance Converter (SEPIC) LED Driver Demo Board is a hardware platform designed to demonstrate the flexible control capabilities of Microchip's Core Independent Peripheral (CIP) hybrid power microcontroller. It is used in a Switched Mode Power Supply (SMPS) LED application. The board incorporates the PIC16F1769 as a freely programmable Power Management Integrated Circuit (PMIC) device, which will be programmed with the code generated using the MPLAB® Code Configurator (MCC) SMPS Library.

In this Application Note, the MCC SMPS Library is utilized for quick and easy configuration and code generation of peripherals used in the SEPIC LED Driver Demo Board. The MCC SMPS Library is a user-friendly add-on that needs to be installed on top of the MPLAB® X Integrated Development Environment (IDE) and MCC. This library generates drivers for controlling and driving the peripherals of CIP hybrid power microcontrollers based on the settings and selections made in its Graphical User Interface (GUI). For more information about the SEPIC LED Driver and MCC SMPS Library, refer to the SEPIC LED Driver Demo Board for Automotive Applications and MPLAB® Code Configurator Switch Mode Power Supply Library User's Guide.

Figure 1. SEPIC LED Driver Demo Board

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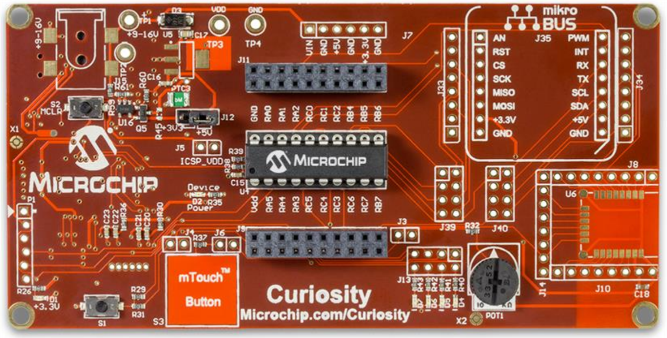
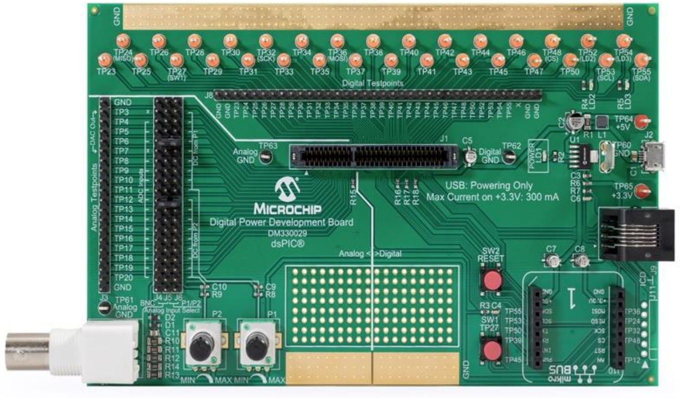
mikroBUS SR Buck

Power Click Board Rev 2.0

- Sync Buck Click Board Spec：
  - Vin = 9V
  - Vout = 3.3V
  - Iout = 1A
  - L = 33µH
  - C = 220µF ESR = 120 mΩ



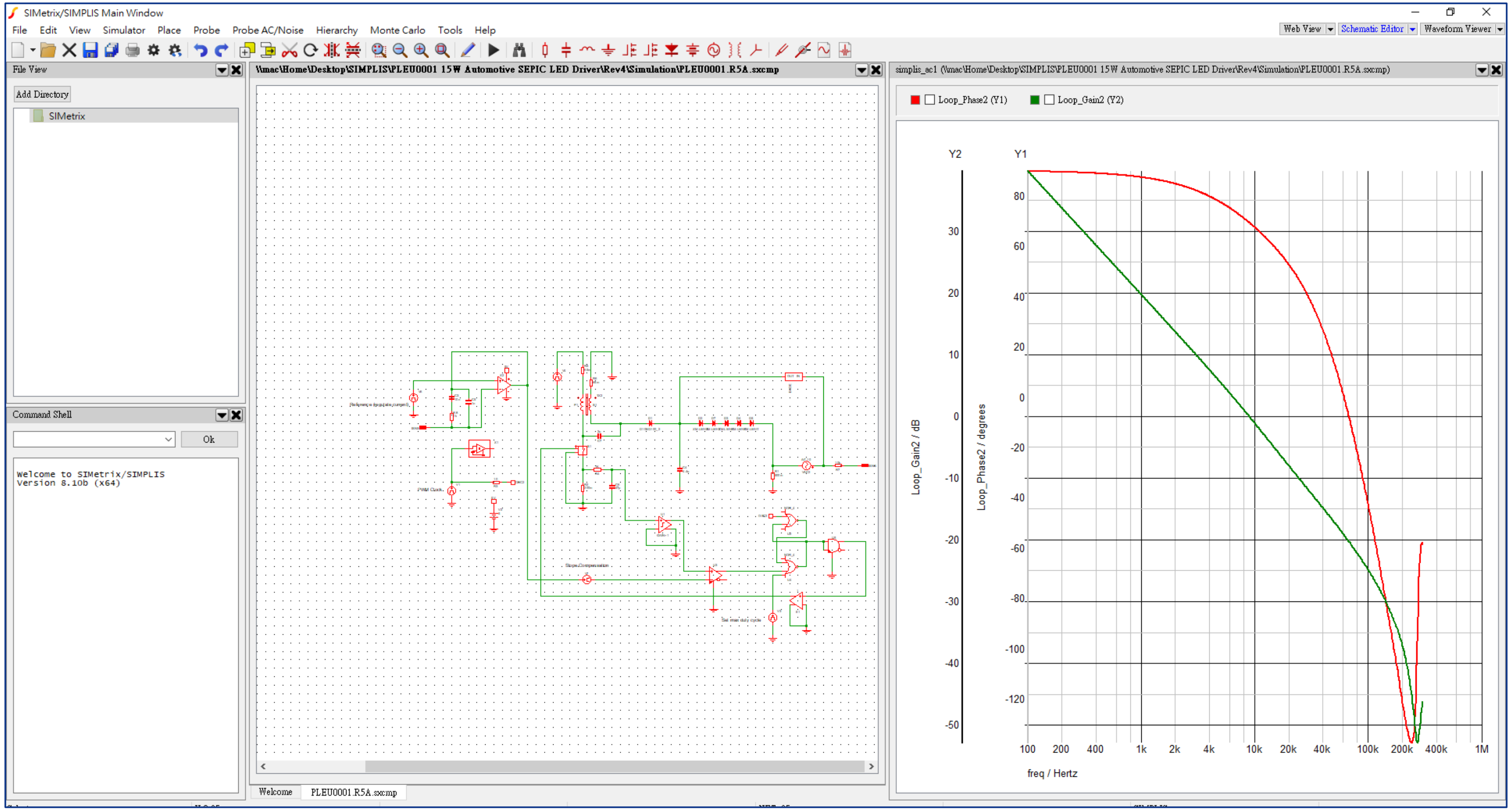


PIC16(L)F176X/177X Family

Development Tools

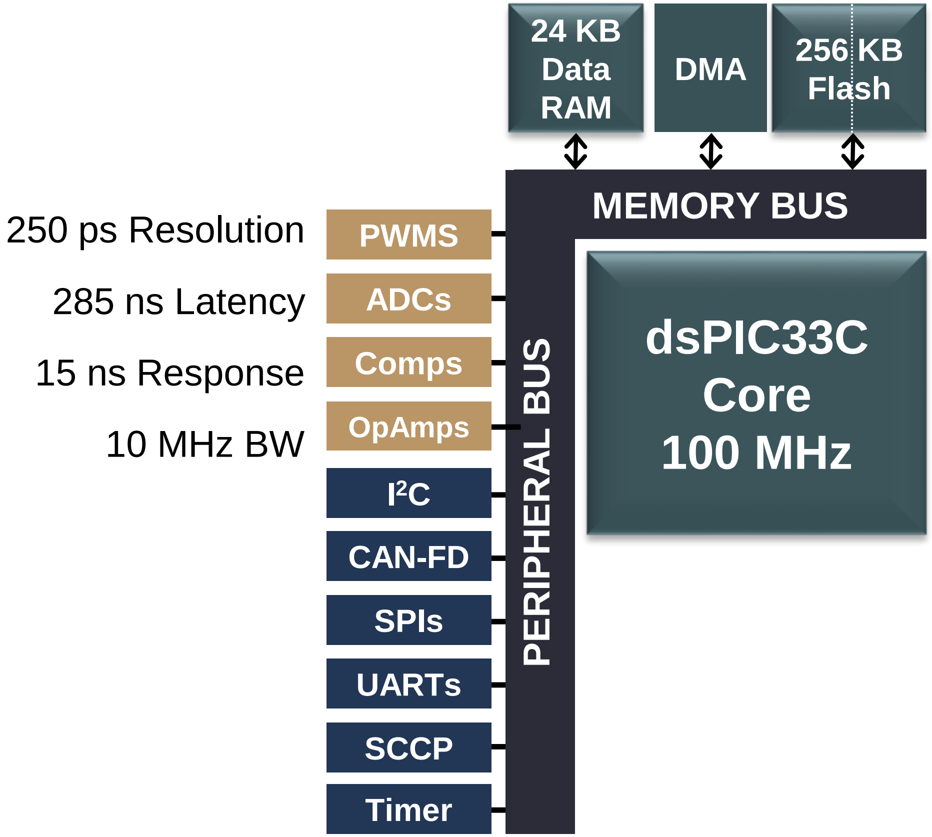
MPLAB® Mindi™ Analog Simulator

Enable analog circuit design with Microchip

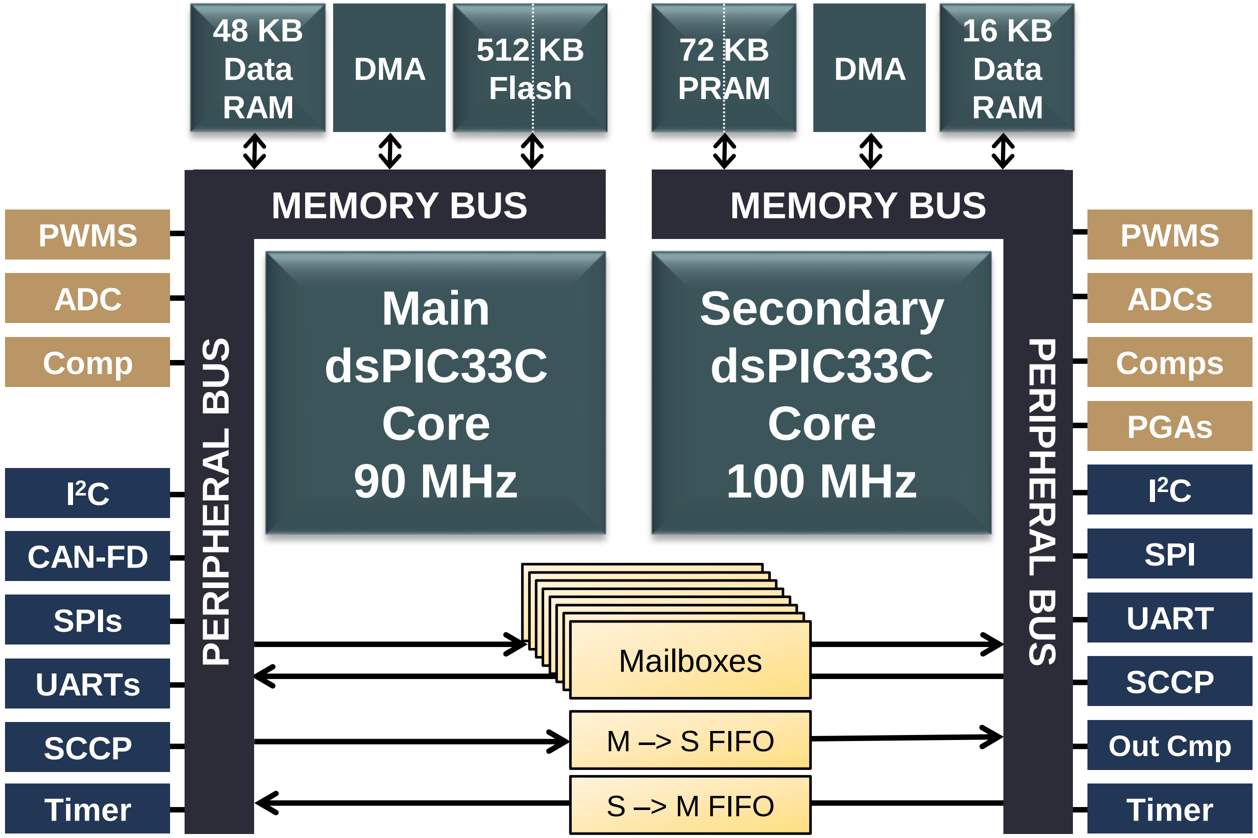


dsPIC33C Family

Single Core dsPIC33CK



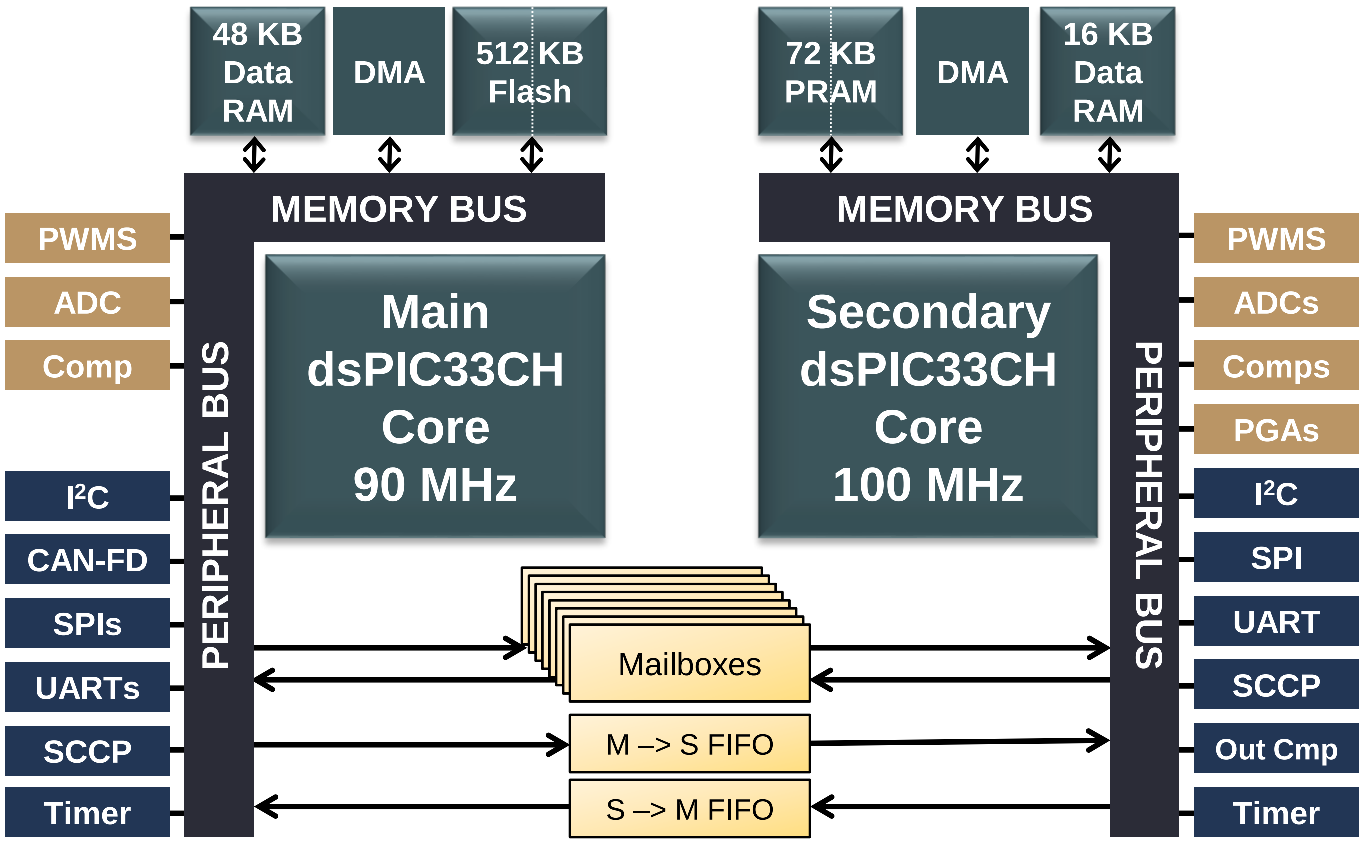
Dual Core dsPIC33CH



MICROCHIP

Main / Secondary Interface (MSI)

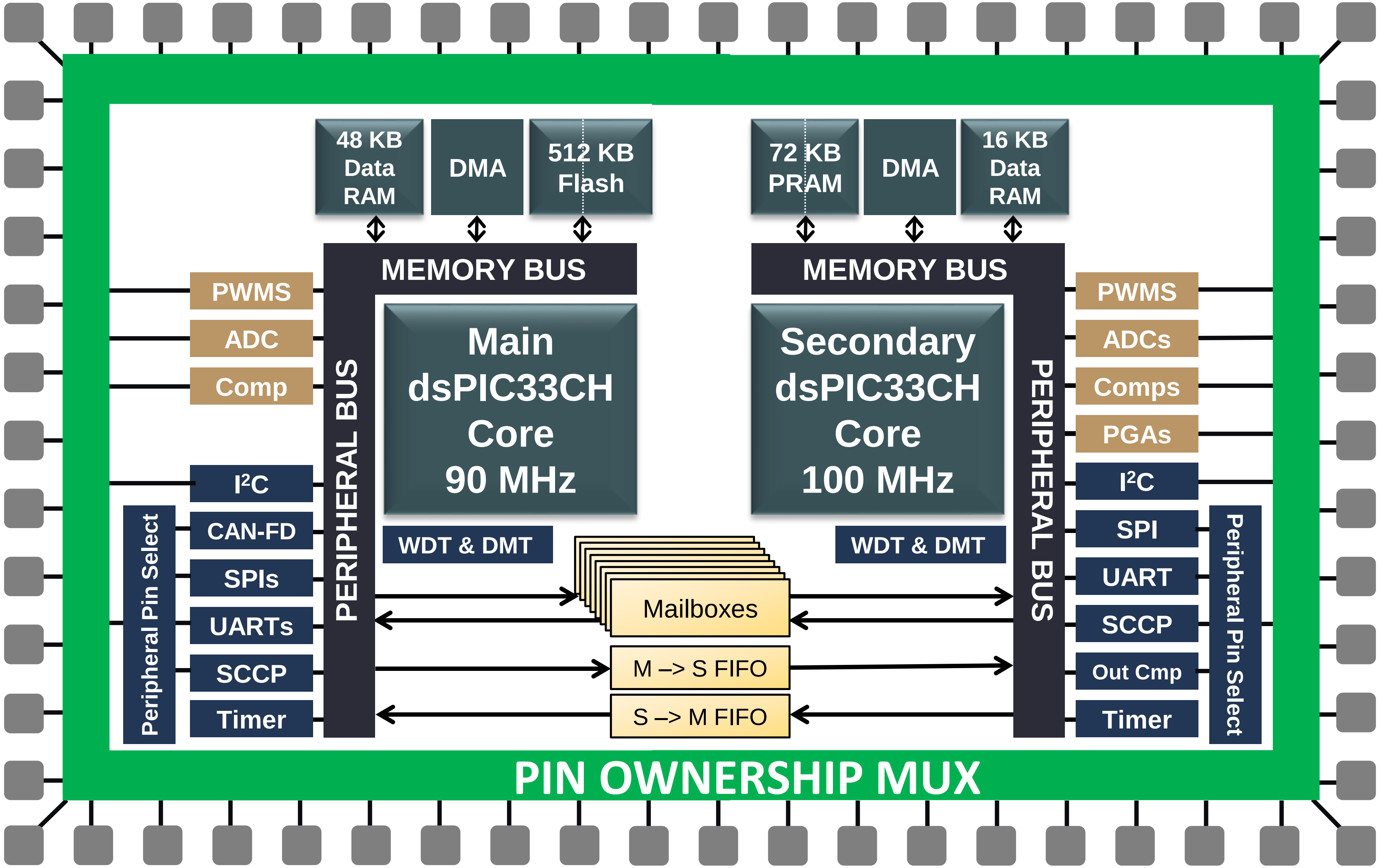
Example: dsPIC33CH512



Configurable direction for all 16 mailboxes
Configurable interrupt operation for mailboxes & FIFOs

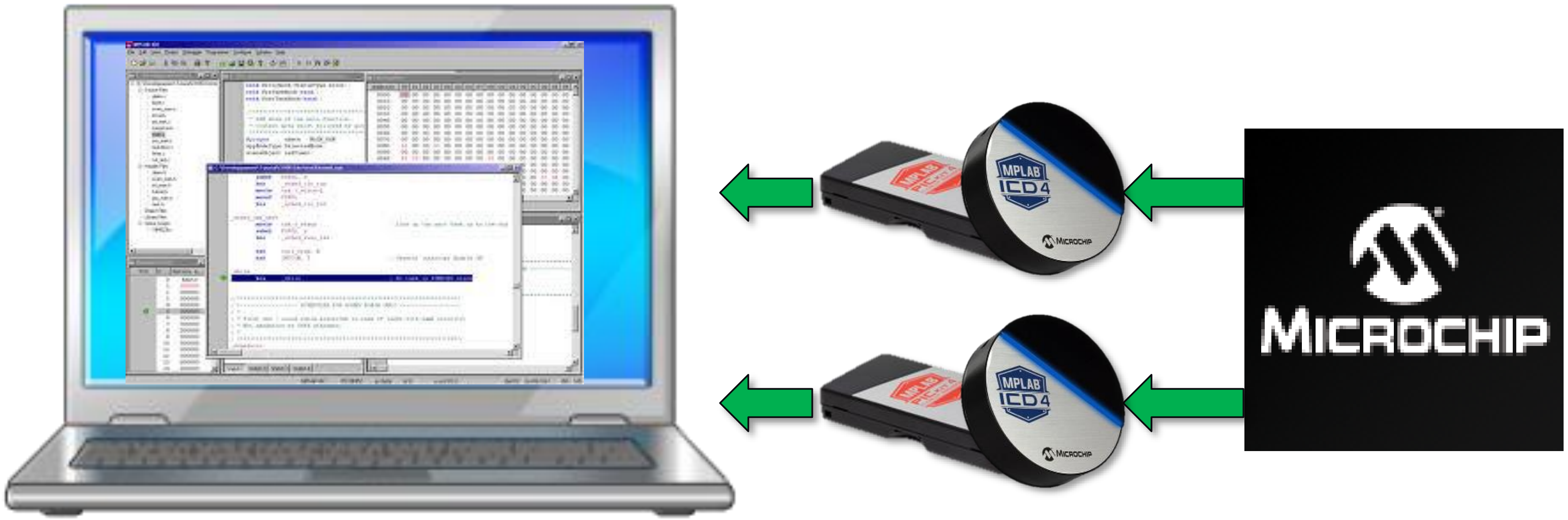
dsPIC33CH Family

Pin Ownership Mux



dsPIC33CH Family

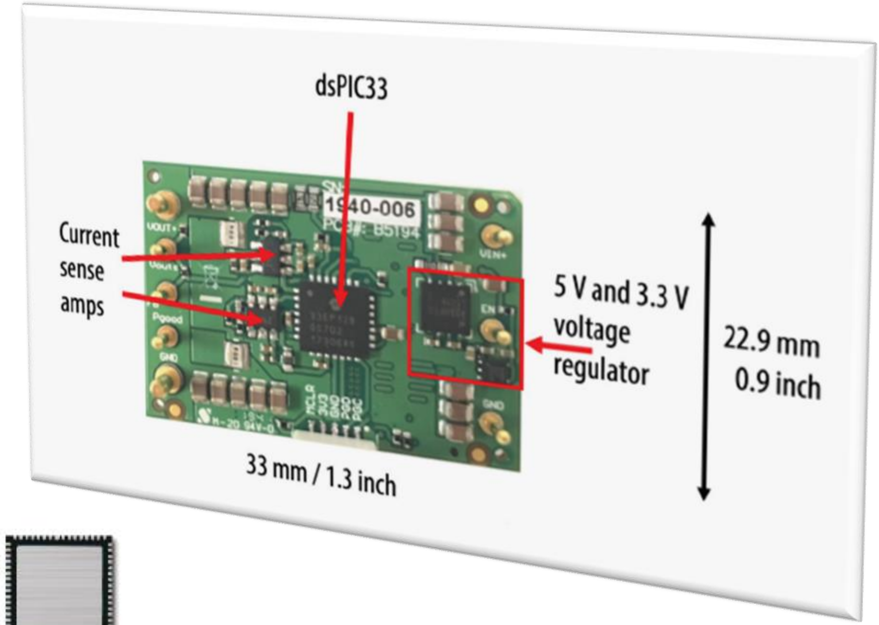
Dual Core Debug



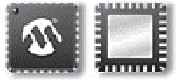
- **MPLAB® supports parallel debug sessions**
- **Main core programs secondary core, hosts image**
- **Debug is independent**
- **Changes to secondary core code are placed back into main core's image**
- **Breakpoints on either core can be configured to halt the other core or leave it running**

dsPIC33CK Family Packages

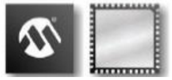
Wide range of packages from 28 to 80-pin



Package Types

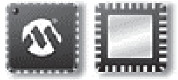


28-lead uQFN (2N)
6 x 6 x 0.5 mm
with corner anchors
(Lead Pitch: 0.65 mm)

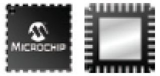


48-lead uQFN (M4)
6 x 6 x 0.5 mm
with corner anchors
(Lead Pitch: 0.4 mm)

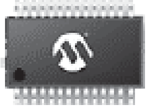
64-lead QFN (MR)
9 x 9 x 0.5 mm
(Lead Pitch: 0.5 mm)



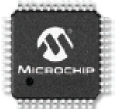
28-lead uQFN (M6)
4 x 4 x 0.6 mm
with corner anchors
(Lead Pitch: 0.65 mm)



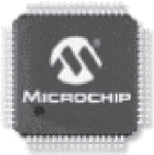
36-lead uQFN (M5)
5 x 5 x 0.5 mm
with corner anchors
(Lead Pitch: 0.4 mm)



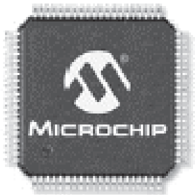
28-lead SSOP (SS)
10.2 x 5.3 x 2 mm
(Lead Pitch: 0.65 mm)



48-lead TQFP (PT)
7 x 7 x 1 mm
(Lead Pitch: 0.5 mm)



64-lead TQFP (PT)
10 x 10 x 1 mm
(Lead Pitch: 0.5 mm)

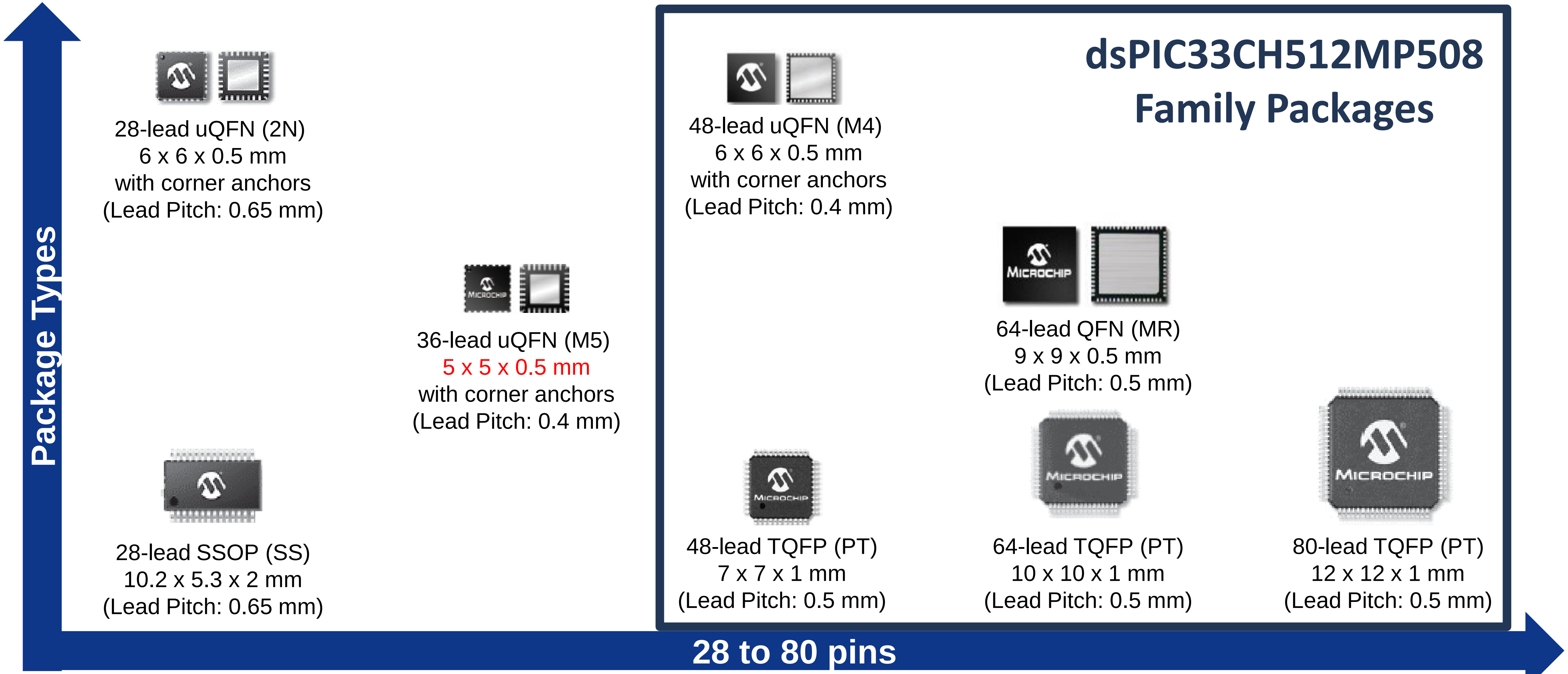


80-lead TQFP (PT)
12 x 12 x 1 mm
(Lead Pitch: 0.5 mm)

28 to 80 pins

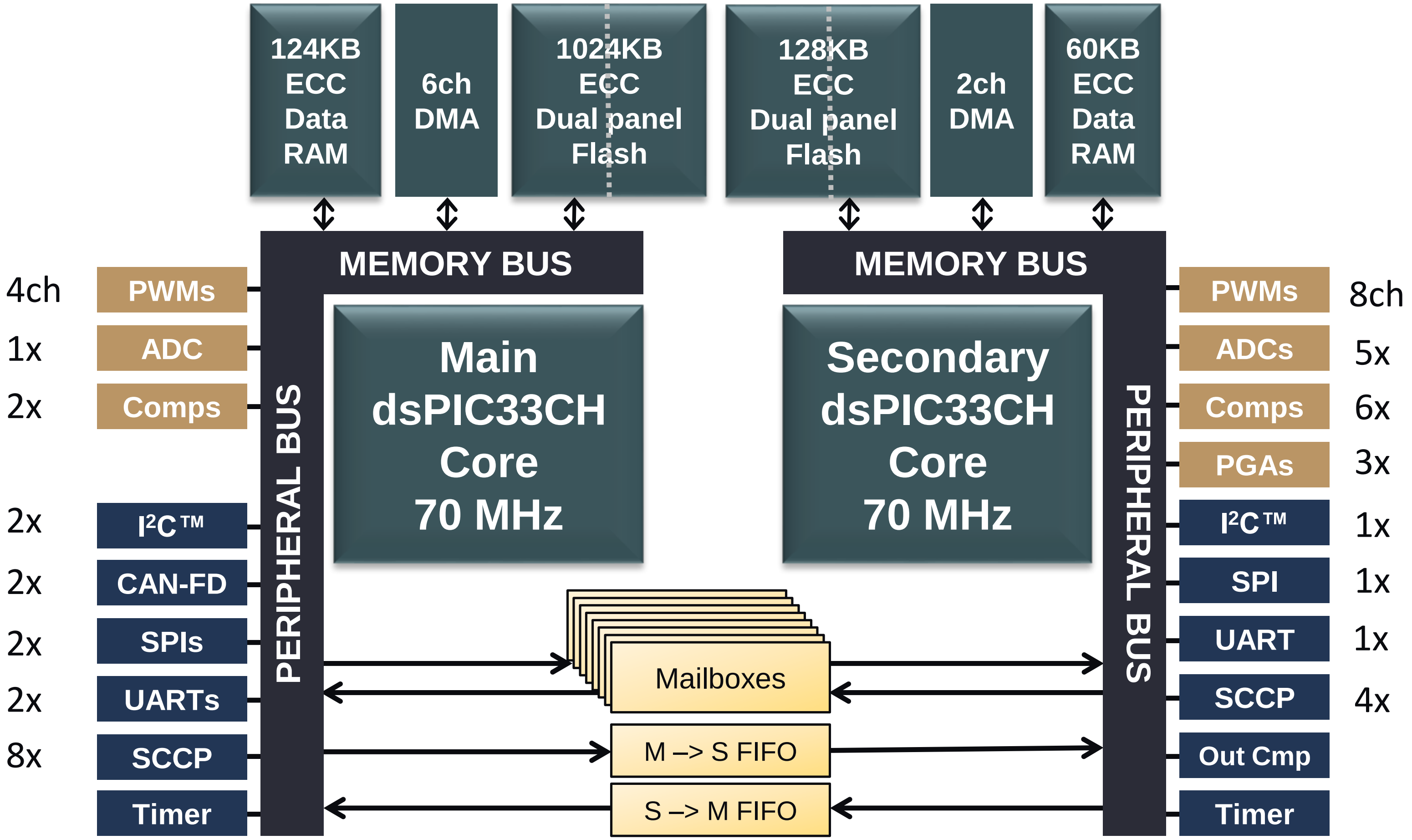
dsPIC33CH Family Packages

Wide range of packages from 28 to 80-pin



dsPIC33CH1024 Family

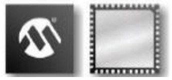
Preview – 6 ADCs, 8 Analog Comparators, 12 PWM Pairs, 3 PGAs



dsPIC33CH1024 Family

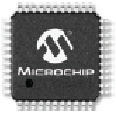
Packages

Package Types

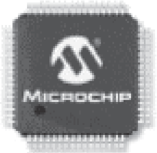


48-lead uQFN (M4)
6 x 6 x 0.5 mm
with corner anchors
(Lead Pitch: 0.4 mm)

64-lead QFN (MR)
9 x 9 x 0.5 mm
(Lead Pitch: 0.5 mm)



48-lead TQFP (PT)
7 x 7 x 1 mm
(Lead Pitch: 0.5 mm)



64-lead TQFP (PT)
10 x 10 x 1 mm
(Lead Pitch: 0.5 mm)

80-lead TQFP (PT)
12 x 12 x 1 mm
(Lead Pitch: 0.5 mm)

100-lead TQFP (PT)
12 x 12 x 1 mm
(Lead Pitch: 0.4 mm)

128-lead TQFP (PT)
14 x 14 x 1 mm
(Lead Pitch: 0.4 mm)

48 to 128 pins

Royalty-Free* Reference Designs

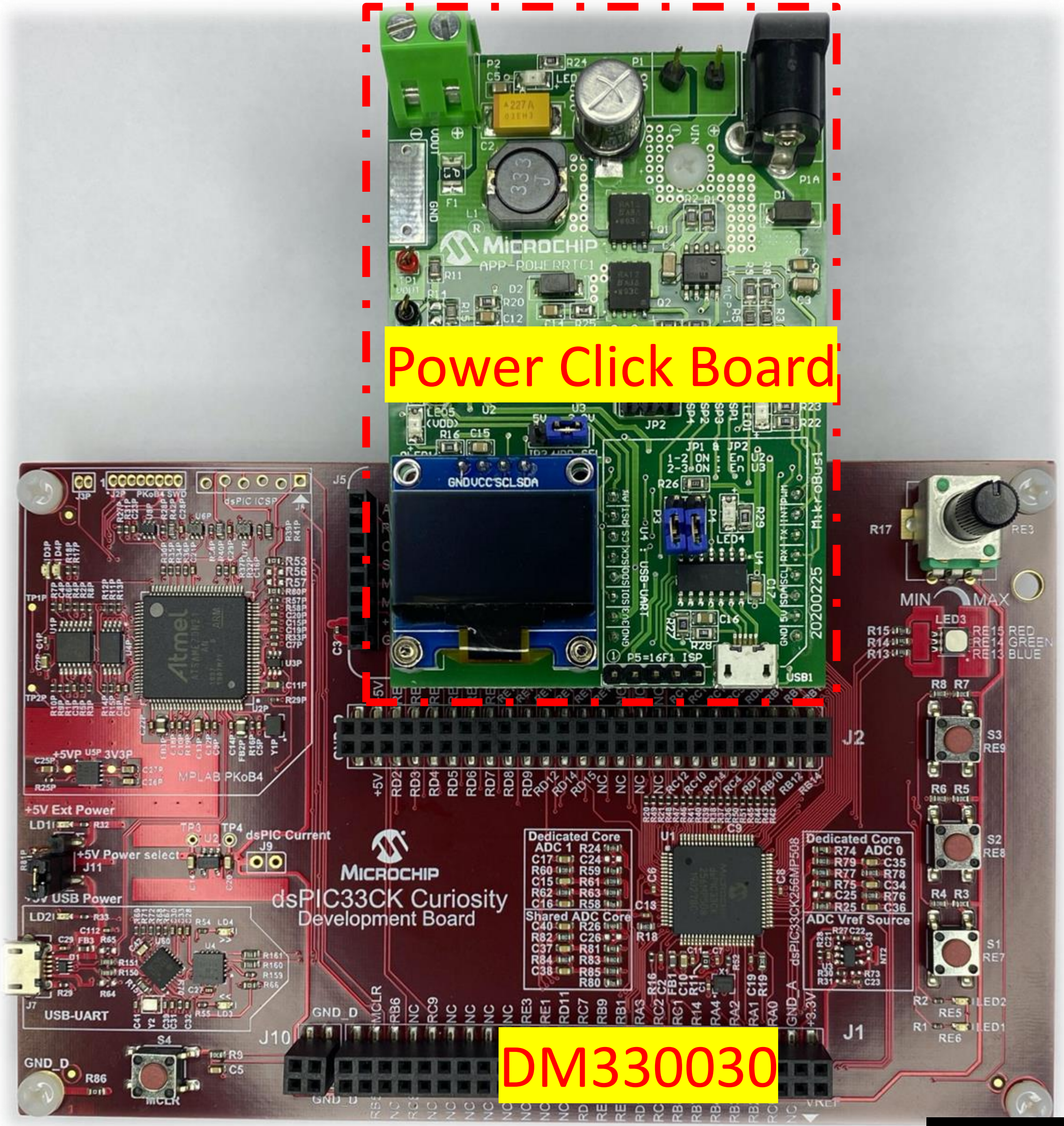
Available Today

- 750W AC/DC Supply
  - *Semi-Bridgeless PFC*
  - *Zero Voltage Switching Full-Bridge with Peak Current Mode Control using Digital Slope Compensation and Synchronous Rectification*
- 720W Platinum-rated AC/DC Supply
  - *IPFC + interleaved 2-switch forward conv with SR*
  - *Adaptive algorithms to achieve > 94% efficiency*
- Enhanced Solar Micro Inverter
  - *250W panel input, grid-tied output*
  - *MPPT to achieve 94.5% efficiency (peak)*
- 1KW Pure Sine Wave UPS
  - *Offline UPS system*
  - *Push-pull converter & full-bridge inverter*
- Interleaved Power Factor Correction
  - *Two phase interleaved PFC*
  - *Up to 400VDC output, 350W sustained*
- DC/DC LLC Resonant Converter
  - *Zero Voltage Switching on half-bridge conv*
  - *Zero Current Switching on synch rectifier. >95% eff*
- Quarter Brick DC/DC Converter
  - *Phase-shifted full-bridge topology*
  - *Planar magnetics and non-linear control for efficiency*

*Royalty-free when used in accordance with Microchip's licensing agreement

SR Buck Power Click Board for Hand-ON

- SR Buck Power Click Board Spec：
  - Vin = 8~12V
  - Vout = 5V
  - Iout = 1A
  - L = 33µH
  - C = 220µF ESR = 120 mΩ
  - f_{SW} = 250 kHz (Deadtime=150ns)
  - fx = 10 kHz
  - P.M. = 60°
- Control loop design:
  - PWM Gain = 21.58dB @12Vin
  - f_0 = 833Hz
  - Double Zero for f_R = 1.868kHz
  - One pole for f_{ESR} = 6.029kHz
  - One pole at $f_{SW}/2$ = 125kHz



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MPLAB® Starter Kit for Digital Power -3

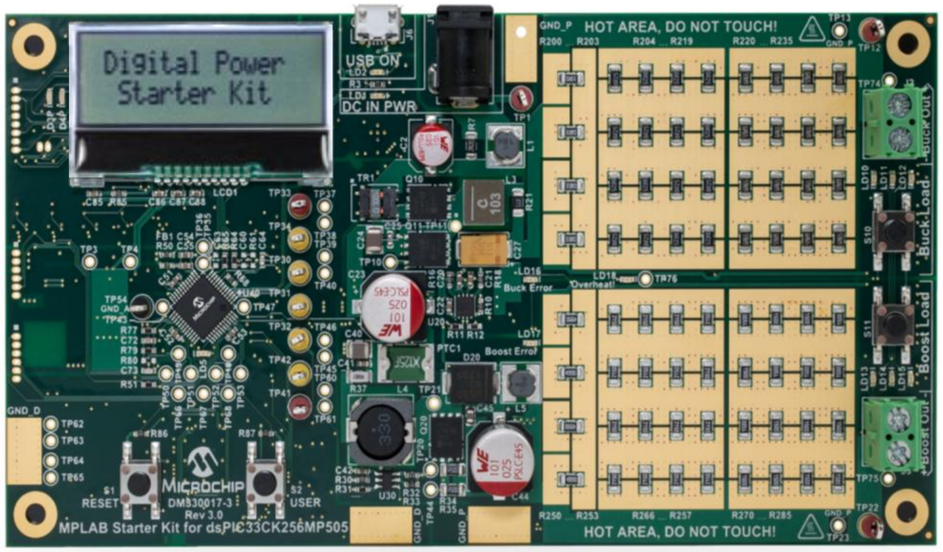
Features:

- dsPIC33CK256MP based
- Independent buck and boost DC/DC converters
- LCD display, status LEDs, temperature sensors
- Configurable resistive loads
- PKOB-4 On-board debugging / programming via USB

Package Contents:

- Board (~ 5” x 2.5”)
- Mini USB cable
- 9V Power Supply
- Info Sheet with schematic

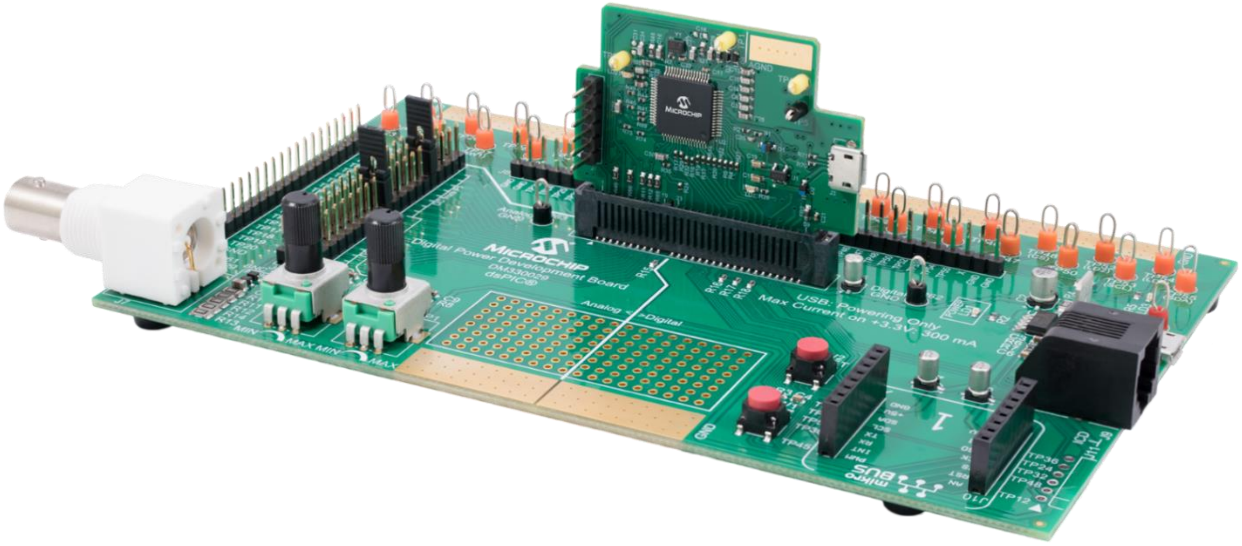
$199.99



Order # DM330017-3

Digital Power Development Board

- Uses new Digital Power PIMs
- Micro Elektronika mikro BUS Socket
- PWM & GPIO Test pins
- Analog Input test pins
- BNC Connector
- Analog potentiometers
- Push button
- Solder pad- Scope ground connection
- Prototyping field (2.54mm raster)



Part Number: DM330029 $112

New Digital Power PIMs

- **Building blocks for Microchip's digital power development boards**
  - Controller easily swapped out for evaluation of various dsPIC33 family members

- **Flexibility for prototyping with PCBs that use this standardized DP PIM connector**

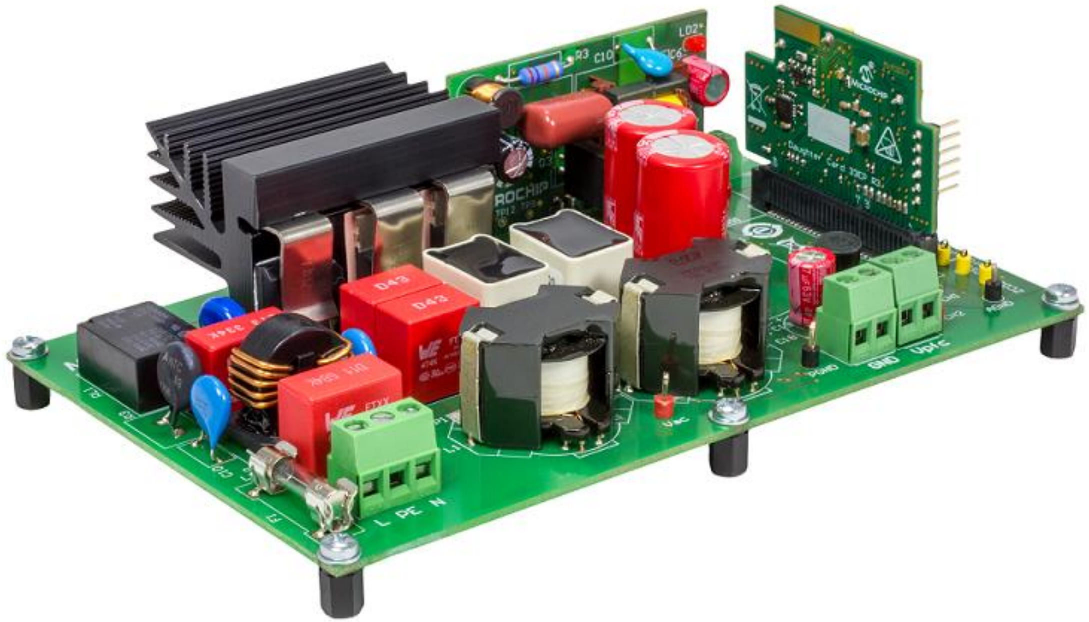
- **Features**
  - ICSP™ programming header
  - On-board LDO with Power Good (PG) function
  - Micro USB connector
  - MCP2221A USB to UART/I2C serial converter
  - Edge connection for analog inputs/outputs, PWM outputs and GPIO ports
  - Test point loop for DAC output

Available today @ $49 each

Available DP PIMs	Part Number
dsPIC33EP128GS808	MA330043
dsPIC33CK256MP508	MA330048
dsPIC33CH512MP508	MA330049

LV PFC Development Board

- **Low Voltage PFC**
  - Vin: 12 - 24V AC
  - Vout: 31 - 42V DC
  - ~50W Max
- **Topology**
  - Single phase or
    Interleaved dual phase
  - Firmware for:
    - Continuous Conduction Mode
    - Critical Conduction Mode (a.k.a. Transition Mode or Boundary Mode)
- **Uses DP PIM controller modules**
- **Companion DC/DC Interleaved LLC Development Board In Development**
- **Part # DV330101 $375**



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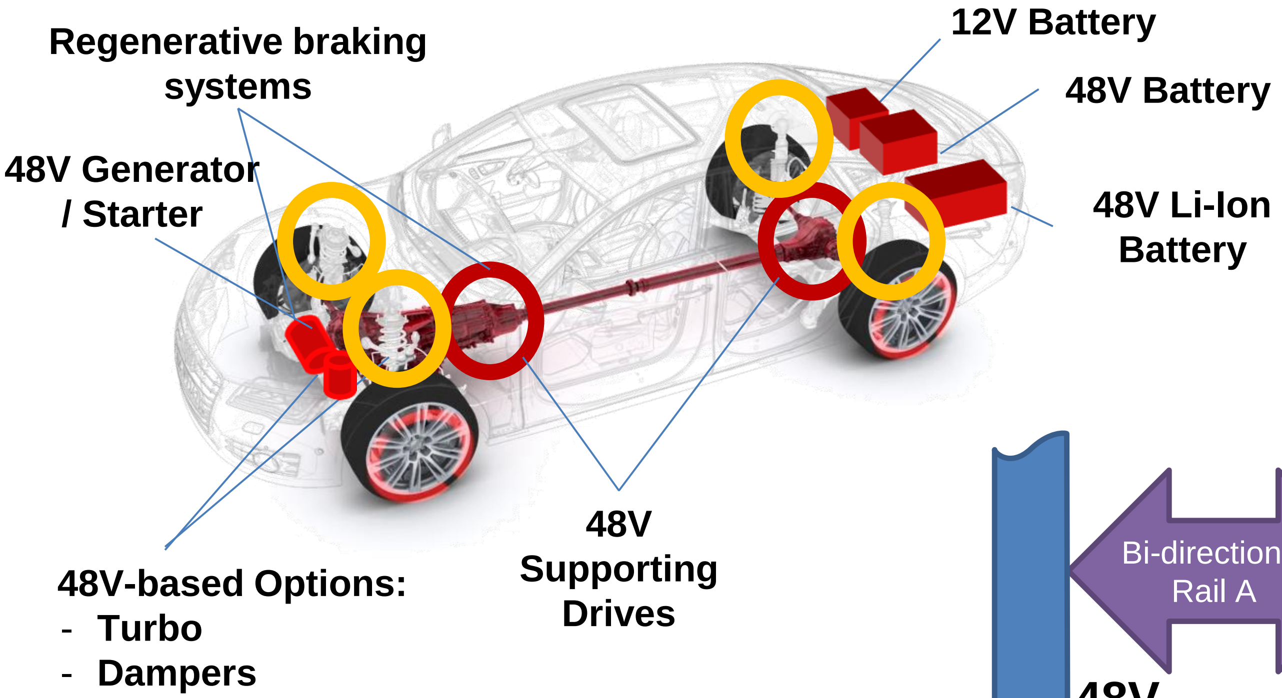
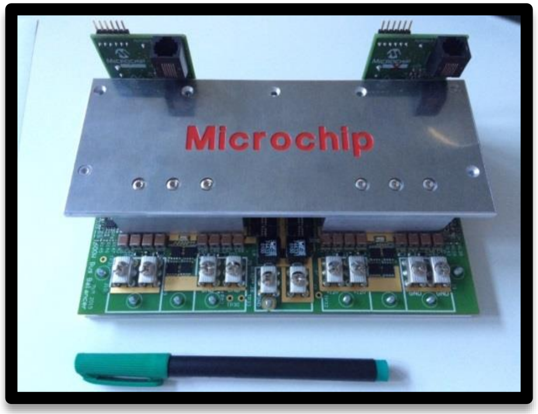
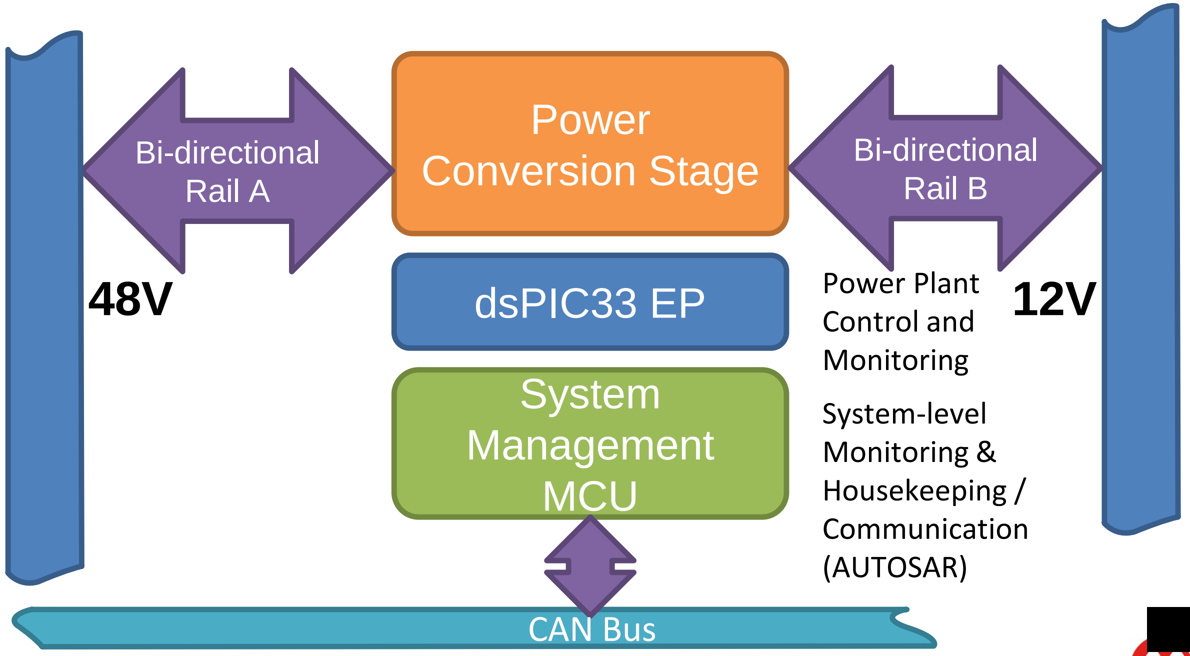
MICROCHIP

Automotive Bidirectional DC/DC Bus Converter







Vienna PFC Reference Design

The primary stage of a High-speed EV Charger

- **30 kW Vienna rectifier topology**
- **98.5 % peak efficiency**
- **3-phase 380/400 VAC, 50 Hz/60 Hz input voltage**
- **<5 % current THD at half and full loads**
- **Microchip 700 V, 15 mOhm SiC MOSFETs mounted on AVVID MaxClip heat sinks to reduce communication loop inductance and voltage spikes across devices**
- **PCB design according to IEC standards, with consideration for safety, current stress, mechanical stress, and noise immunity**
- **dsPIC33CH controller with verified open-source software using 3-level modulation for digital control**

Matching 30kW LLC charger in development

Transphorm’s 4 kW Bridgeless Totem-Pole PFC

dsPIC33CK and Transphorm’s SuperGaN™

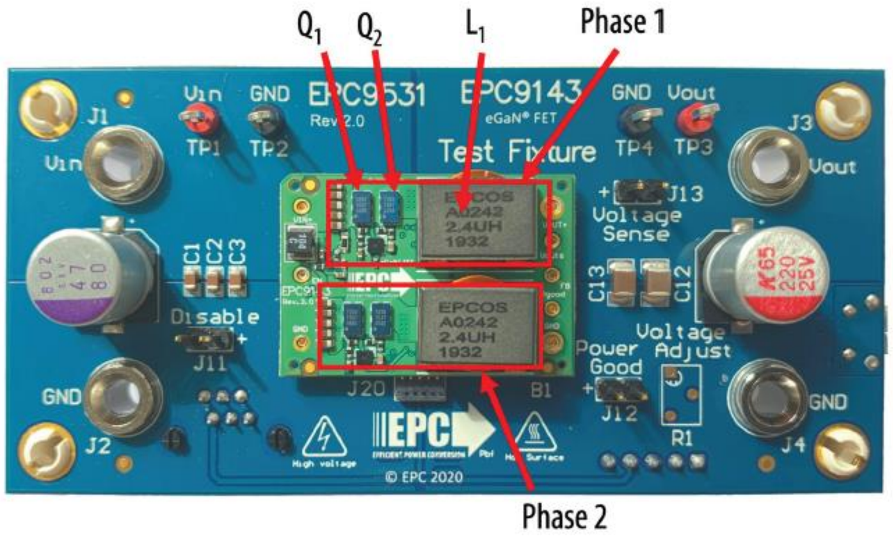
- **> 99% peak efficiency**
- **< 2% THDv with < 3% THDi noise distortion**
- **> 0.99 PF**
- **Zero Load / High Load startup ability**

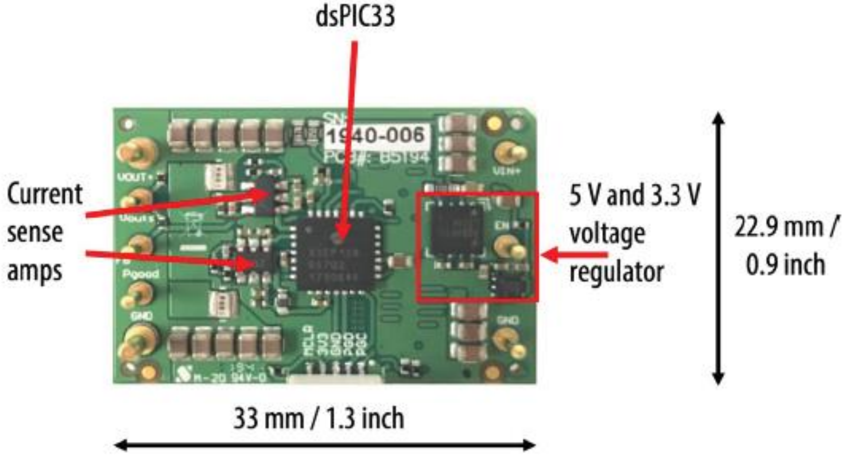
Test Setup and Conditions	
Evaluation Kit	TDTTP4000W066C-KIT
Operating frequency	66 kHz
Input voltage	85 Vac to 265 Vac
Output voltage	385 Vdc ±5%
Digital power PIM	dsPIC33CK256MP506
GaN device	TP65H035G4WS
Gate resistor	30 Ω
Gate ferrite bead	200 Ω @ 100MHz

EPC's 300W 1/16th Brick IBC Converter

Reference Design Features

- **Microchip dsPIC33CK digital signal controller**
- **EPC GaN FETs with 3.2 mΩ RDS(on)**
- **Two-phase synchronous buck topology**
- **48 V in -> 12 V out**
- **Power density: 730 W/in³**
- **Output power: 300 W**
- **Peak efficiency: 95.8%**
- **Size: 1.3 x 0.9 x 0.4"**





Summary

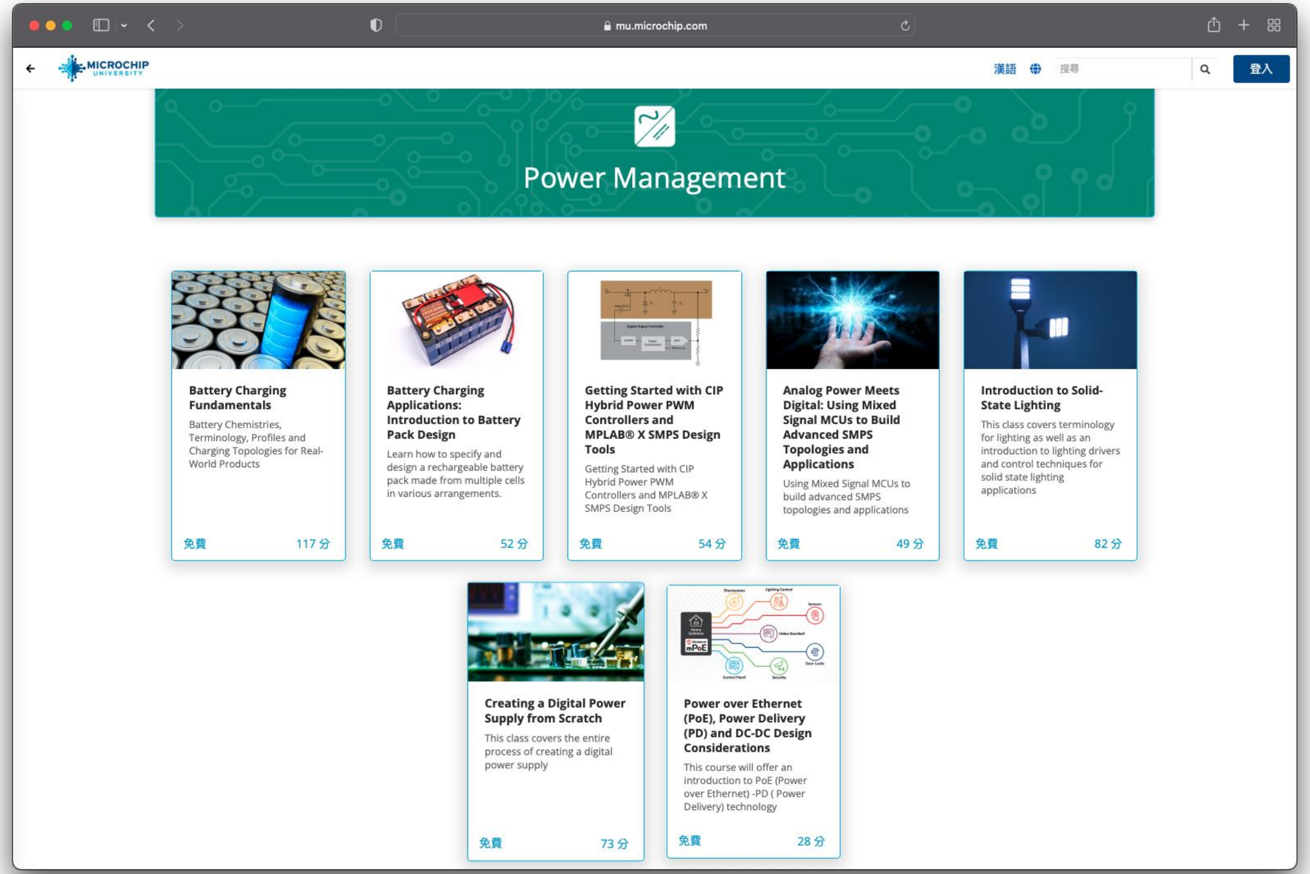
- **Power Factor Correction reduces energy losses and overall costs and is required on most switch mode power supplies**

- **Implementing active PFC especially digital PFC, is quite complex but can achieve high PF, low iTHD, and work with universal mains.**

- **The dsPIC© DSC enables advanced PFC techniques for improved system performance**

Training Courses For Power Management

- **Microchip University – Power Management**
  - https://mu.microchip.com/page/power-management



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The Book For Reference ☺

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MICROCHIP

May The *Power* Be With You