The challenges of SI Models

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About Samtec

Cable assembles

High Precision RF connectors

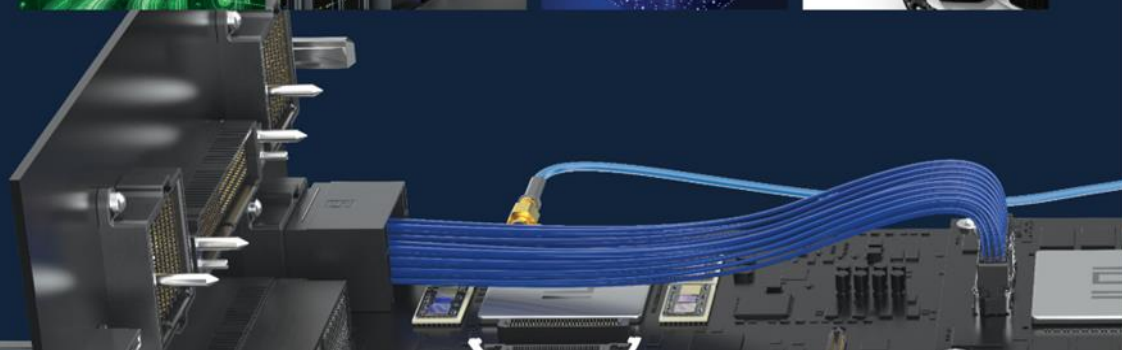
High-Speed, High-Density Backplanes & Arrays

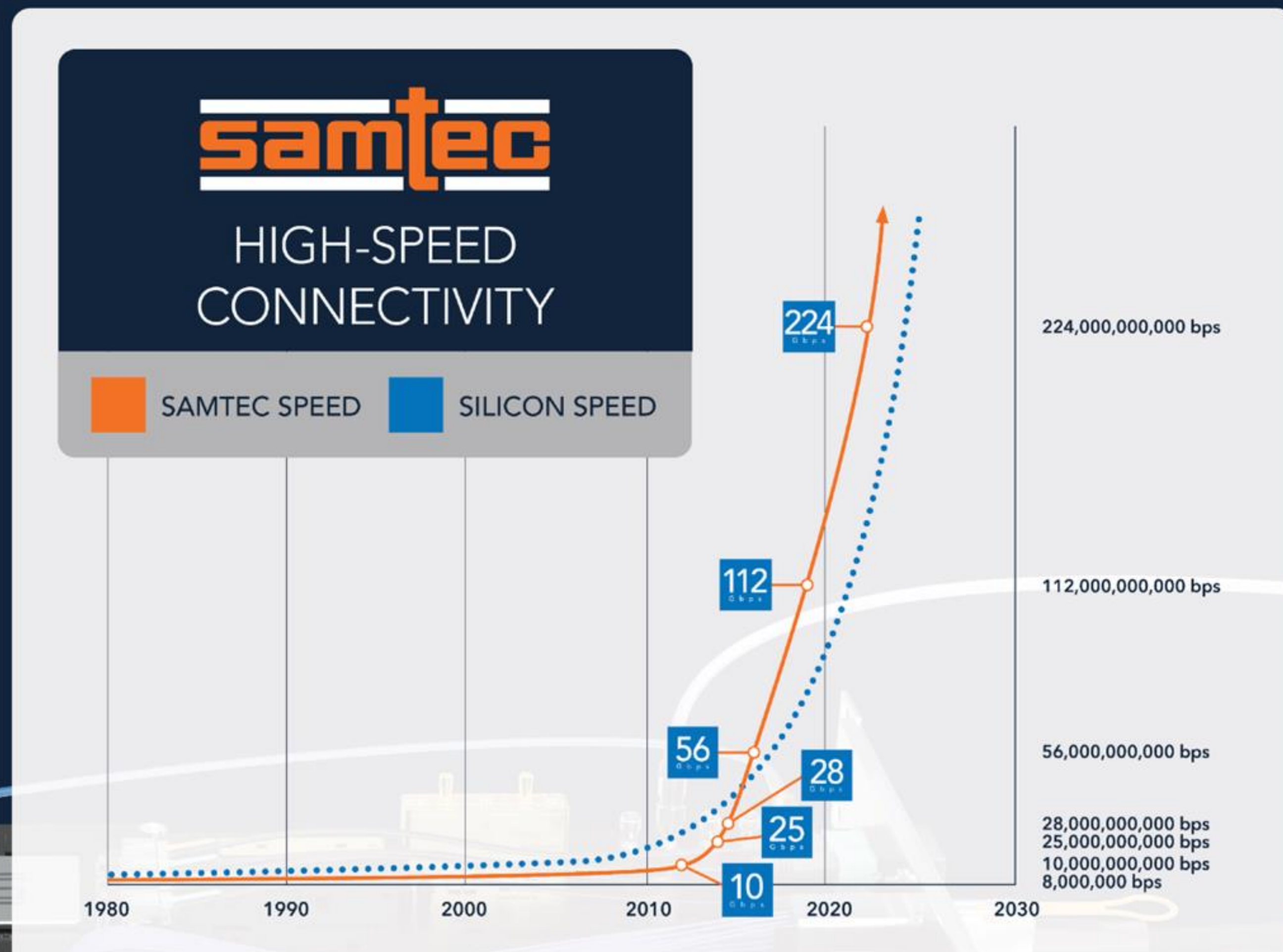
Both inside and outside the box

The industrial

THE
TECHNICAL
RENAISSANCE IS…

…driven by ***progress***, challenged with unprecedented performance ***demands***, a catalyst for next level technologies and ***innovation***…





Research & Development

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Challenges

Developing time

Pressure of time to market

Accuracy

Accurate performance evaluation

Complexity

SI,PI & Thermal

Cost

Cost of errors is high

Simulation could be the good answer

Simulations need models

The evolution

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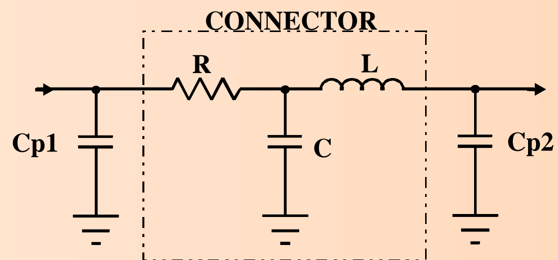
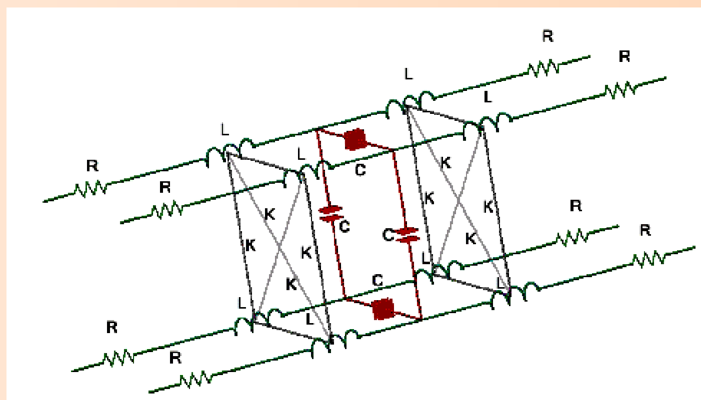
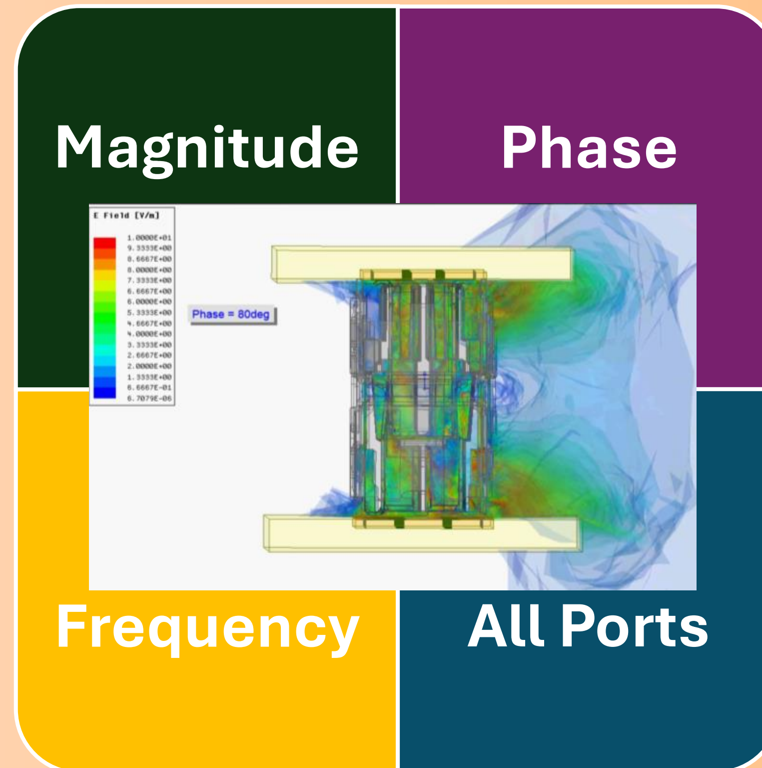




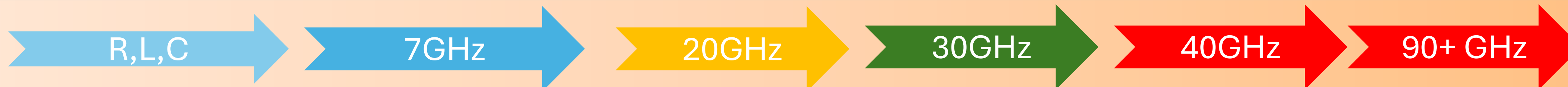
2D Solver

Spice Base

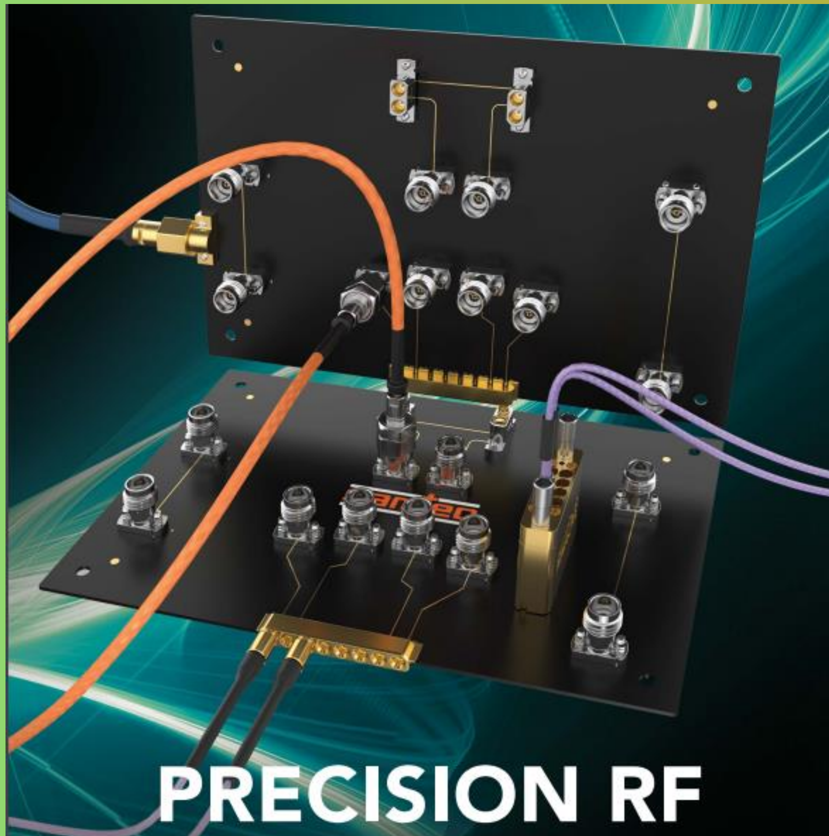


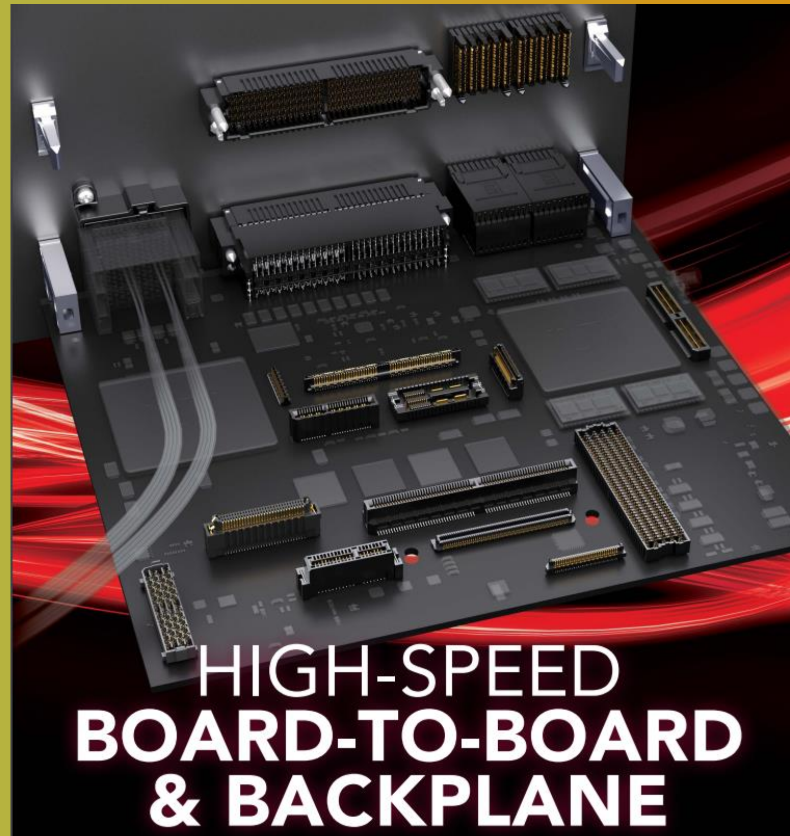
3D Solver

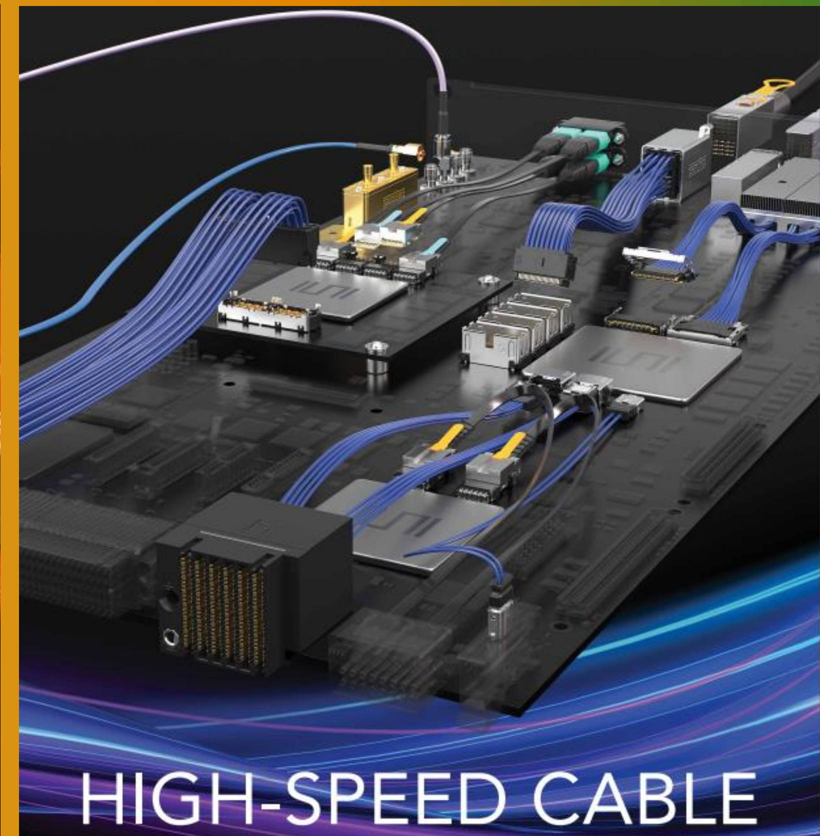
S-parameter



Model support







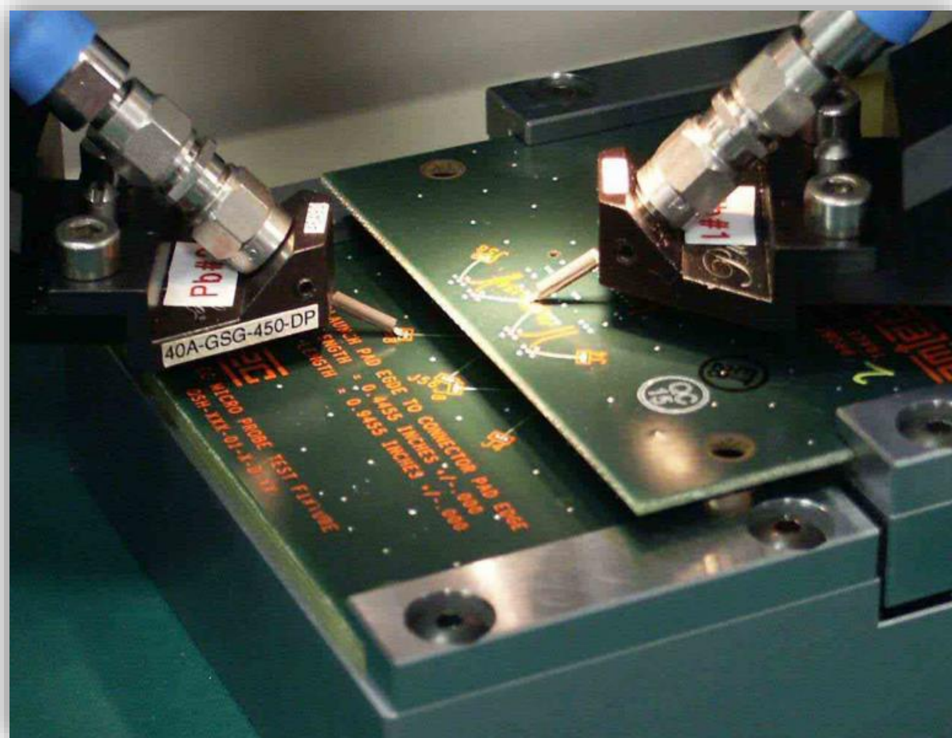
Correlation : Index of model accuracy

Measuring fixture

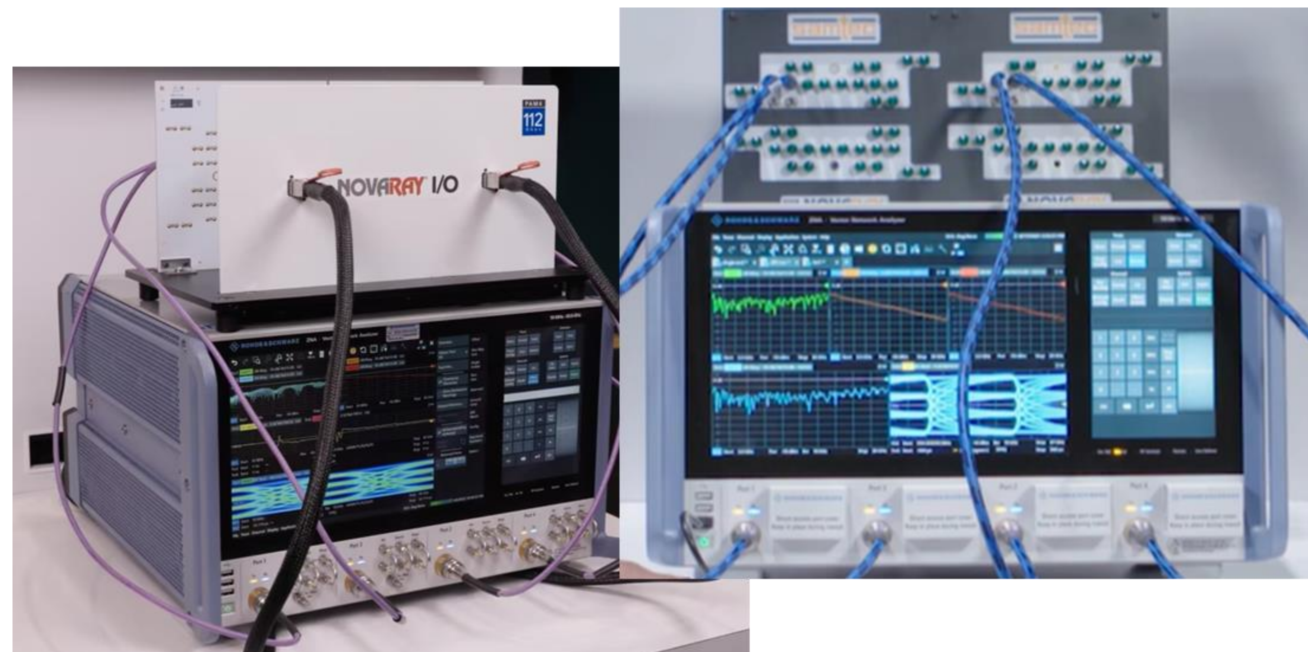
PCIE-G5

292-CM

Measuring system



Micro-probe



VNA/PNA

Factors

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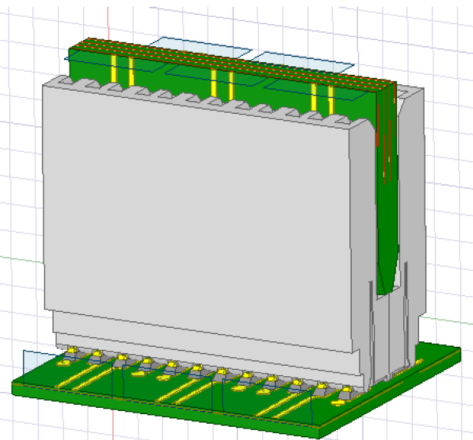
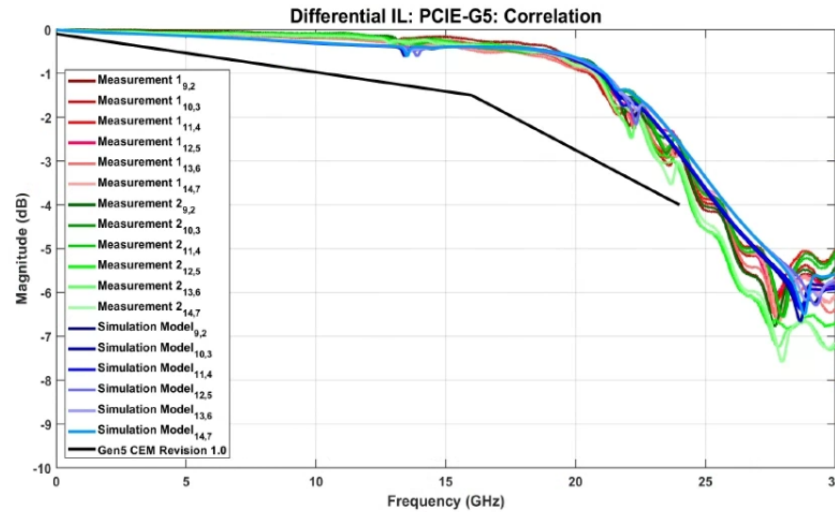
- **Material**
  None-conductive(connector body, insert/over molding, insulator…)
  Conductor(copper, brass…)
- **Contact deflection**
  Deflecting angle
- **Production tolerance**
  contact insertion, forming, sway
- **Processing**
  solder volume, part placement
- **Application**
  mating depth, compression force
- **De-embedded Process**
  De-embedding method, de-embedding bandwith
- **PCB design/tolerance**
  mis-registration, via structures

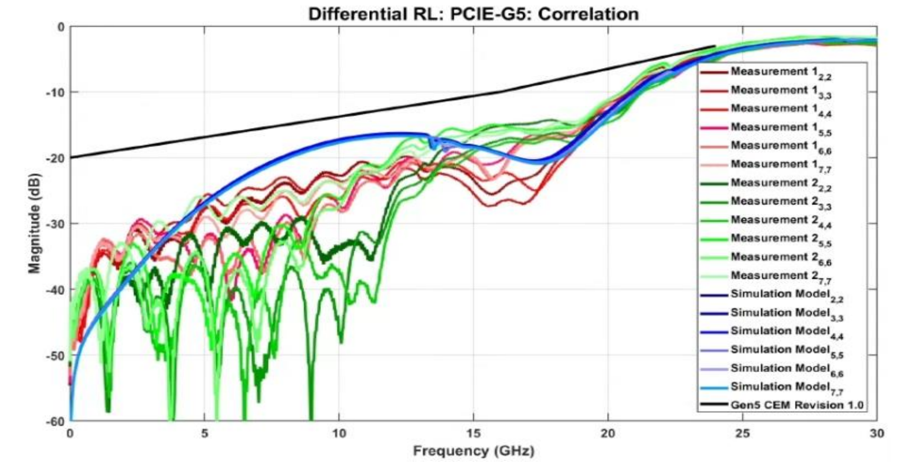
Correlation - PCIE-G5



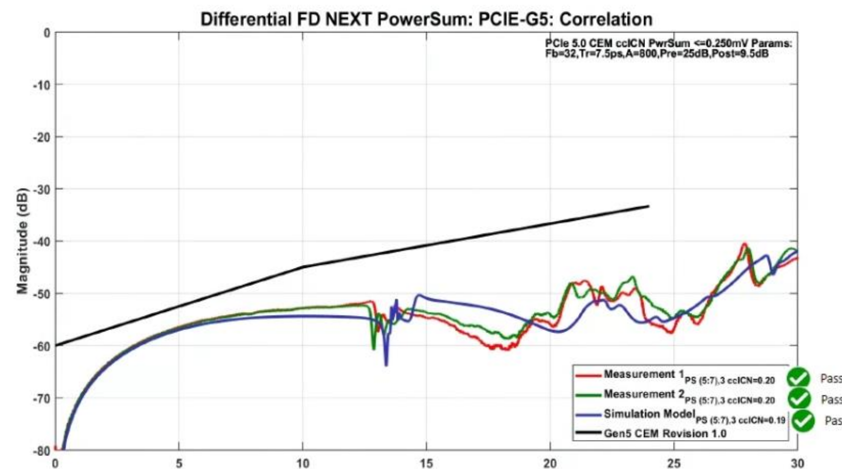
Differential Insertion Loss:



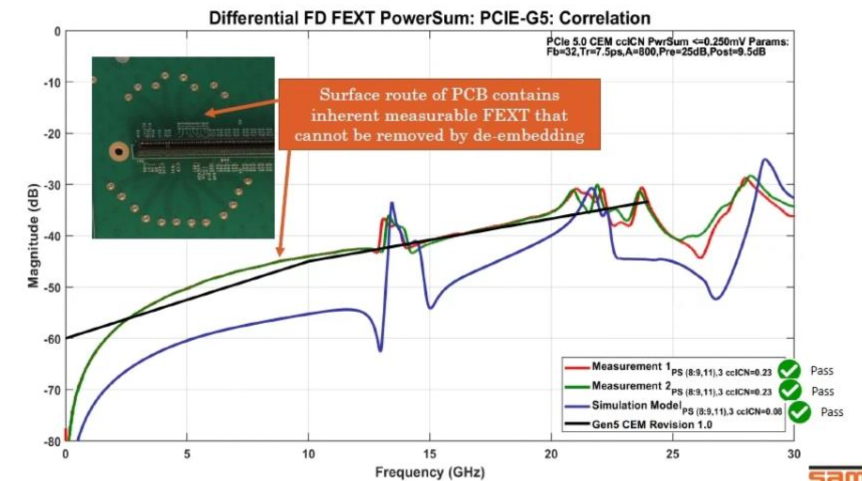
Differential Return Loss:



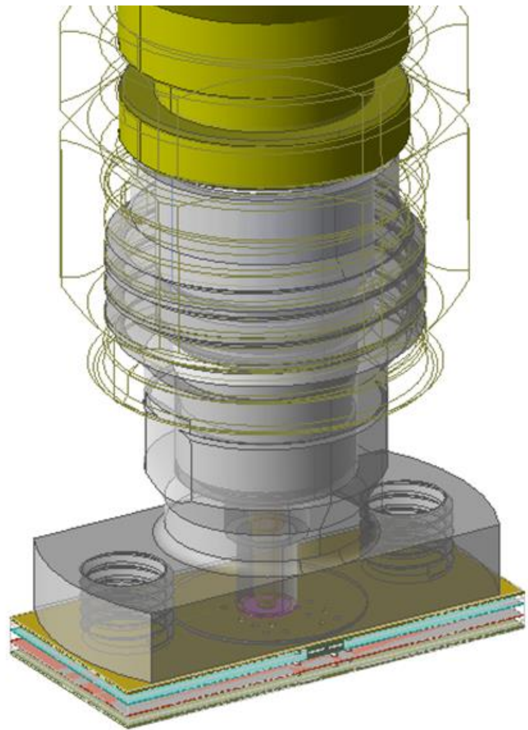
Differential FD NEXT: Power Sum

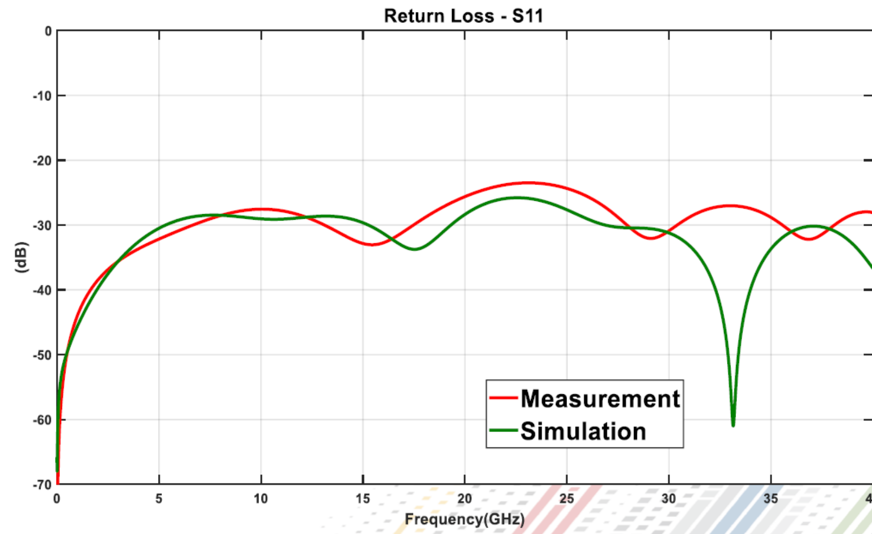


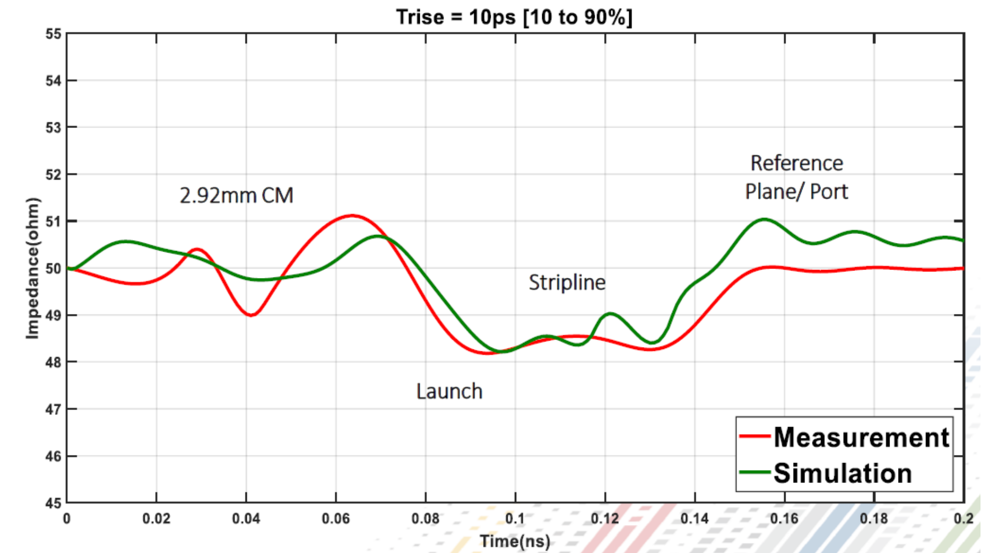
Differential FD FEXT: Power Sum

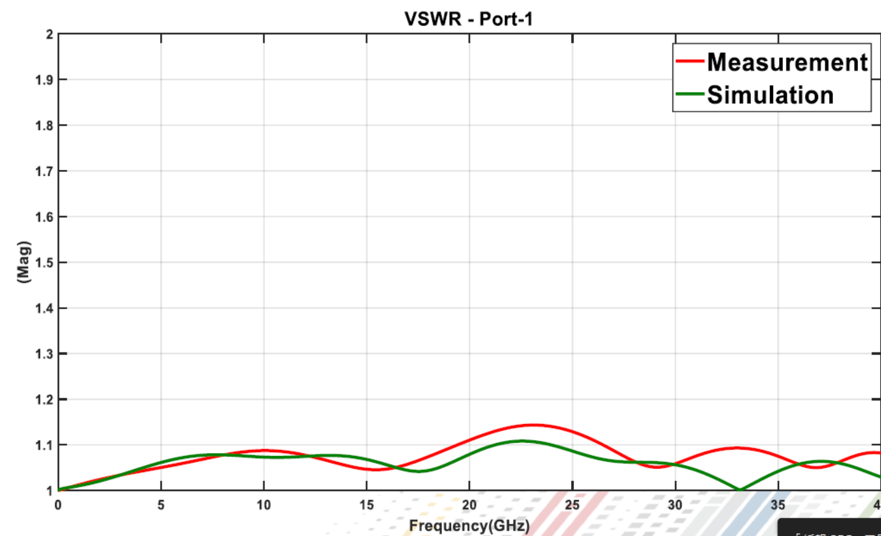


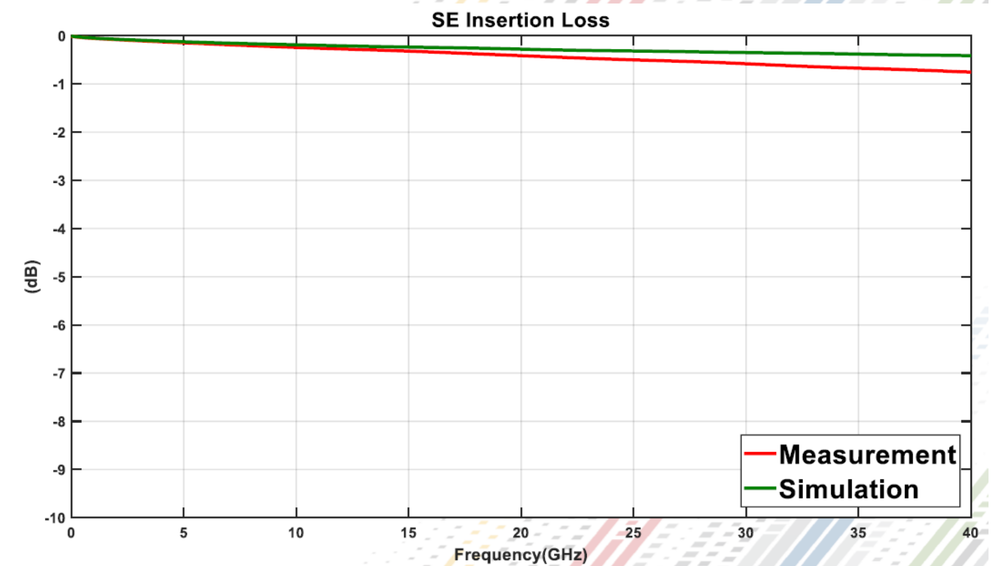
Correlation – 292-CM











Samtec models

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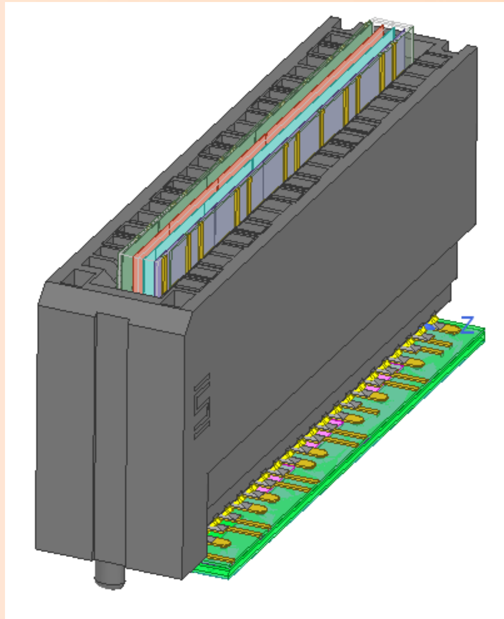
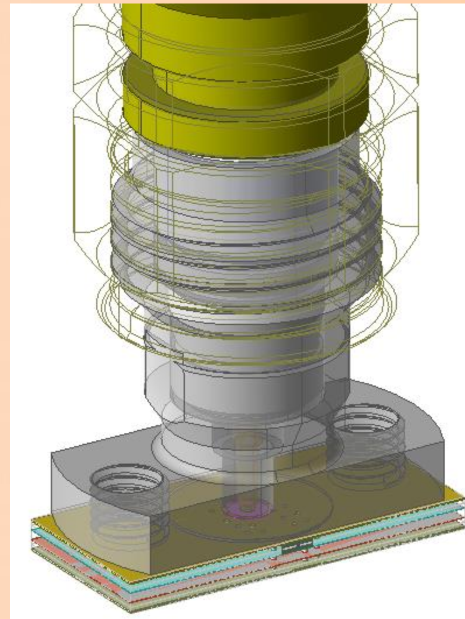
- **Model correlation is time consuming**
- **Model is not perfect, even the correlated model**
- **Most of models for high-speed products are correlated model**
- **None correlated model doesn’t mean a bad model**

Model Boundary

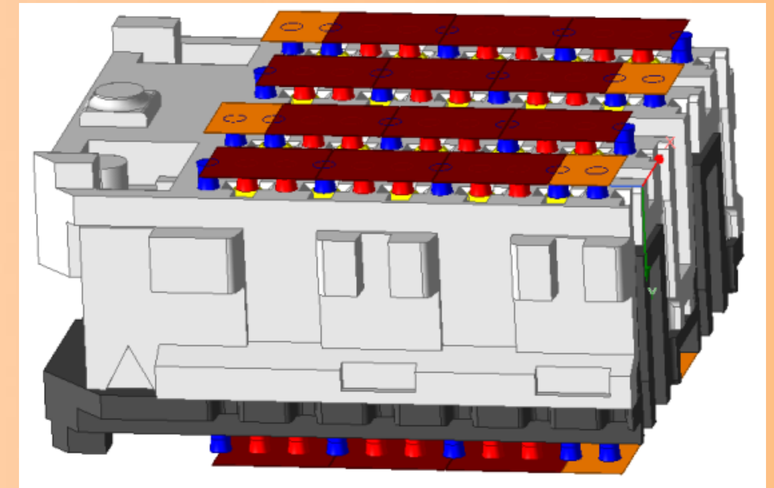
Two row SMT connector



RF connector



High Density BGA

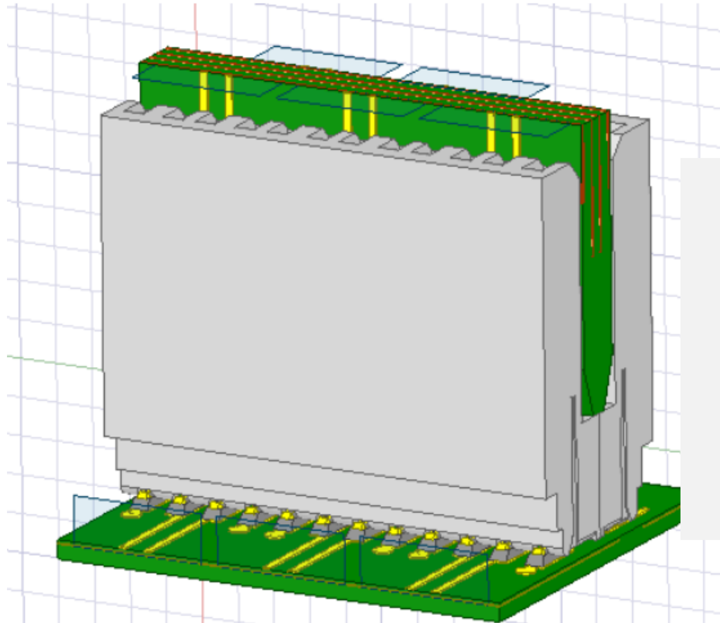


Connector + Predefined PCB

Connector + specific PCB

Connector Only

Two row SMT connector

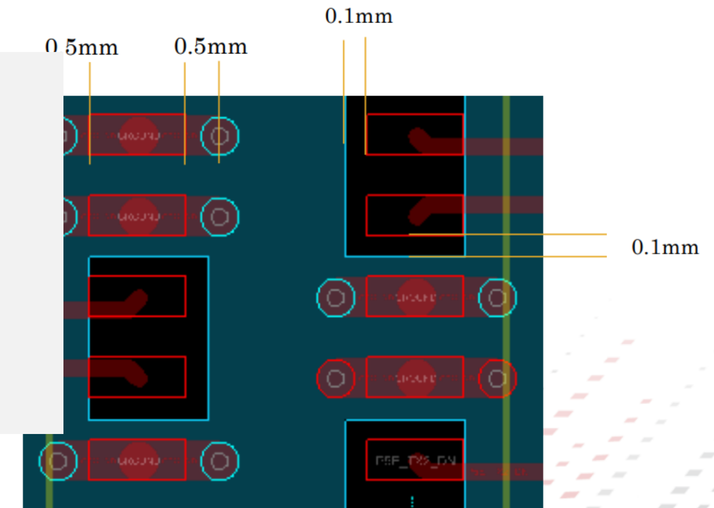


3D structures

Layer Number	LayerName	Material	Thickness mils	Thickness mm
	TOP_SM	PSR-4000-BN	0.71	0.018
6	BOTTOM	PLATED COPPER (0_5oz)	2.6	0.066
	BOTTOM_SM	PSR-4000-BN	0.71	0.018
Total thickness over solder mask and plated copper			63.95	1.624

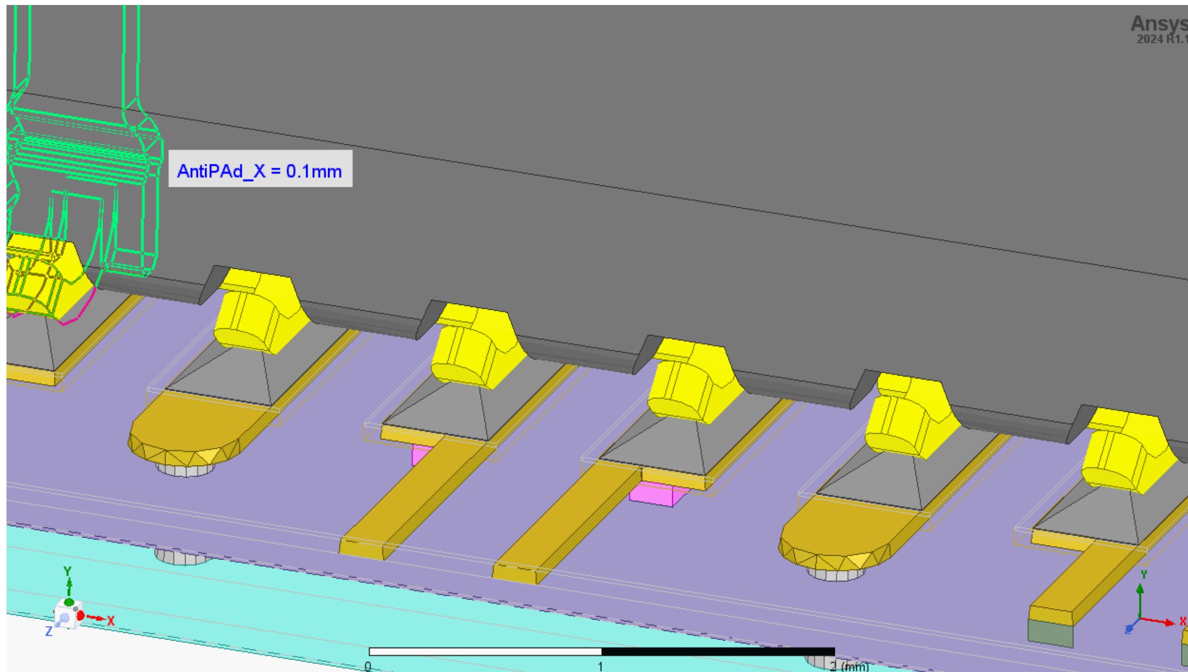
PCB stack-up

What if different PCB ?
What if different Anti-pad?
How accurate it is in my channel?

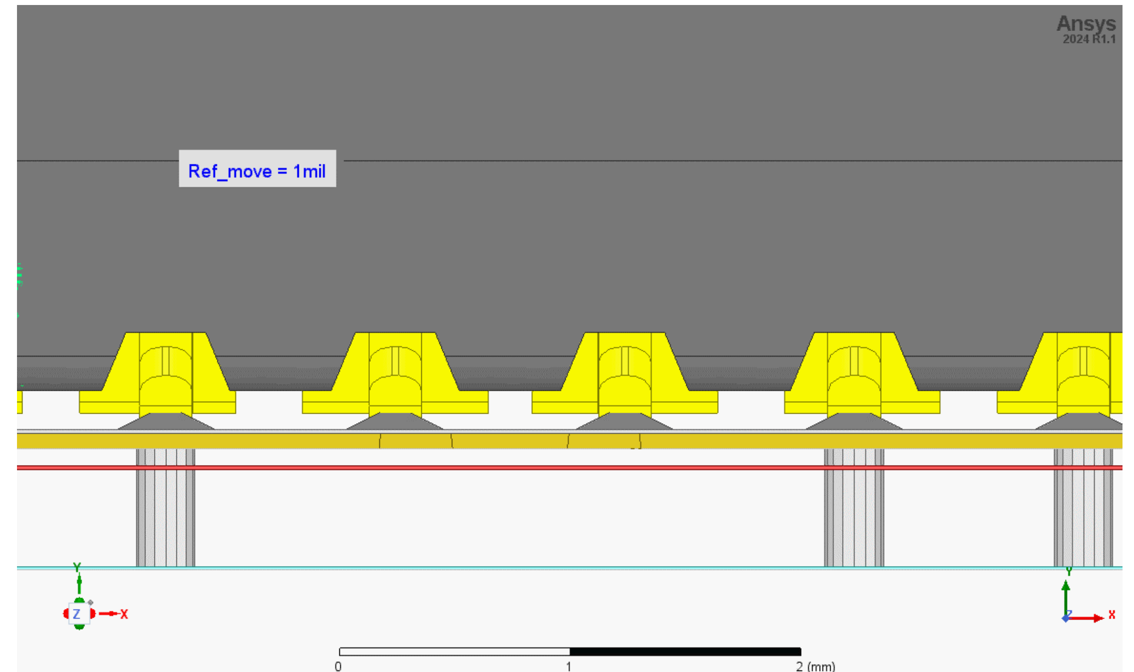


Reference Layout

Does it matter?



Sweep Anti-pad size



Sweep stack-up

Anti-Pad variations

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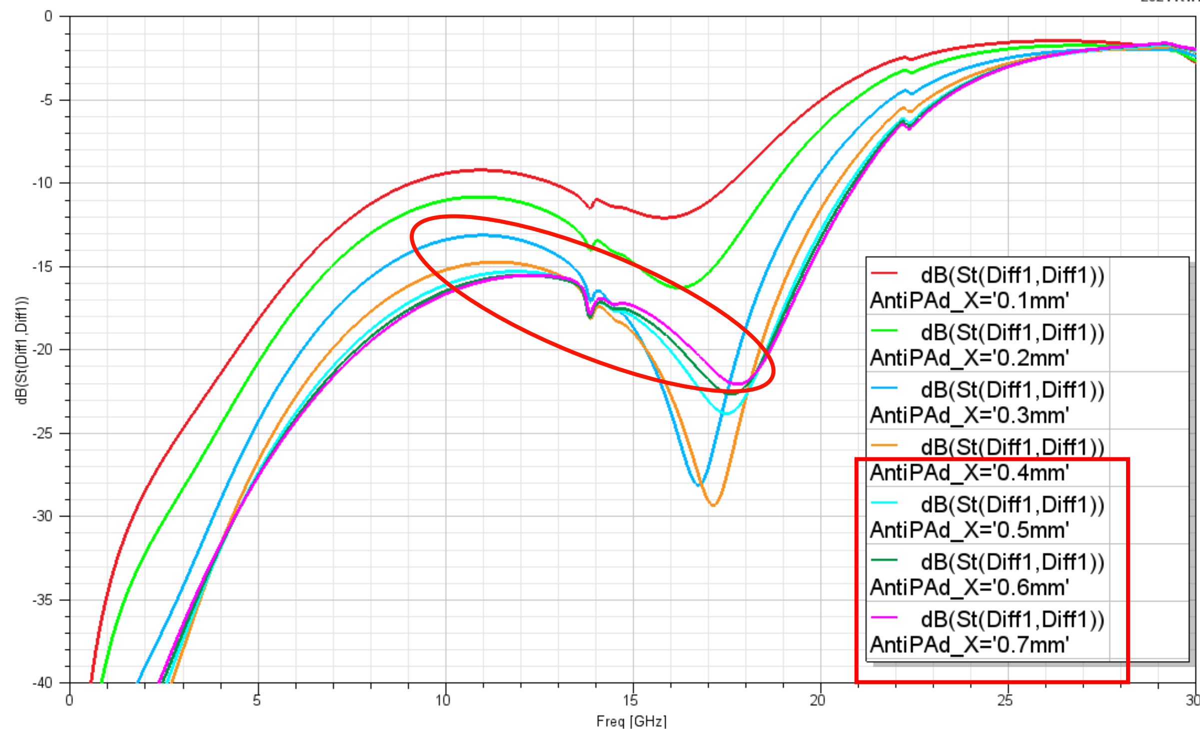
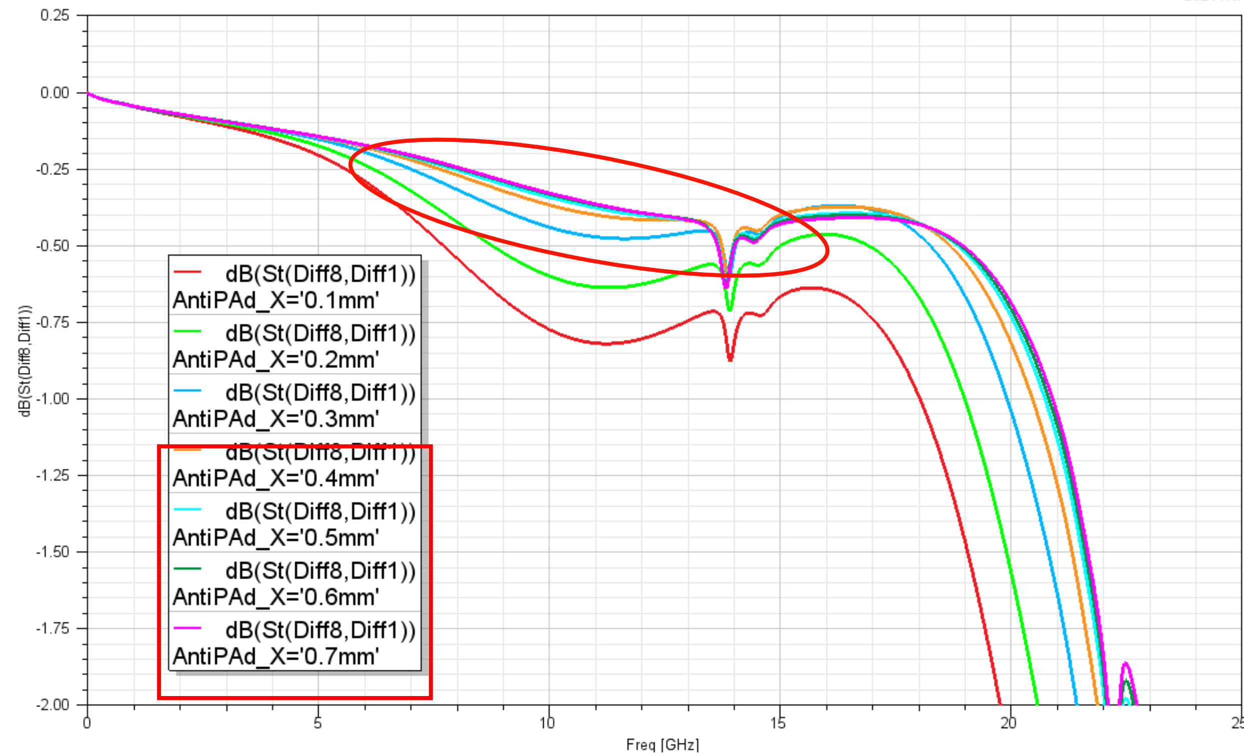
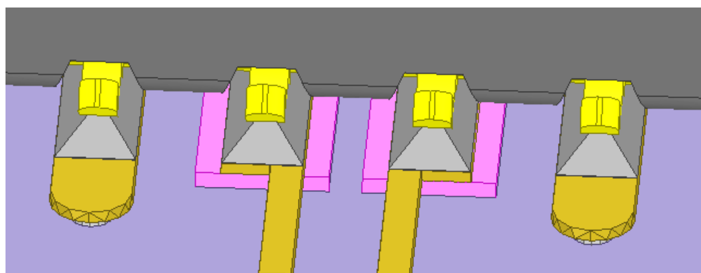
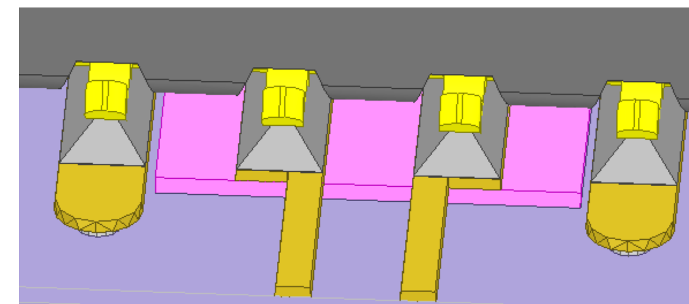
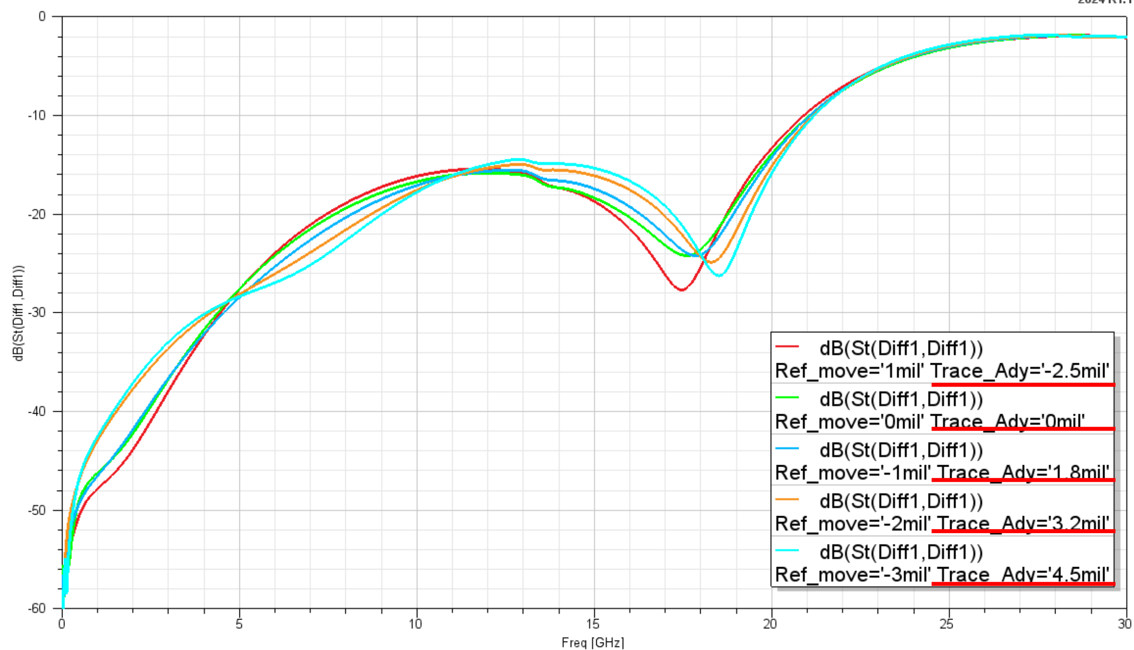


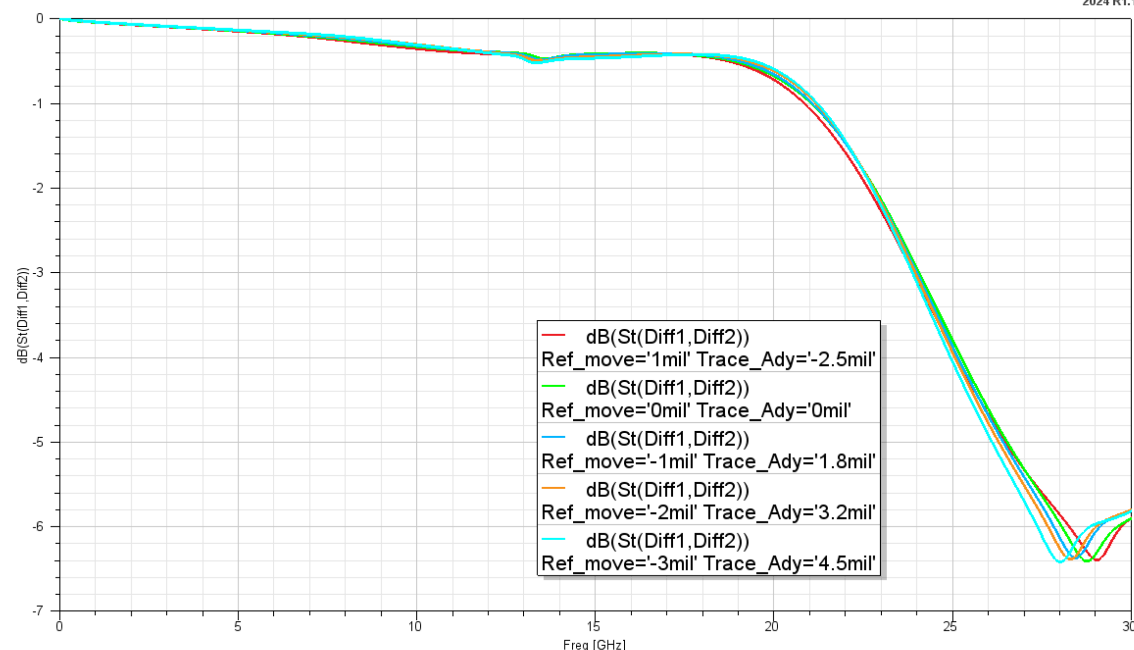


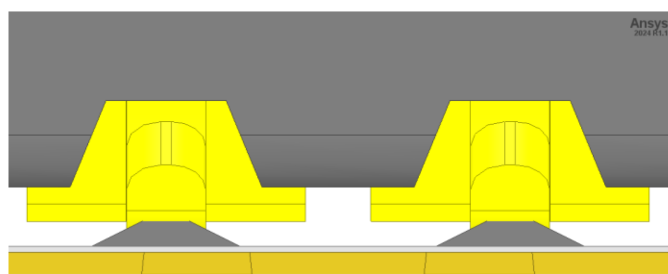




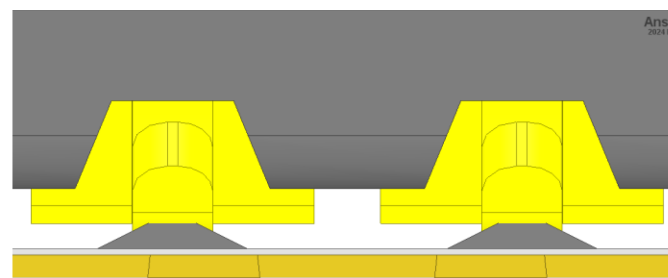
The stack-up

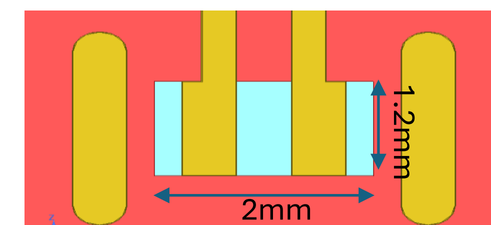




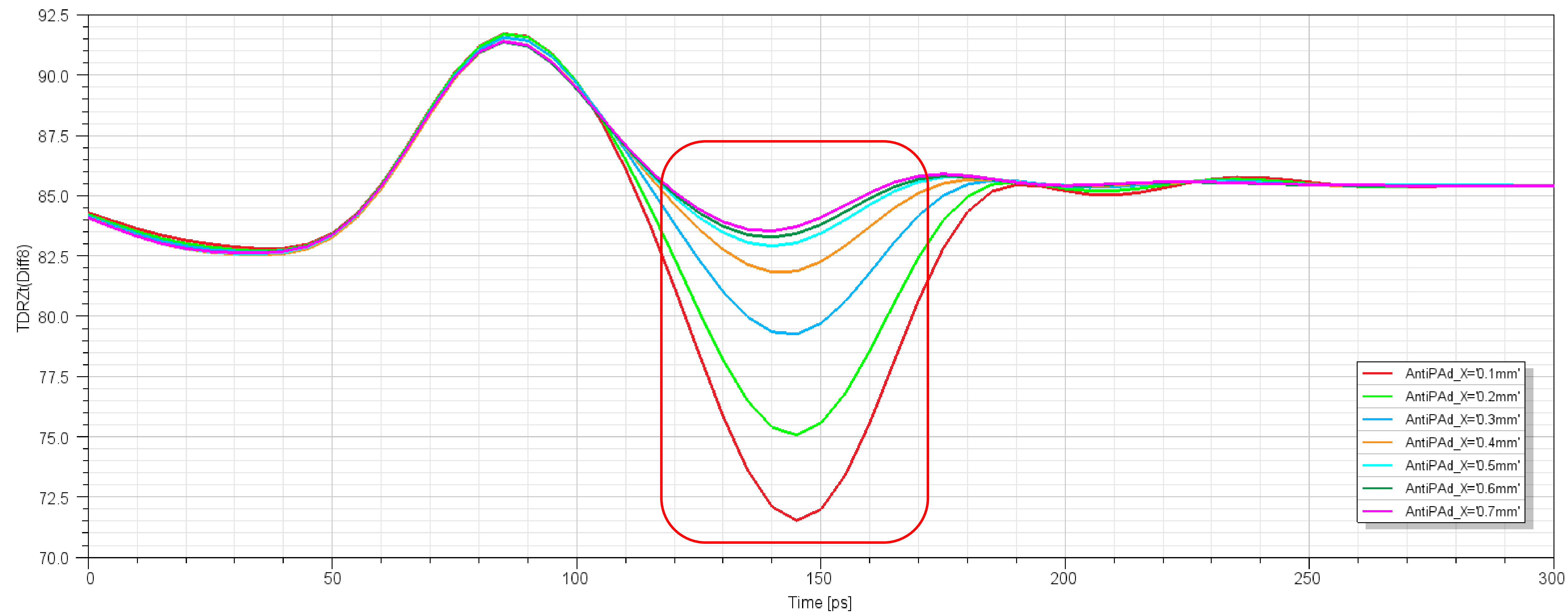


3mil to 7mil





Why is that?



How about RF connector?

RF connectors

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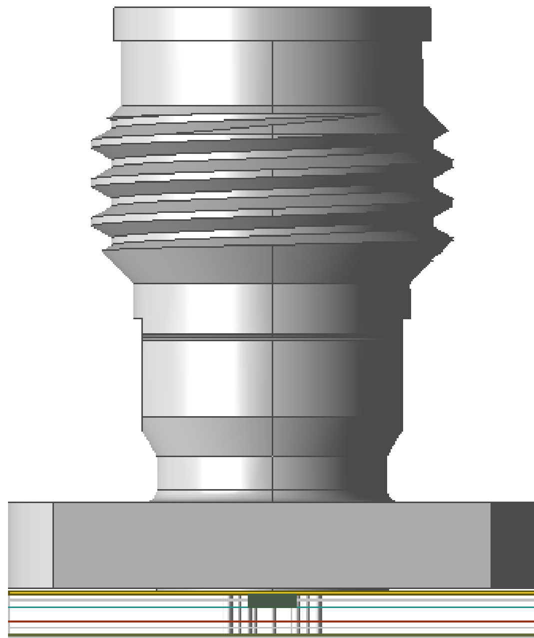
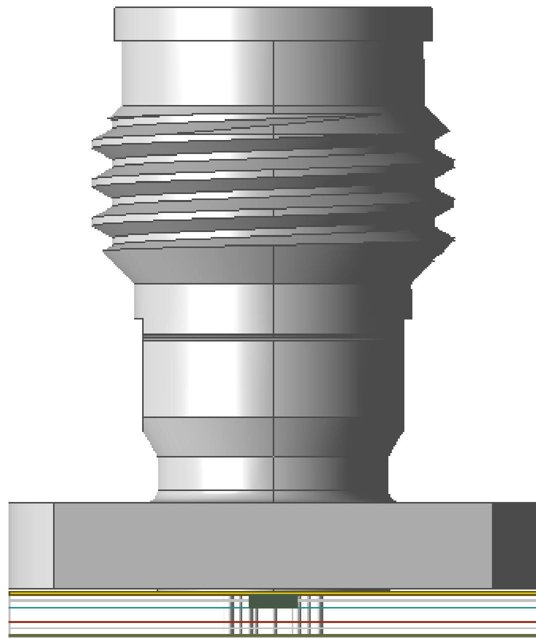


Full mated model
with specified PCB design

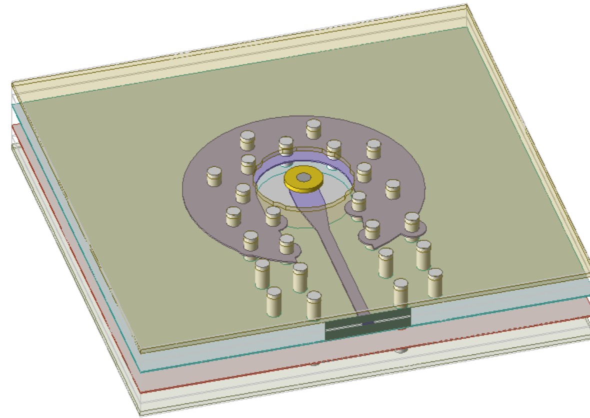
Everything inside the PCB will change the result

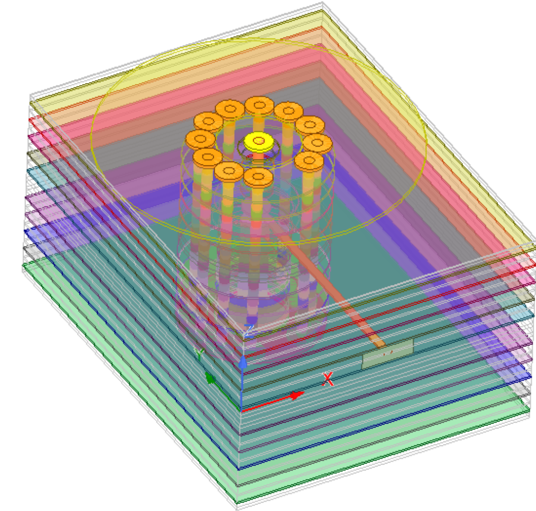
- **Stack-up**
- **Via type: mechanical drill, uVia, blind via…**
- **Via dimensions: pad size, drill size, back-drill**
- **Breakout Layer: via length**
- **Ground via pattern**

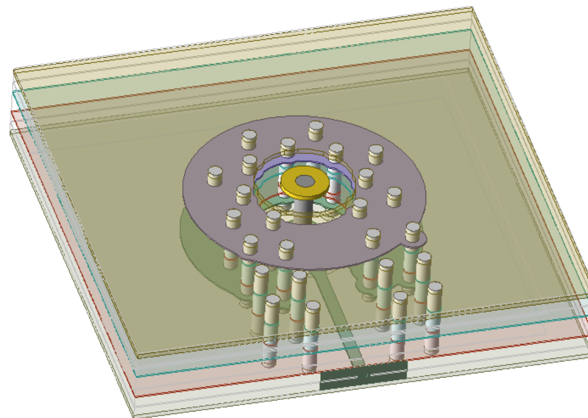
Connector with PCBs

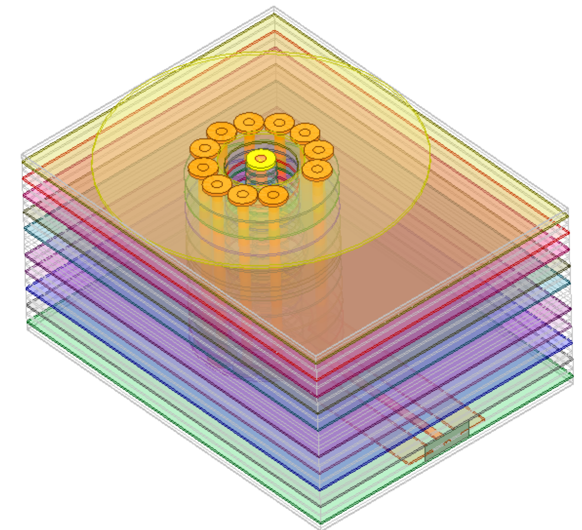


Full mated model

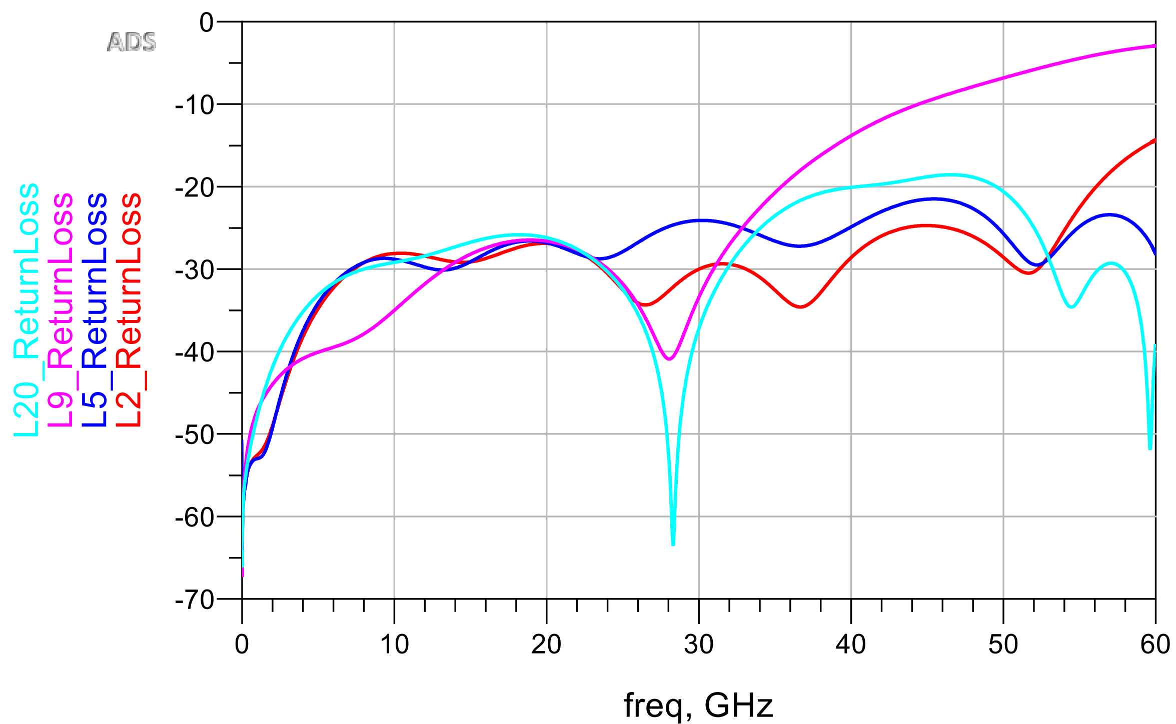


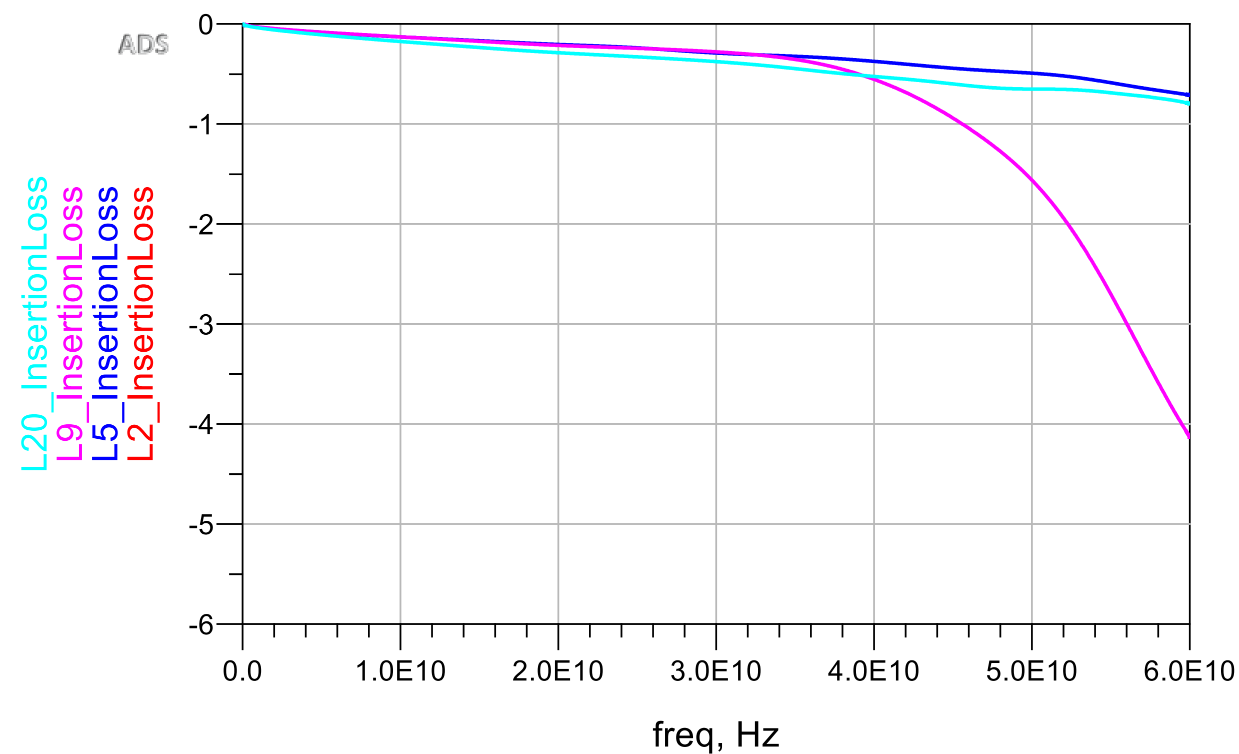






Results





Alternative

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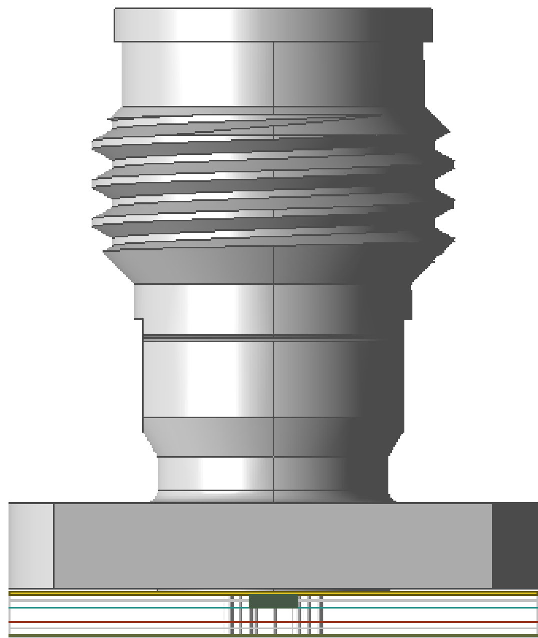
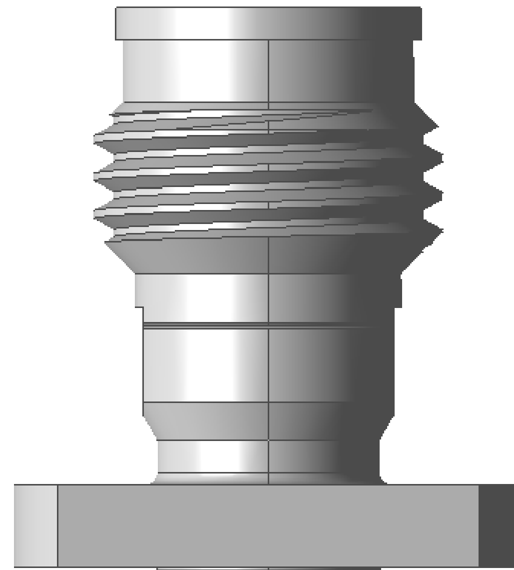
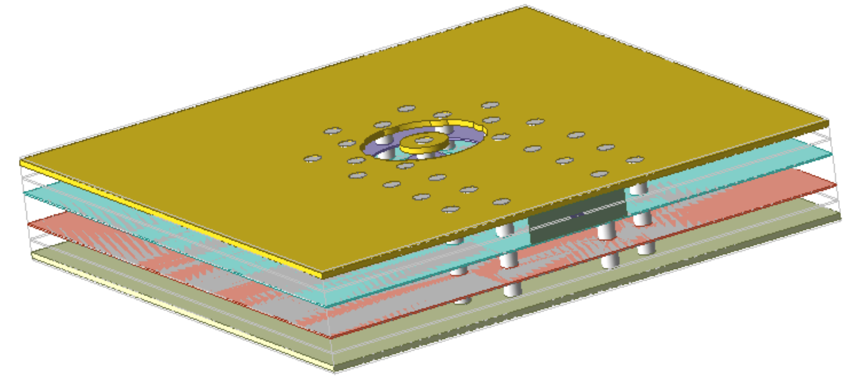


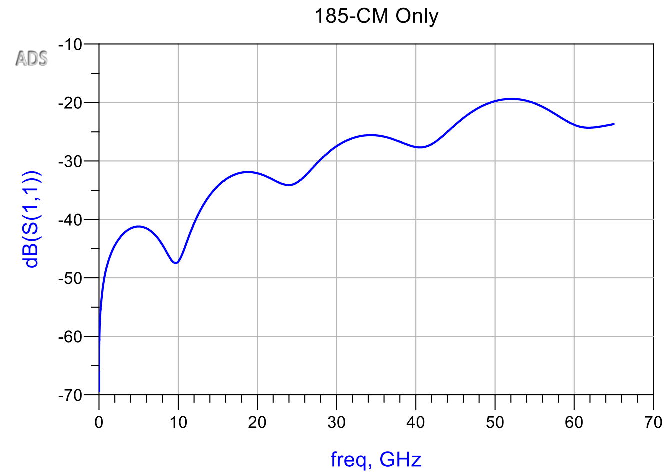
Full mated model

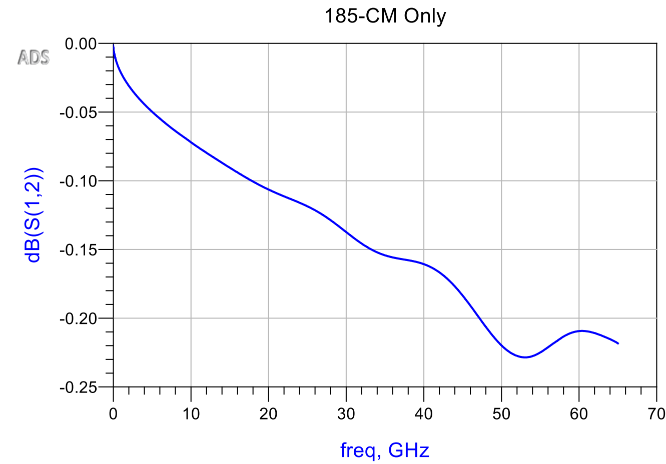


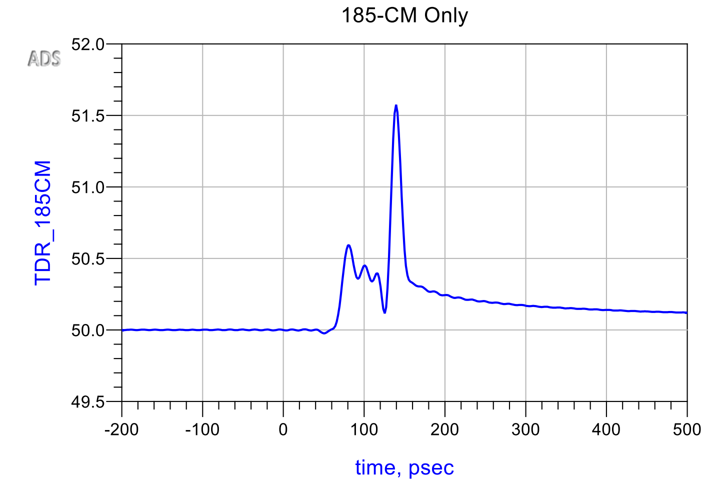


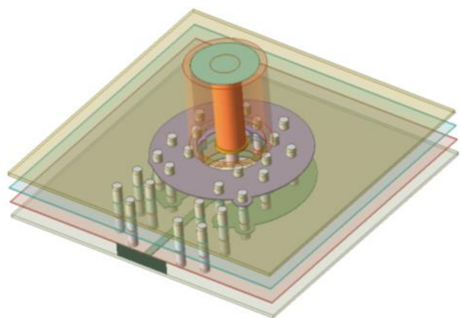
Concatenated model?

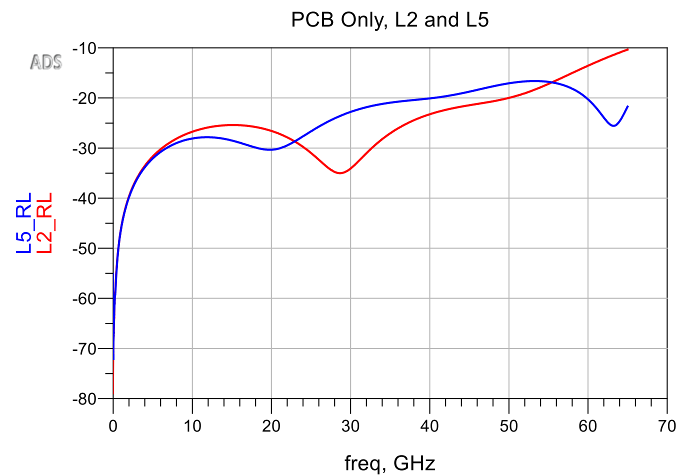
Let’s separate the models (L2 & L5)

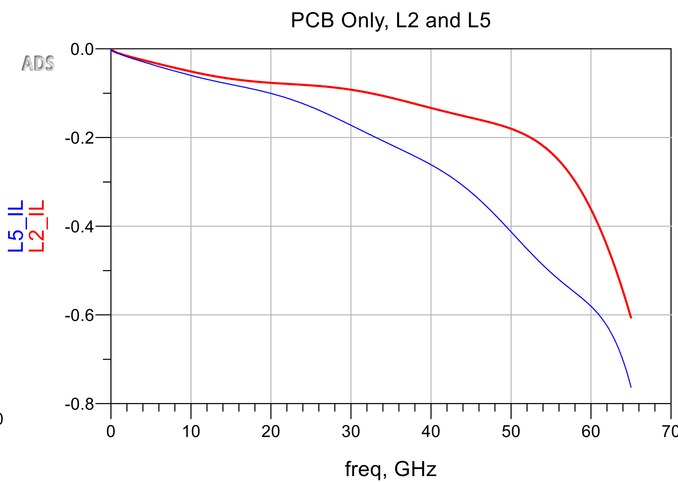


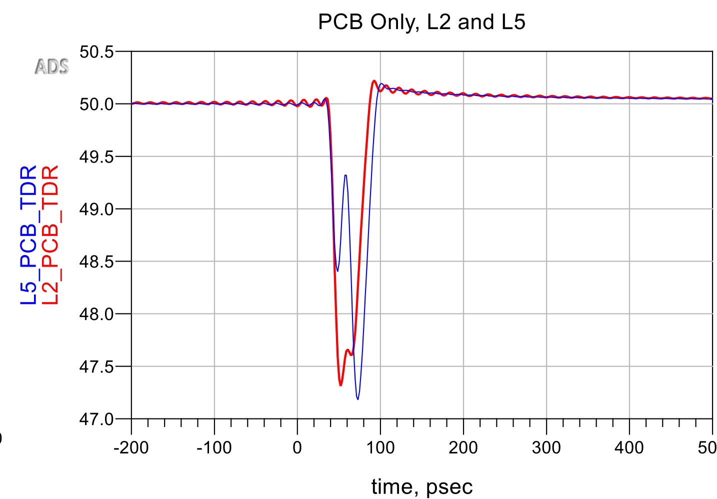




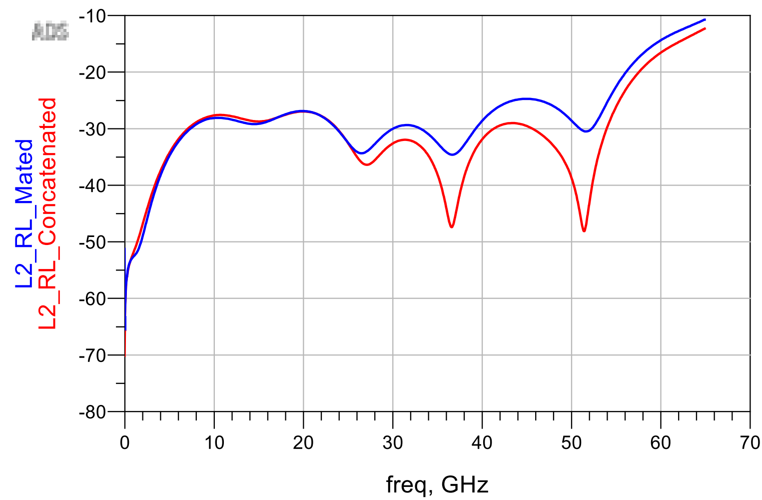


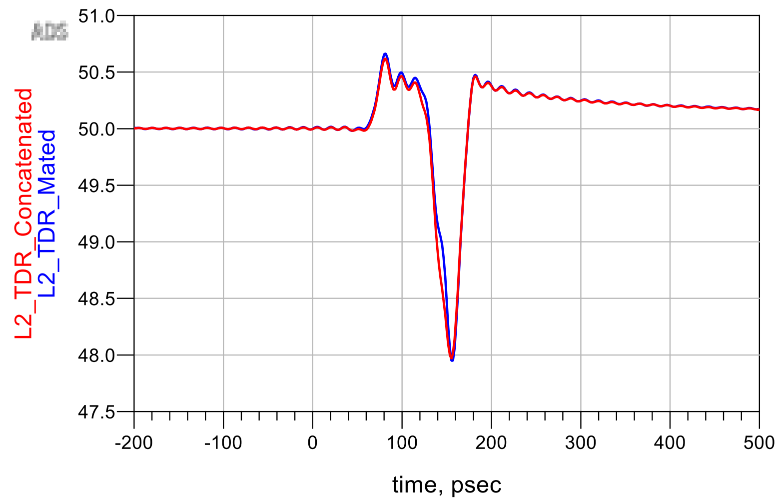


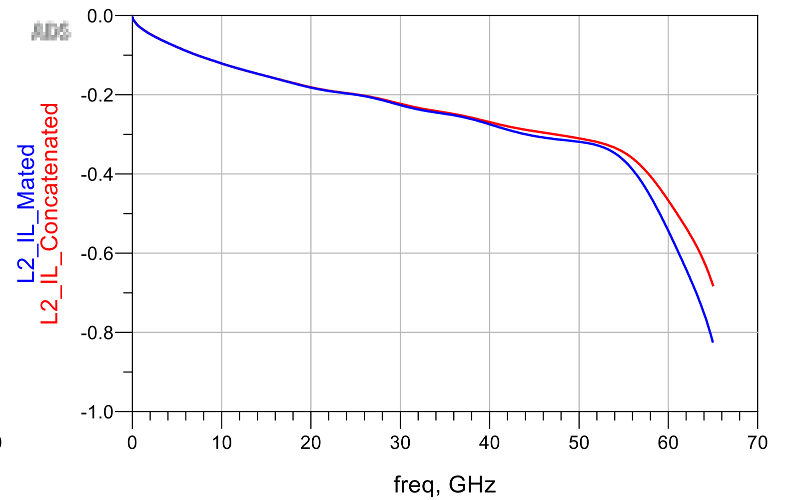


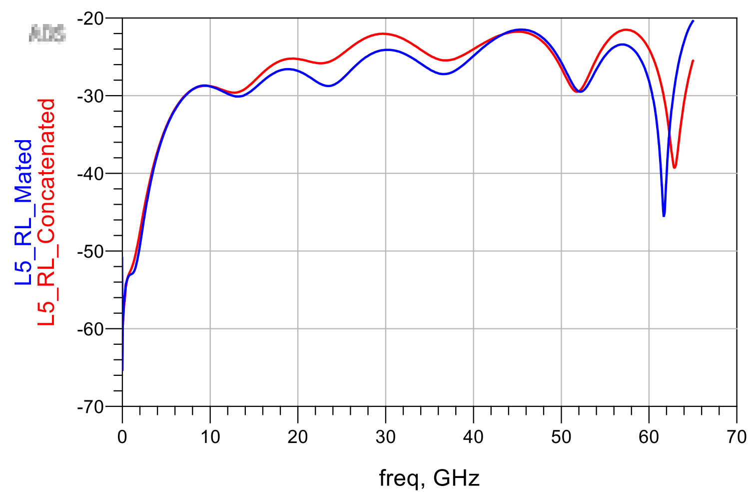


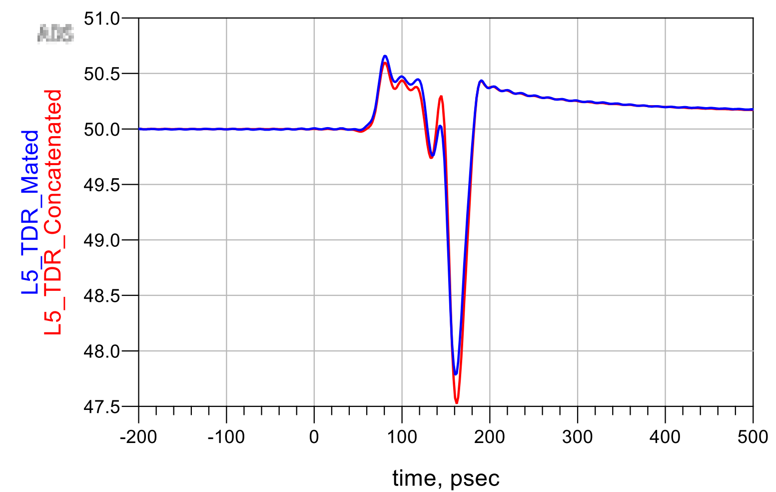
The comparisons (L2 & L5)

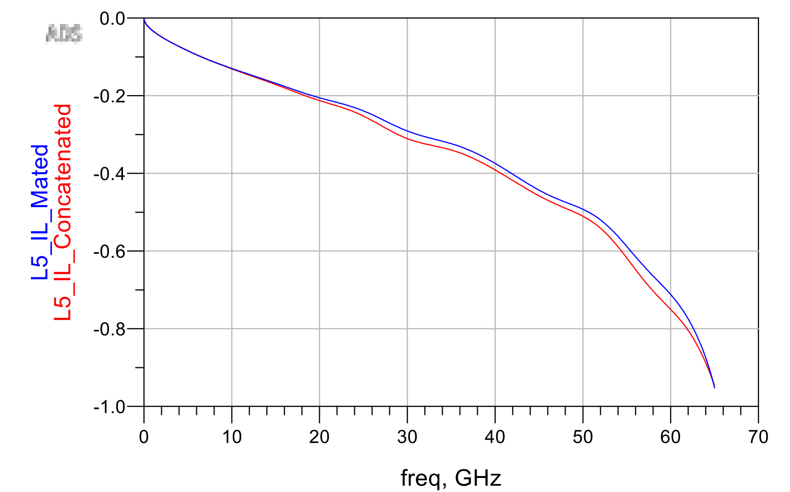




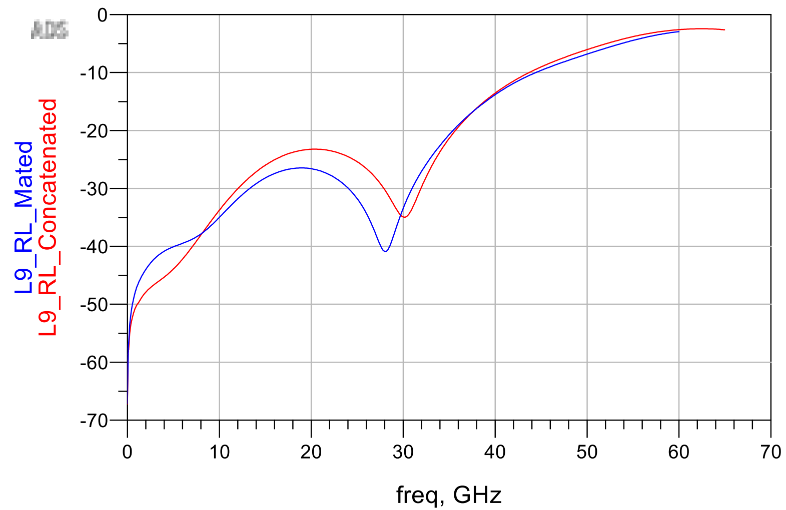


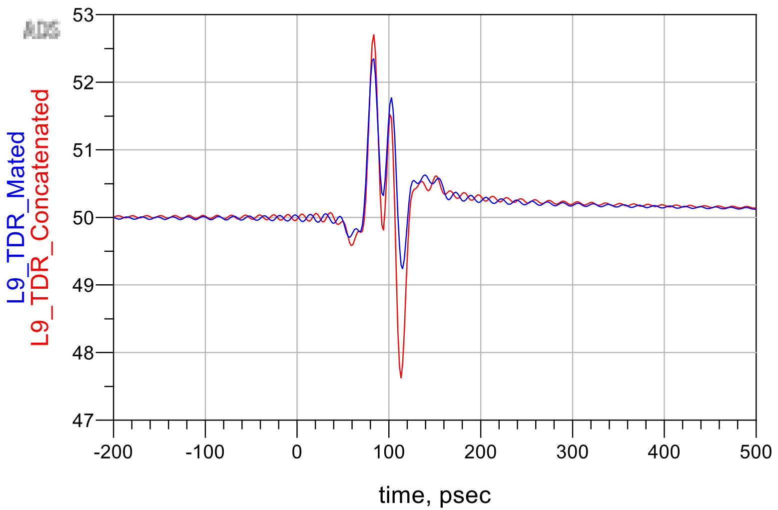


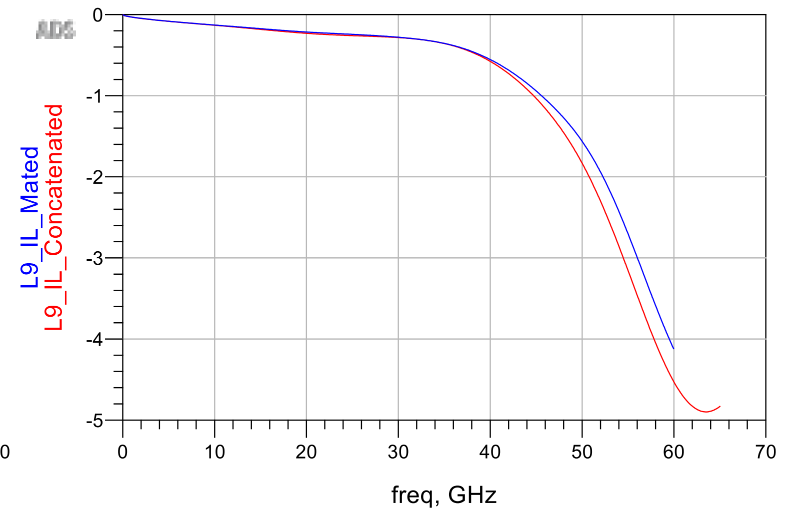


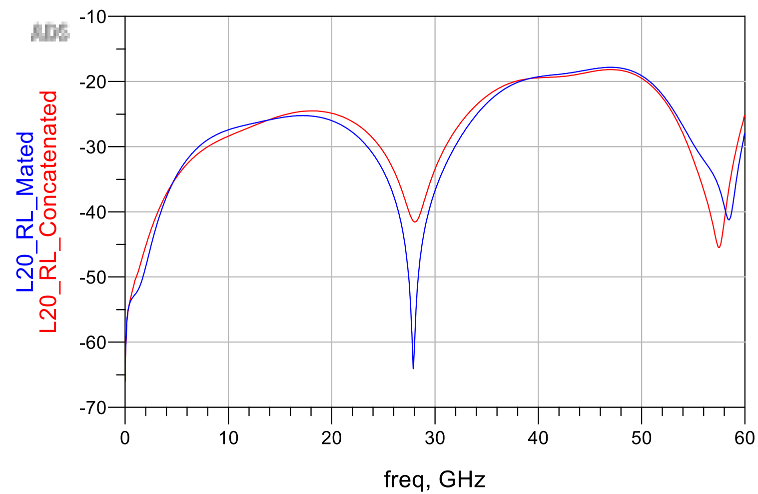


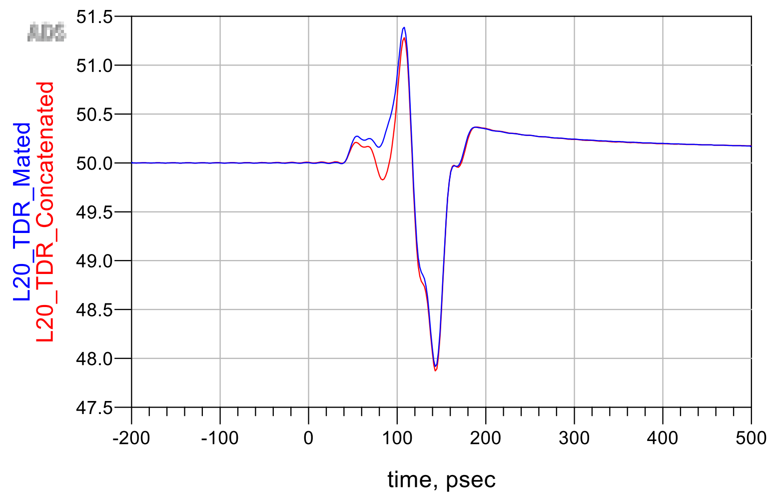
The comparisons (L9 & L20)

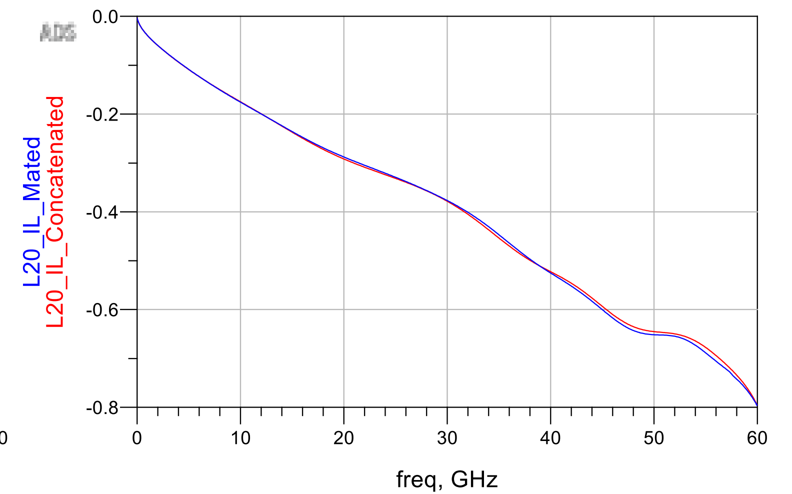






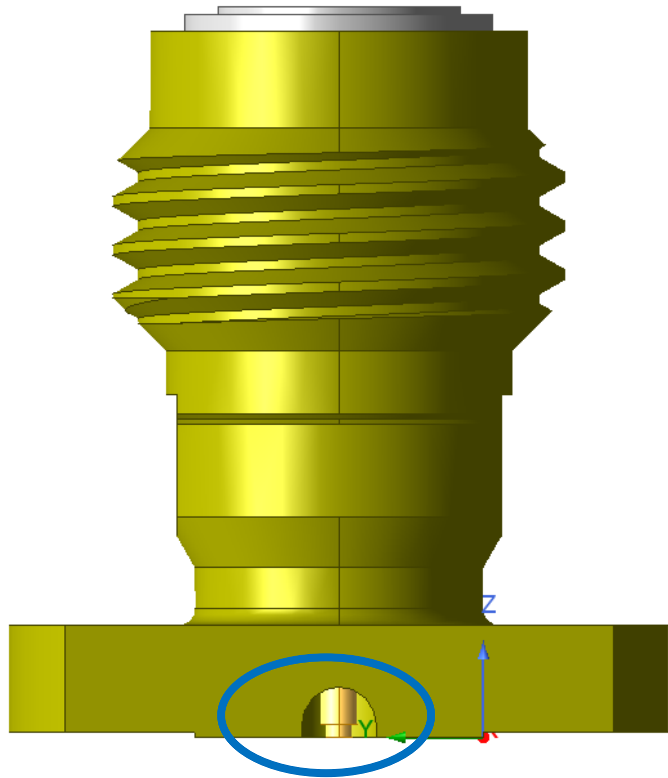


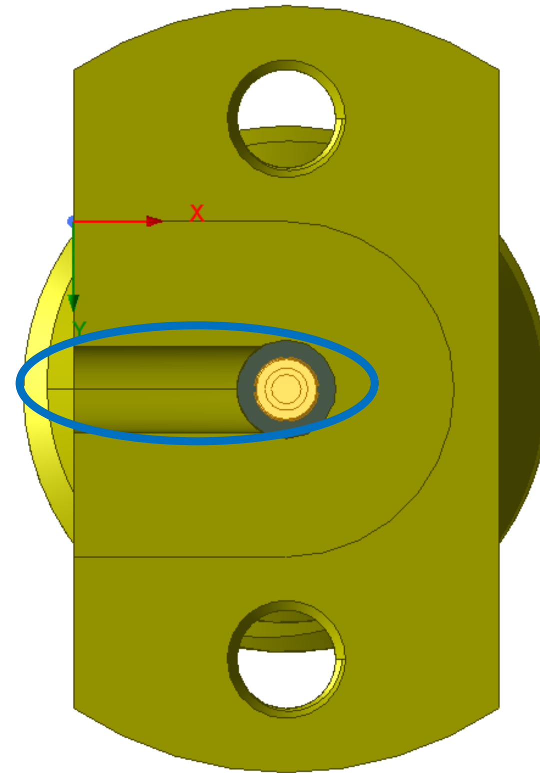




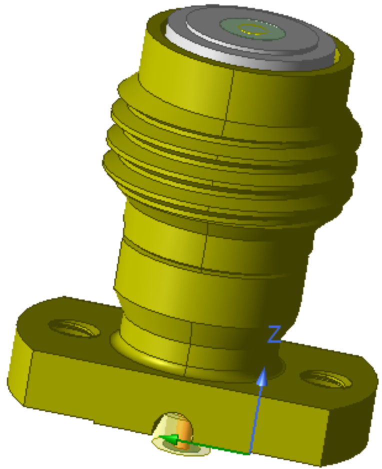
185-CMM – The microstrip version

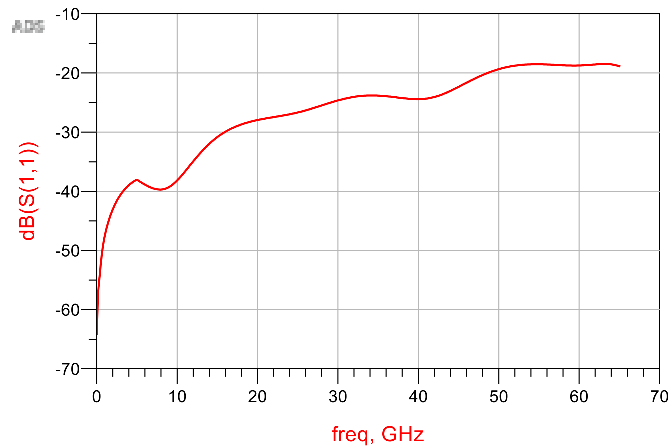
samtec

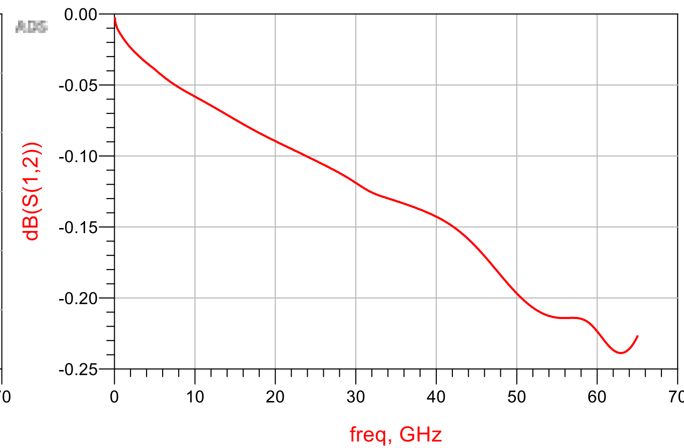


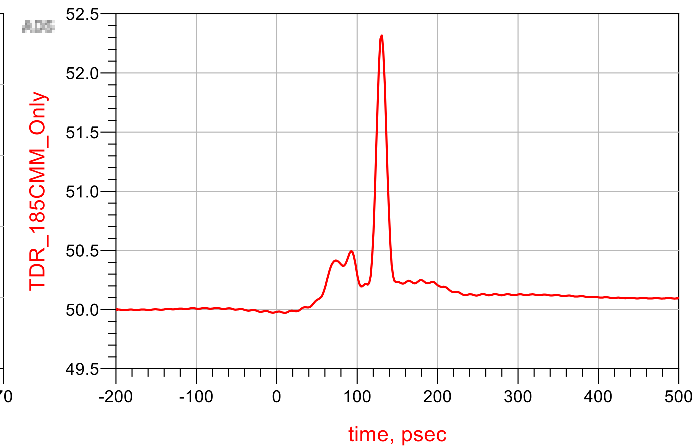


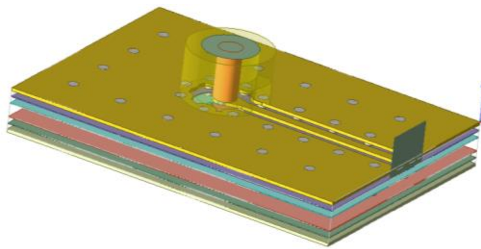
Separated model

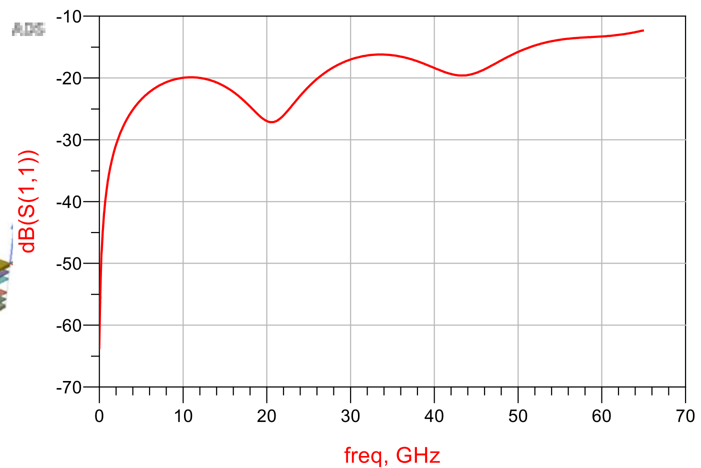


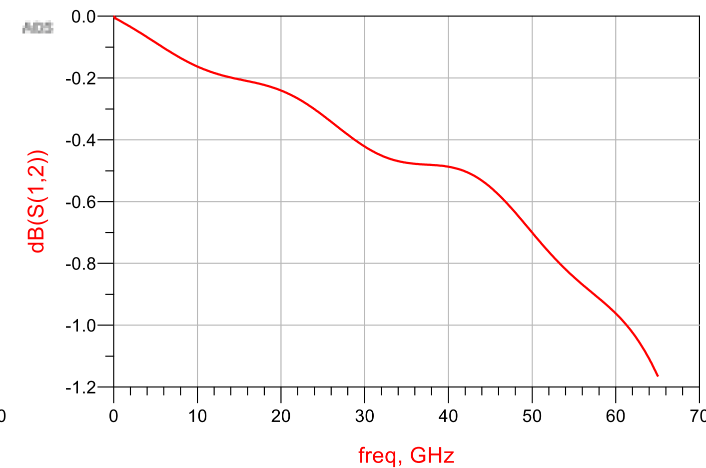


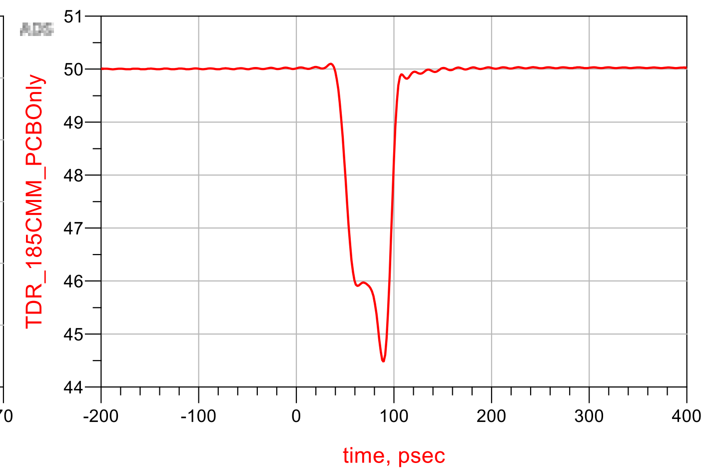




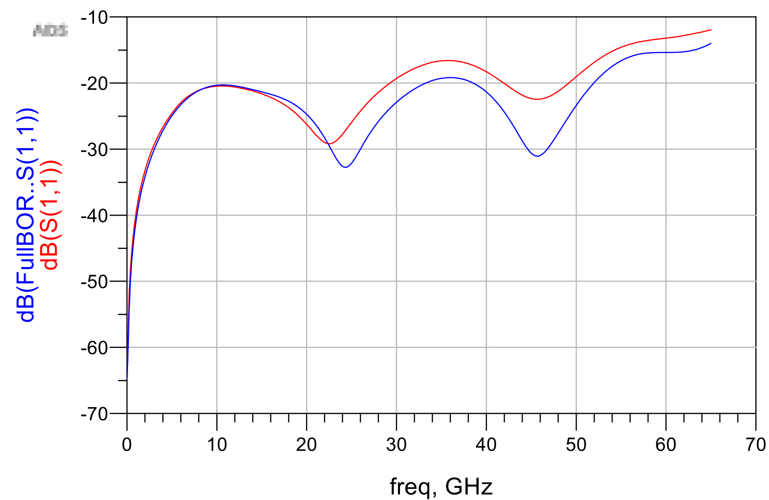


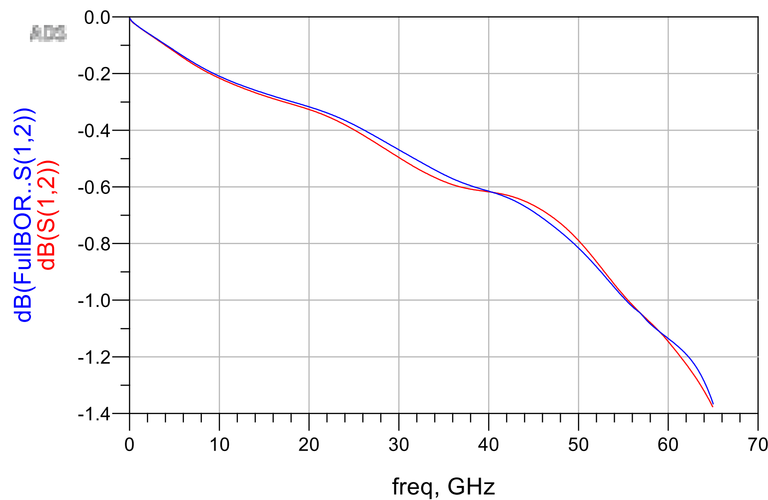


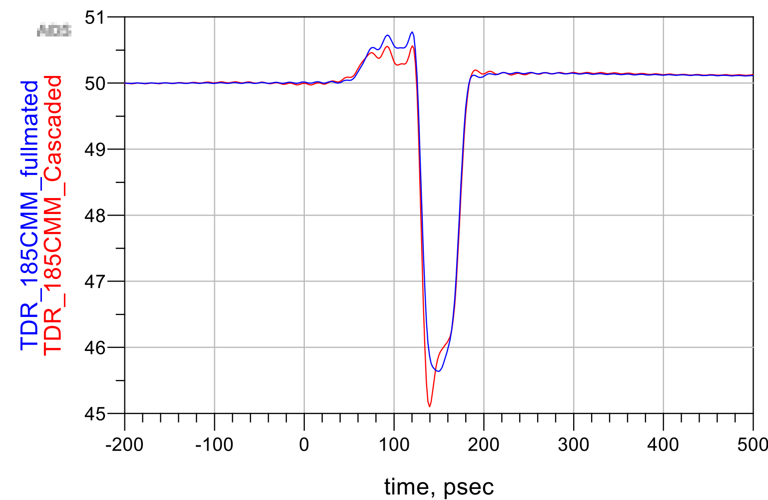


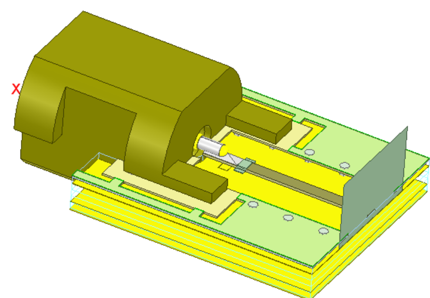


The comparisons- 185CMM

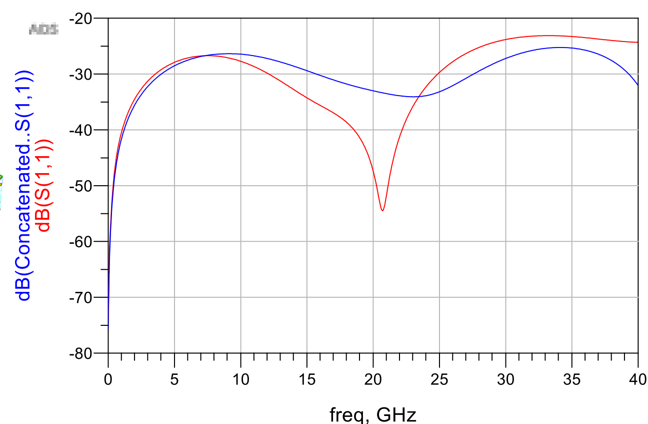


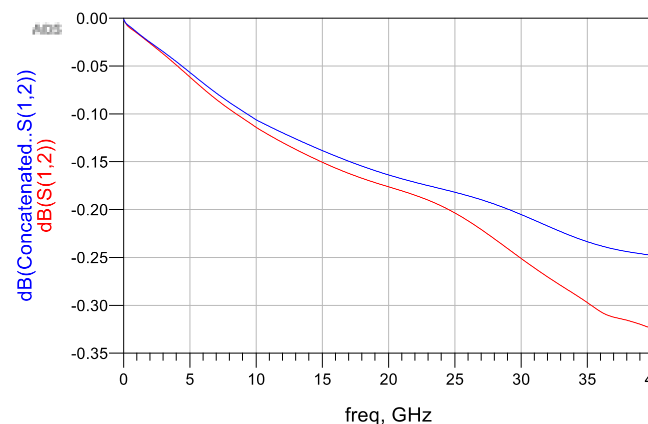


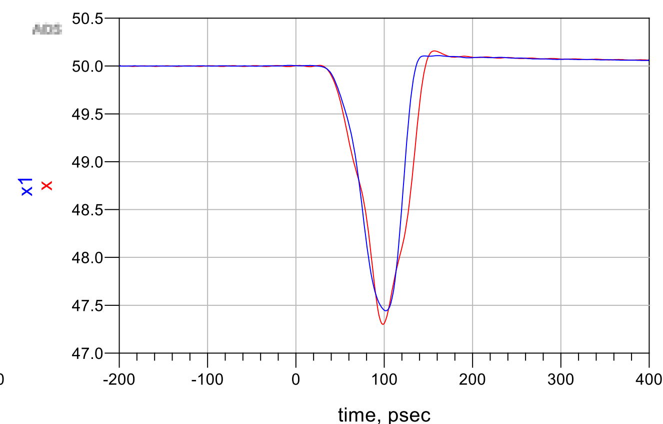




Doesn't work well







What if there is a big enough anti-pad?

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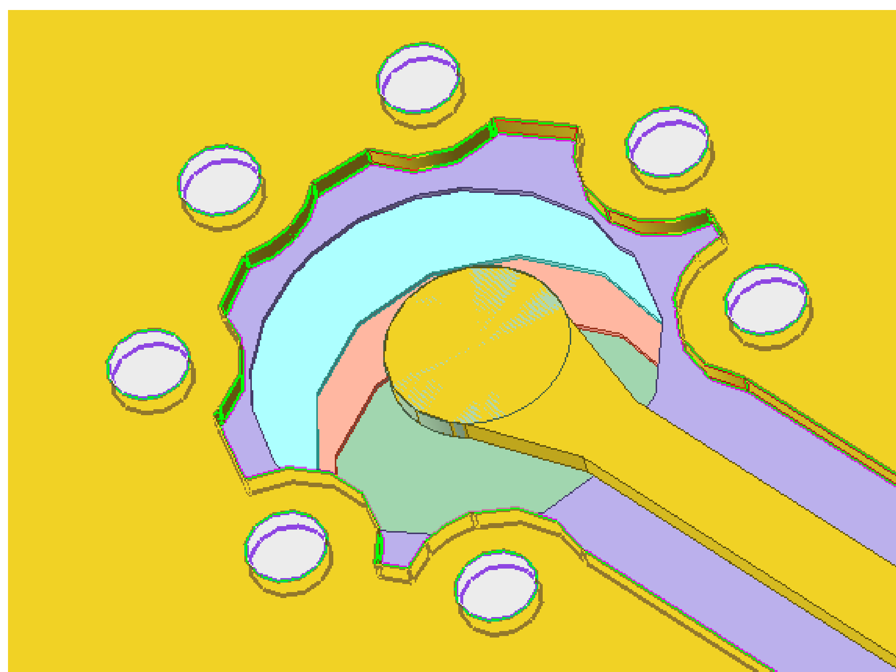


Ansys
2024 R1.1

StackMove = 0mil

Z
Y
X

0 1.5 3 (mm)

No, it doesn't work!

Terminal S Parameter Plot 2

BOR_SweepStackup

Ansys
2024 R1.1

dB(St(Coax_CC_T1,Coax_CC_T1))

0
-10
-20
-30
-40
-50
-60
-70

0 10 20 30 40 50 60 70

Freq [GHz]

dB(St(Coax_CC_T1,Coax_CC_T1))
Setup1 : Sweep
StackMove='0mil'

dB(St(Coax_CC_T1,Coax_CC_T1))
Setup1 : Sweep
StackMove='1mil'

dB(St(Coax_CC_T1,Coax_CC_T1))
Setup1 : Sweep
StackMove='2mil'

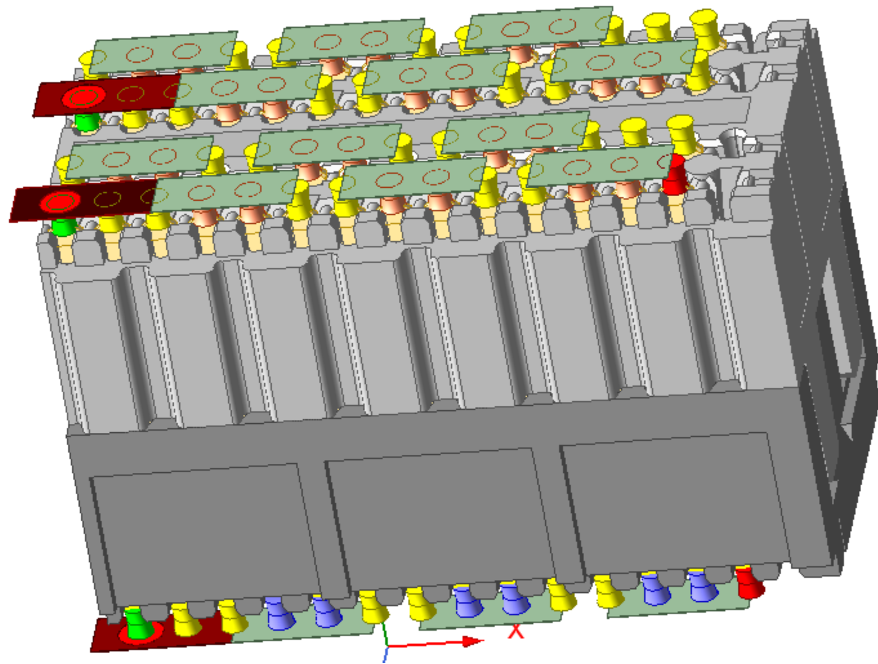
dB(St(Coax_CC_T1,Coax_CC_T1))
Setup1 : Sweep
StackMove='3mil'

dB(St(Coax_CC_T1,Coax_CC_T1))
Setup1 : Sweep
StackMove='4mil'

What we have learned here

- Model for two row SMT connector is more forgiving to the PCB effects
- For RF connector, a model for connector with specified PCB launch would be suggested
- For coax-like RF connector (strip-line breakout), it’s possible to offer/use connector-only model for models cascading.
- For none-coax-like RF connector (micro-strip), connector-only model is not practical
- PCB effects become dominator when signal path is inside the PCB

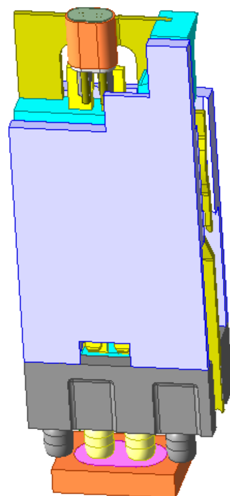
Array connector: We don't have a choice

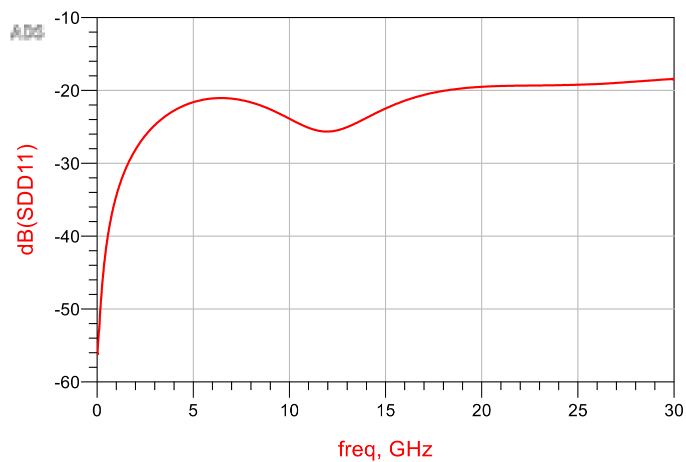


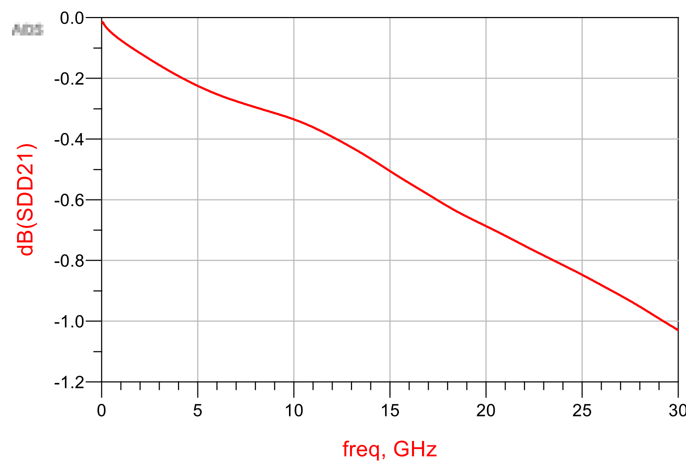
Connector only model

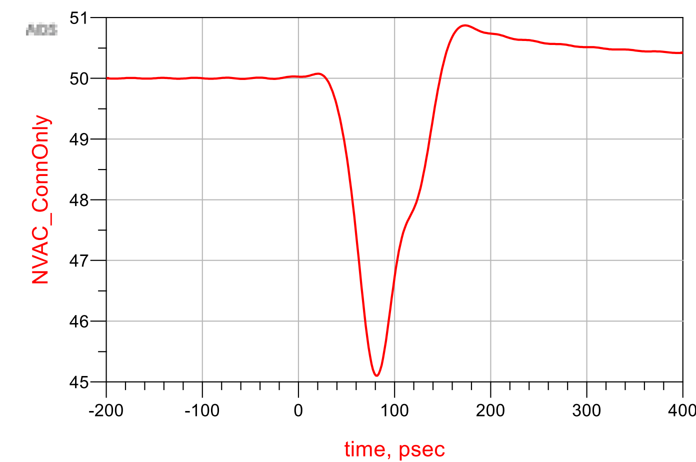
- Correlated model
- Ports set on solder ball/pad
- Pre-defined pinout
- Cascading PCB model by customer is required since the board effect is not predictable

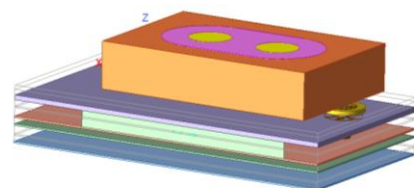
Separated models

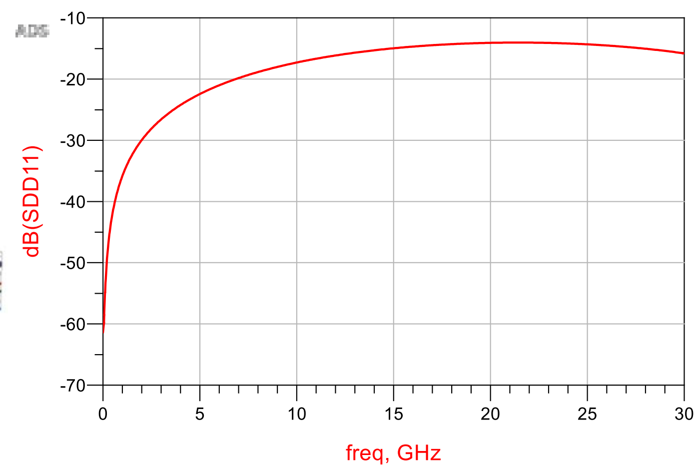


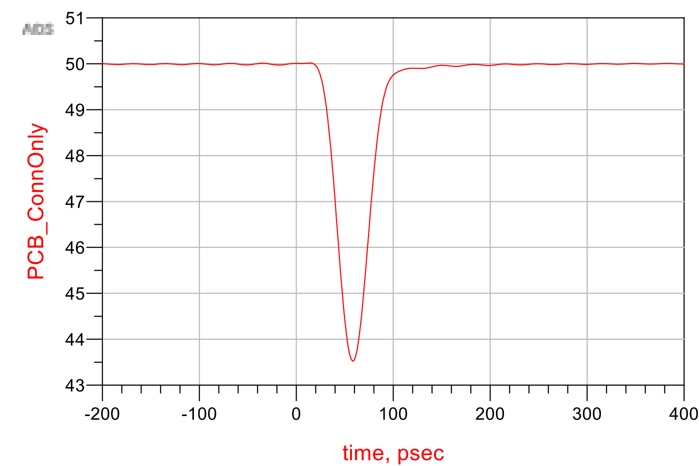




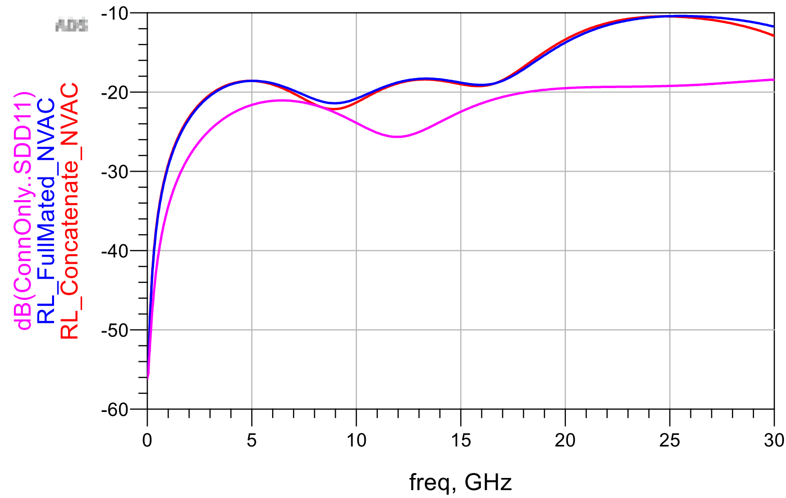


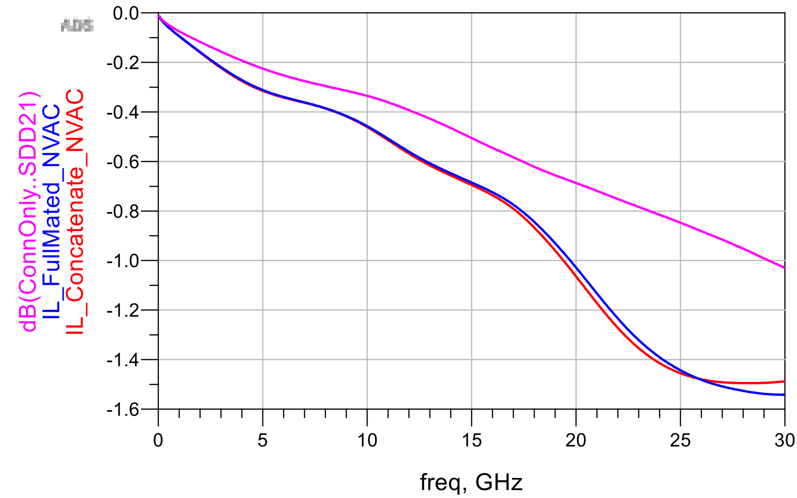


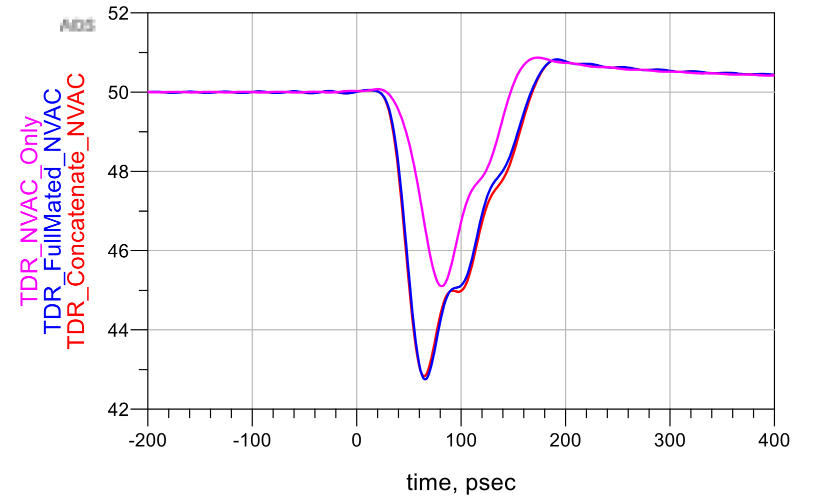




Yes! Model Cascading works



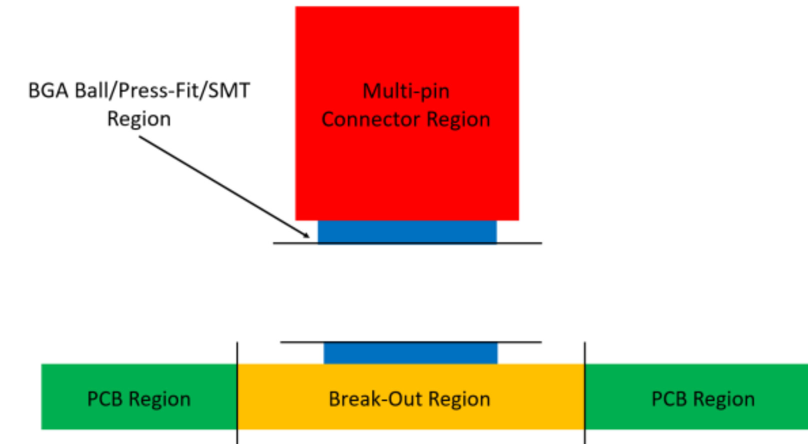




Cascading models or End-to-End model?

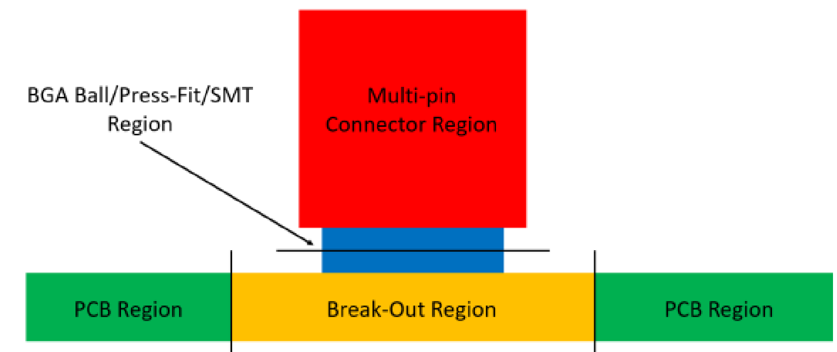
Cascaded Interconnect Model:

- A separate and then cascaded simulation of the geometry
  - There is a cut made in the simulation
  - Typically, this is done at the BGA region
- Allows for the mixing and matching of parts
- Smaller simulation results in a shorter run-time

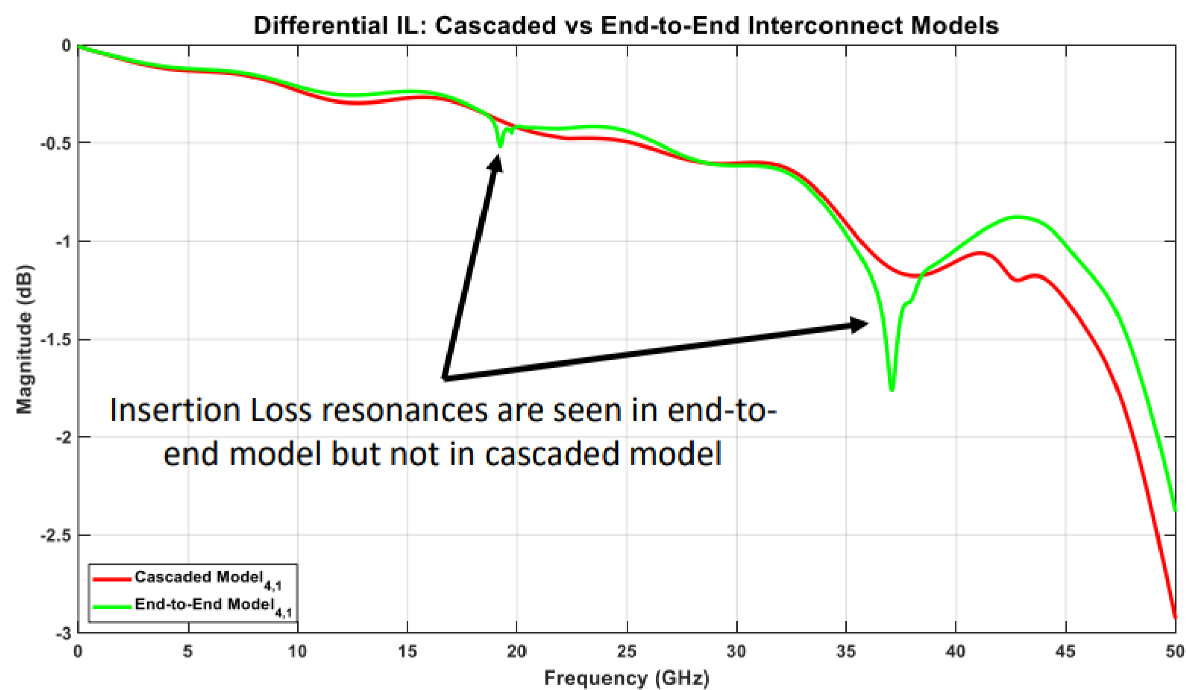


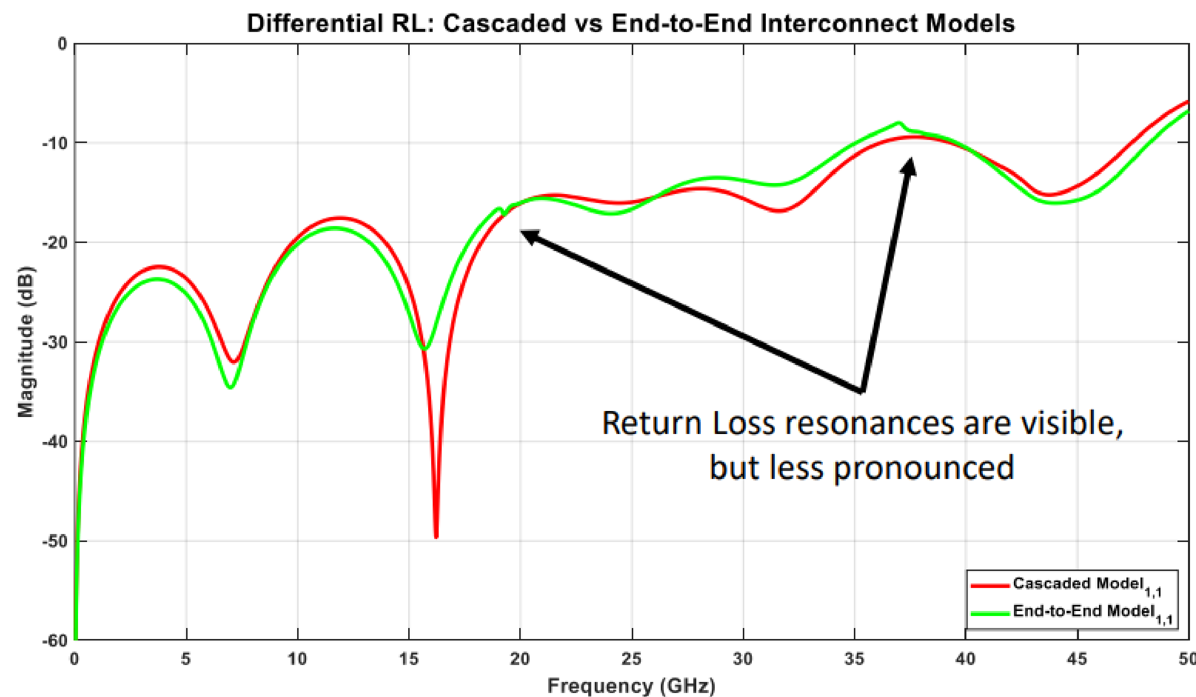
End-to-End Interconnect Model:

- A continuous and complete simulation of the geometry
  - There are no cuts made in the simulation
- More closely mimics actual performance in a system • Larger simulation results in a longer run-time

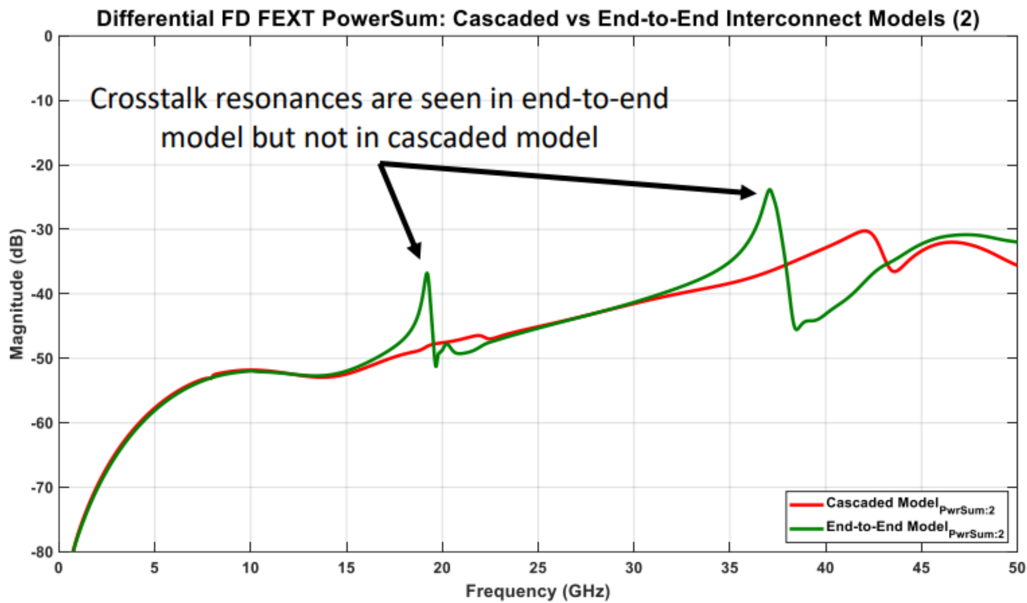


Performance Impact

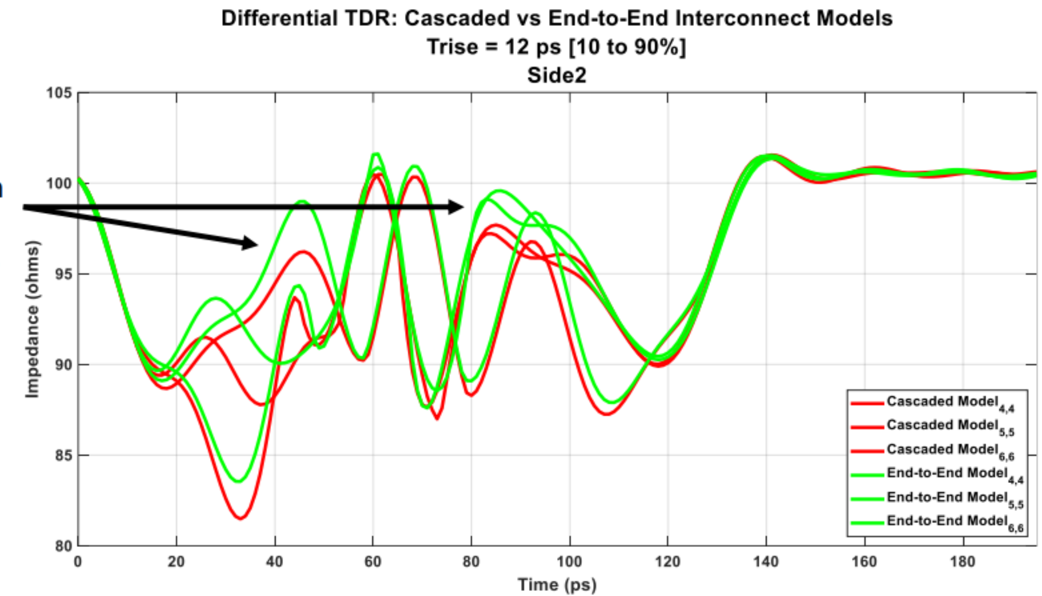




Performance Impact



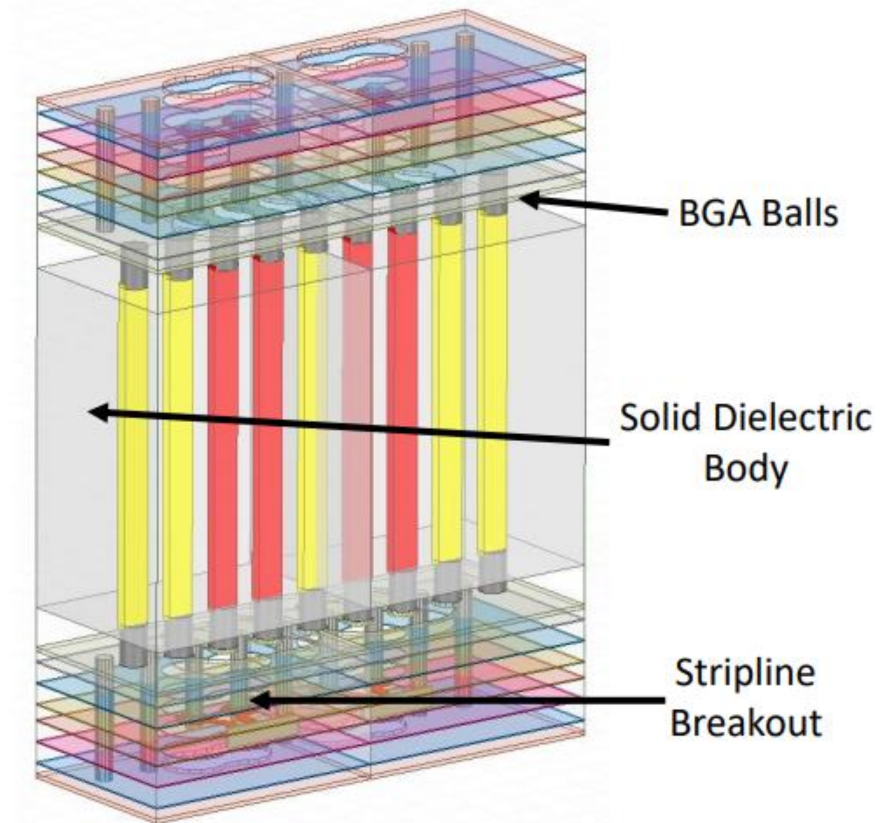
There is a small impedance impact in the boundary region between the models, which is instead continuous in the end-to-end model



Simplified Test Model

samtec

- This model was made to mimic the performance of a real connector
- Design Metrics:
  - 5mm Height
  - BGA Ball Attach
  - Short L1 Microstrip to Via
  - L8 Stripline Routing
- While simplified, this design displays similar characteristics of the real connector shown in previous slides



Isolating the Resonance

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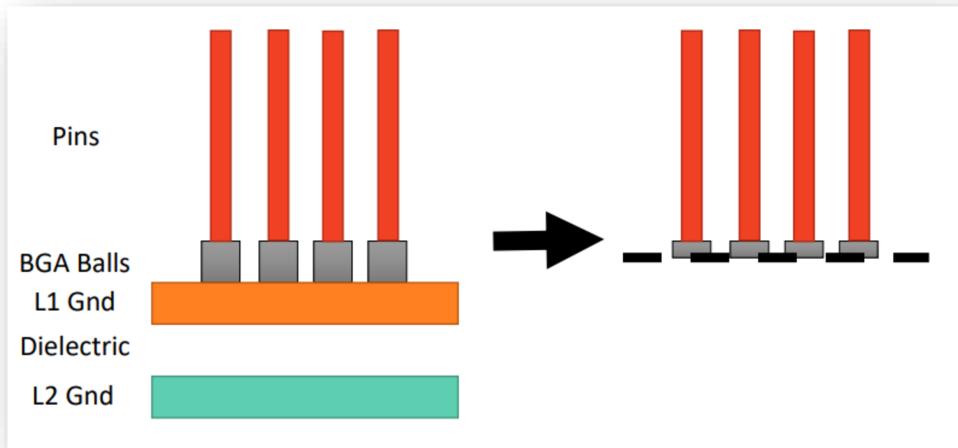
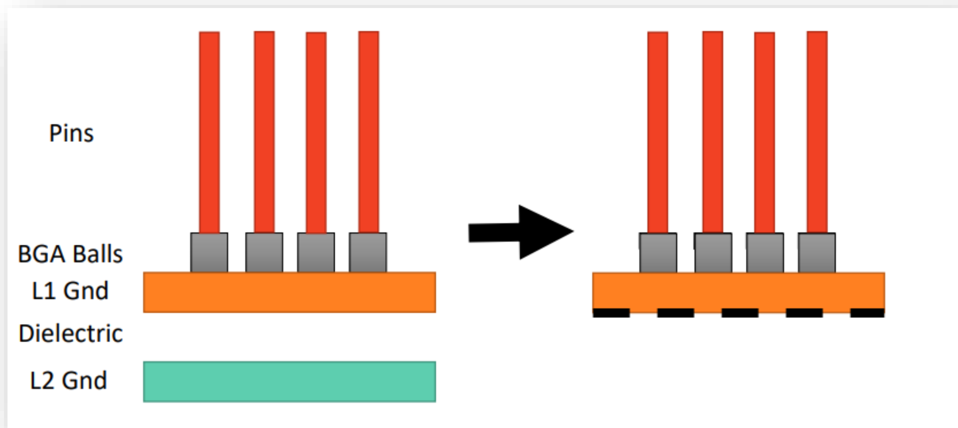
Do not resonate ← | → Resonate

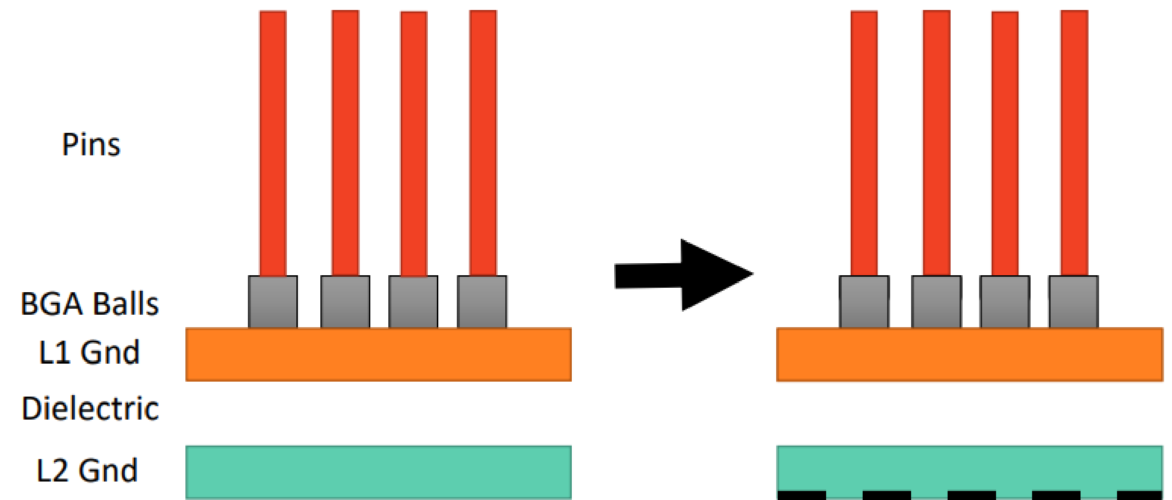
CUT AT BGA BALLS



CUT AT L1 GND PLANE

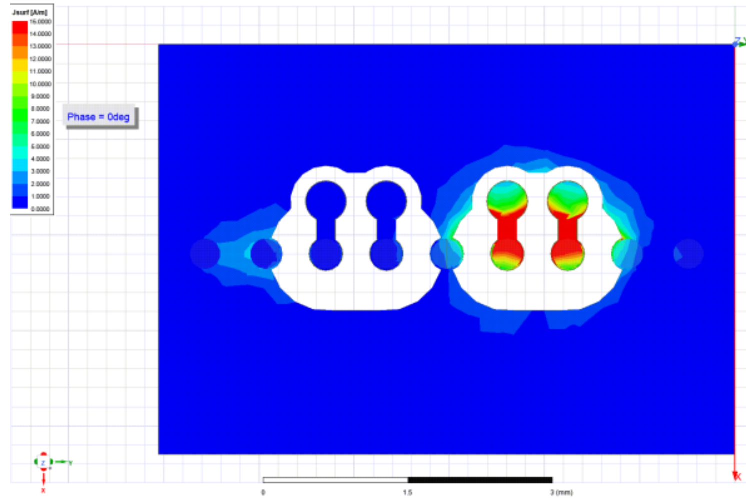


CUT AT L2 GND PLANE

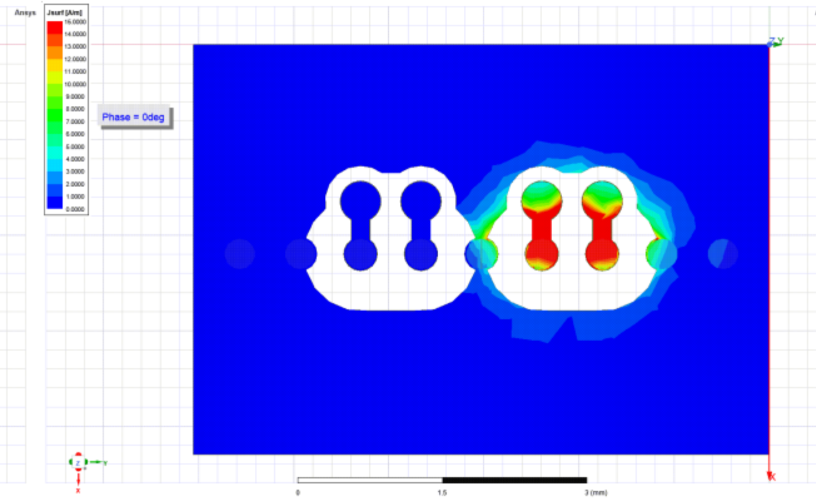


EM-Field

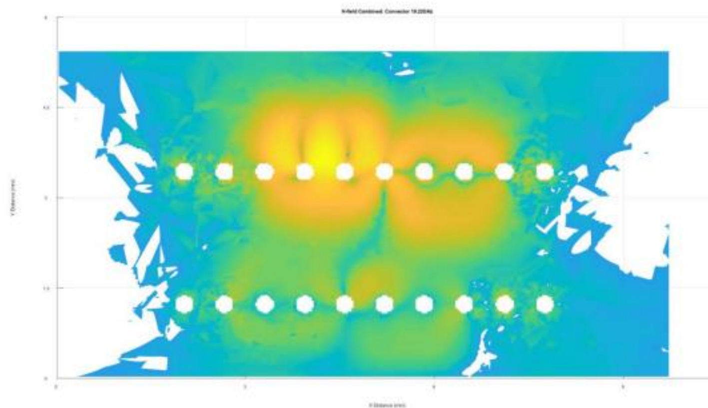
Simulation with Resonance



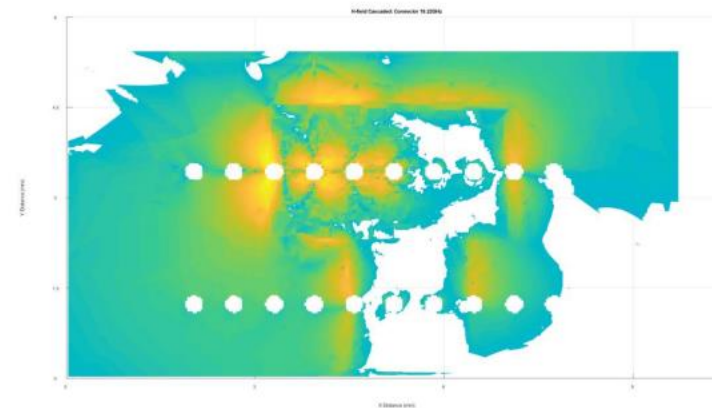
Simulation without Resonance



Simulation with Resonance



Simulation without Resonance



Additional Resonance Considerations

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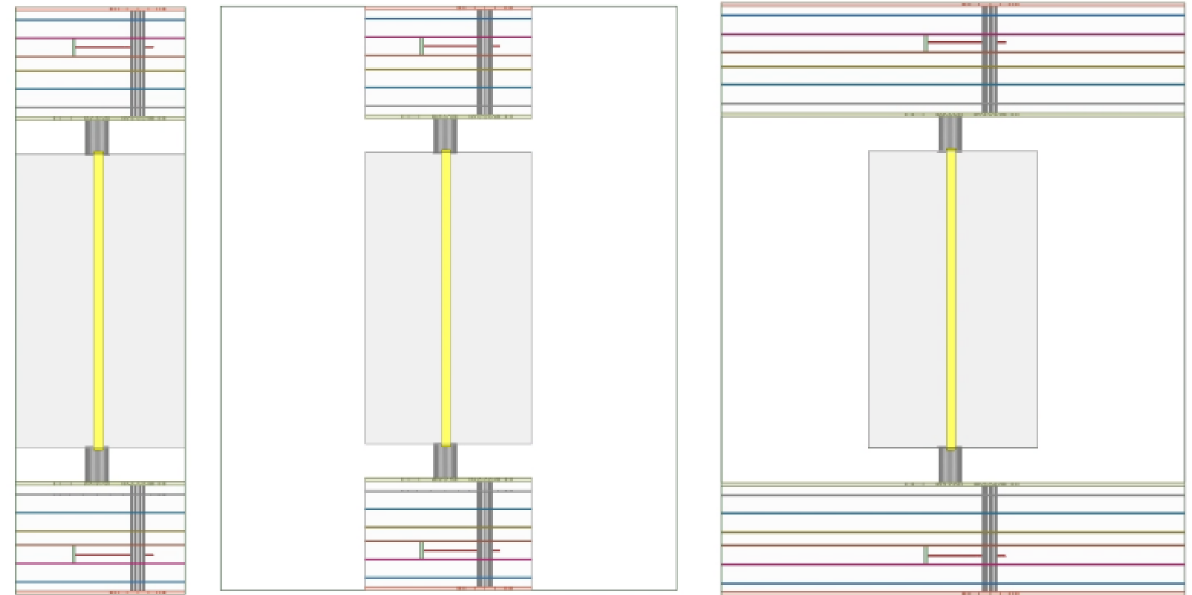
- It is important to consider all possible factors which could impact the presence/absence of a resonance
- Some possible factors:
  - Airbox boundary type
  - Airbox location
  - Size of ground planes
  - Impedance boundaries on unused pins
  - Via location in board
  - Grounding top plane of board



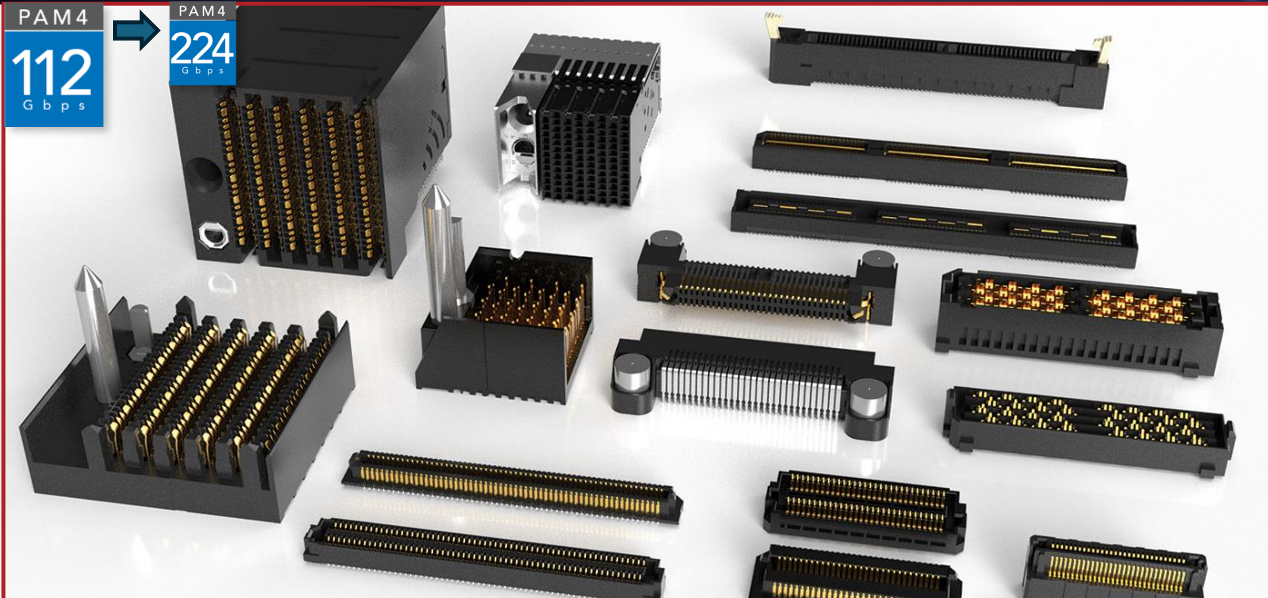
As we know…

Challenges for SI is endless!

Reference & Thanks

Robert Branson: Cascaded or End-to-End Models: What Do We Give Up?
https://www2.samtec.com/l/271452/2022-08-19/35krkg

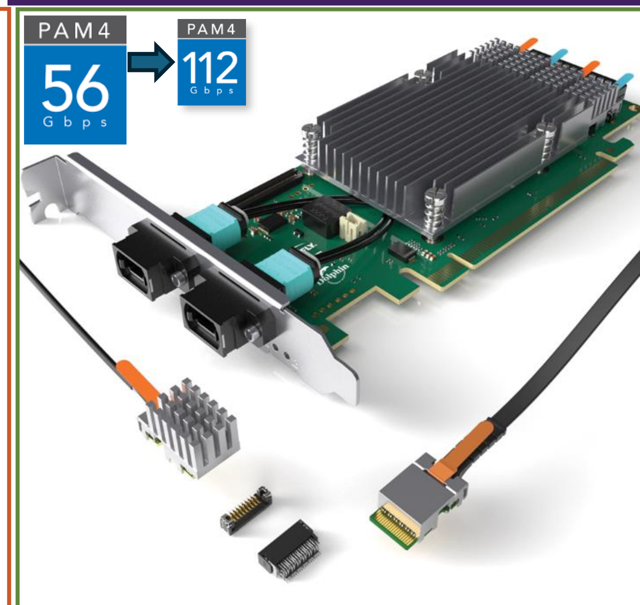
Alejandro Solis & Jason Chiang: material and information support
Henry Dai: Simulation support


PAM4
112
Gbps
PAM4
224
Gbps
HIGH-SPEED BOARD-TO-BOARD
OPEN-PIN-FIELD ARRAYS | GROUND PLANE STRIPS | ULTRA-MICRO | BACKPLANE

PAM4
112
Gbps
PAM4
224
Gbps
HIGH-SPEED CABLE
FLYOVER® MID-BOARD & PANEL | BACKPLANE MICRO COAX & TWINAX

MAX
60
Amps
RUGGED/POWER
RUGGED BOARD-TO-BOARD | BLADE POWER
MICRO DISCRETE WIRE | RUGGED I/O | ULTRA RUGGED

FLEXIBLE STACKING
LOW PROFILE | PASS-THROUGH | ONE-PIECE
SKYSCRAPERS | SHROUDED HEADERS | IDC SYSTEMS


PAM4
56
Gbps
PAM4
112
Gbps
OPTICS
MICRO FLYOVER SYSTEMS™ | EXTENDED TEMP
PCI EXPRESS®-OVER-FIBER

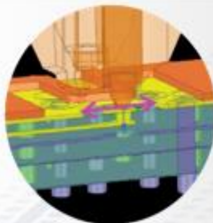
DC TO
110
GHz
RF
PRECISION RF | 50 Ω SOLUTIONS
75 Ω SOLUTIONS | ORIGINAL SOLUTIONS

Samtec TDC - Taiwan Design Center (RF Center)

Samtec Confidential

CABLES
Design & Fabrication
of Raw Cable
Cable Assemblies

CONNECTORS
Design & Fabrication
Cable Connectors
Board Connectors



TECH SUPPORT
Launch Optimization
Simulation & Testing
Full System Optimization

Vertical Integration
=
Full System Support

TDC (Taiwan Design & Manufacture center)

RF compression mount connector

NEXT GEN MICROWAVE CABLE

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Samtec Confidential

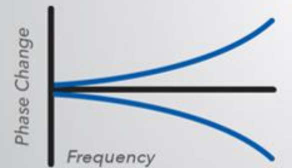
INTERLAYER IMPROVES STABILITY

Nitrowave™ Low-Loss Cable Construction with Interlayer

The addition of an interlayer improves stability resulting in more accurate, dependable performance.

Good Stability vs Flexure

With Interlayer



Poor Stability vs Flexure

Without Interlayer

Flex Life	
Unrestrained Flex	400,000 cycles

Multi-port solution

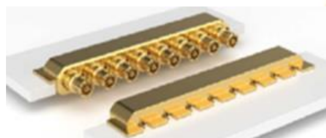
samtec

Samtec Confidential

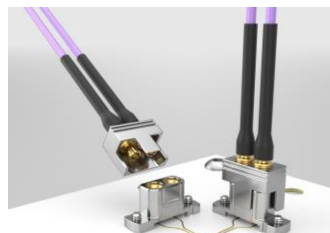
MAGNUMRF™ GANGED RF ASSEMBLIES

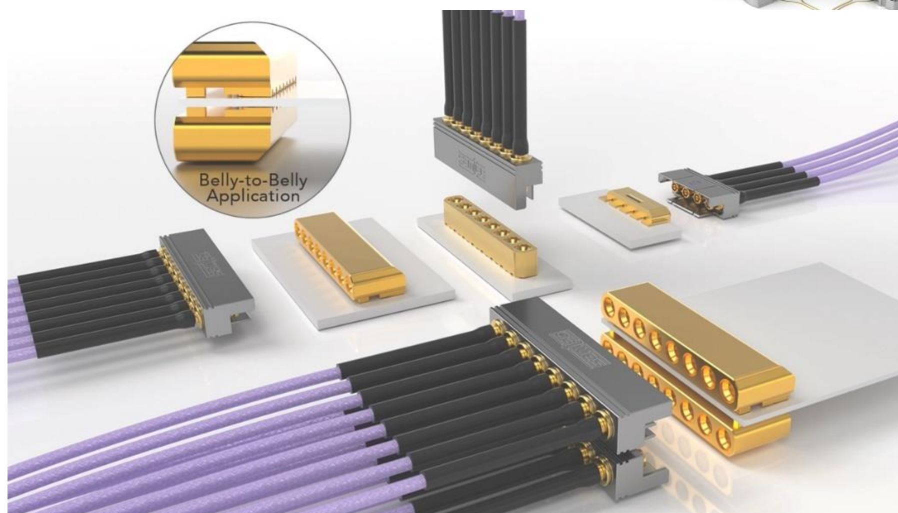
DC TO 65 GHz

Board-to-Board



Cable-to-Board

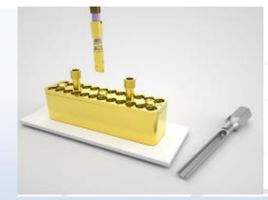
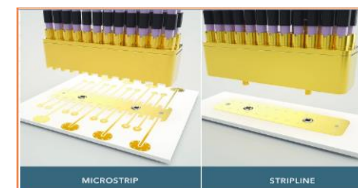




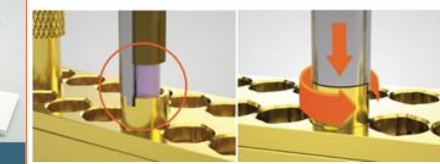
BULLSEYE® TEST POINT SYSTEM

PERFORMANCE TO 40/50/70/90GHz

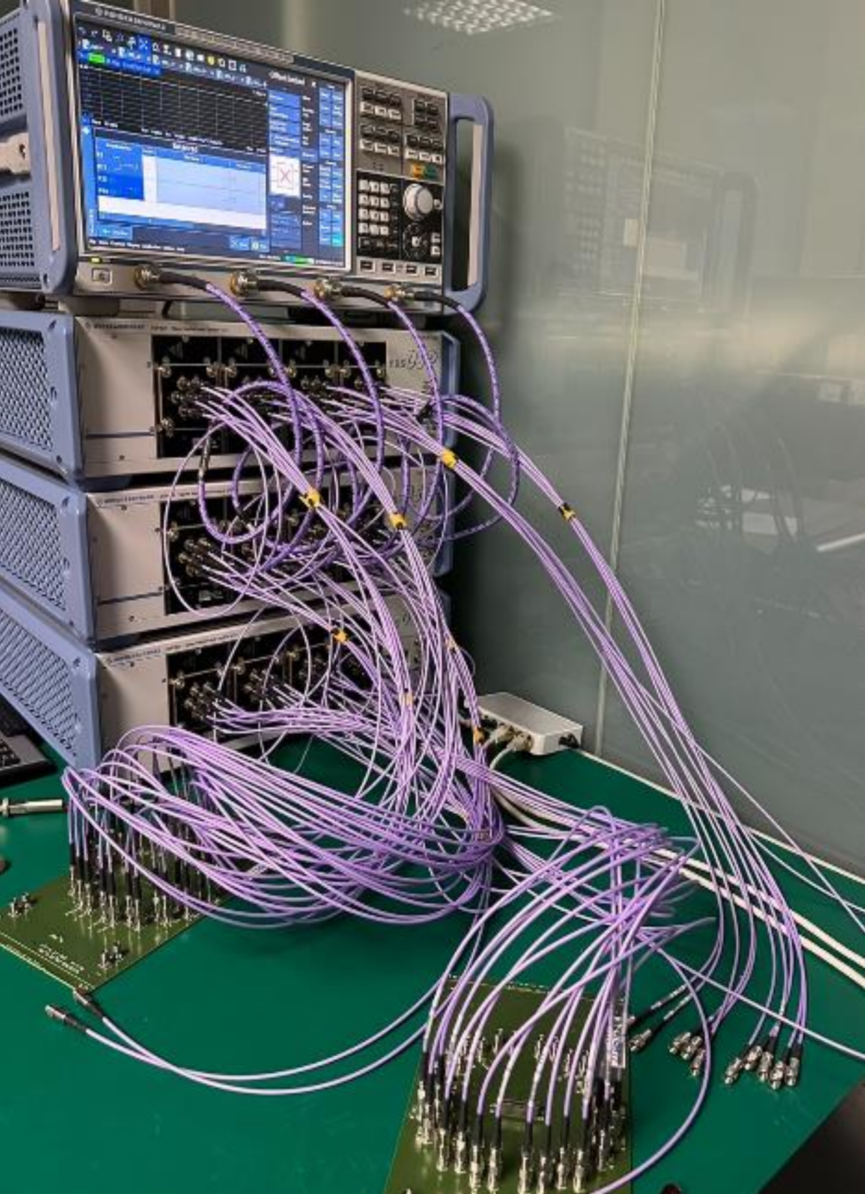
TEST ASSEMBLY	SERDES CHARACTERIZATION
BE90A, 90 GHz	PAM4 224 Gbps
BE70A, 70 GHz	PAM4 112 Gbps
BE40A, 50 GHz	PAM4 56 Gbps

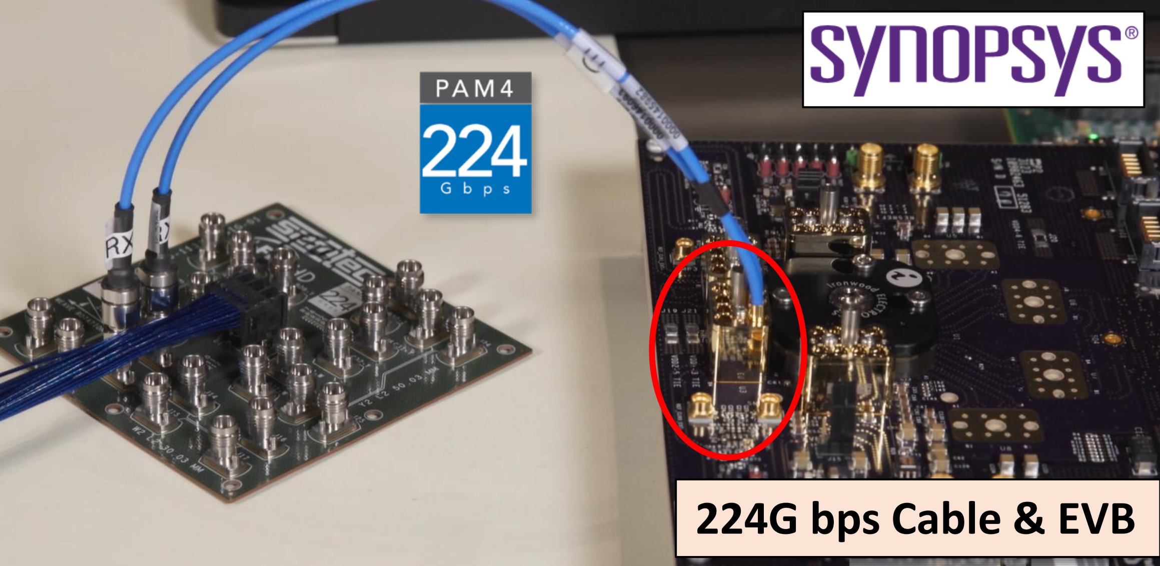



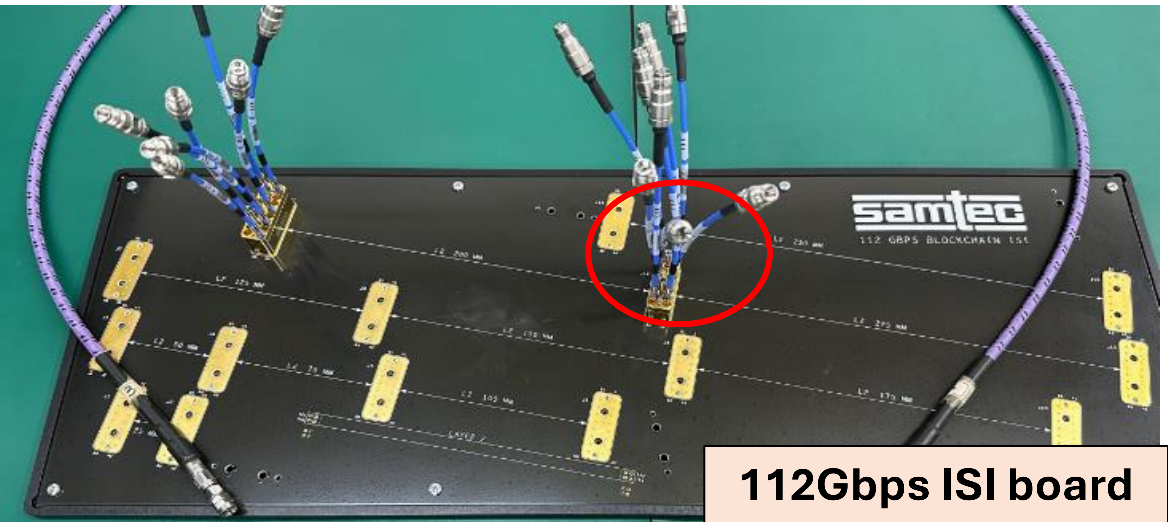
REMOVING INDIVIDUAL CABLES



Test Fixture & Test system







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