THE CHALLENGE FOR TESTING CABLE&CONNECTOR UNDER HIGH-SPEED DIGITAL INTERFACE

Sam Tsai
Application Engineer, Rohde & Schwarz Taiwan Ltd.

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Make ideas real

AGENDA

- PCIe evolution & demand for cable and connectors
- Challenges of high-speed interconnect
- Cable connector assembly specification
- R&S automated VNA solution

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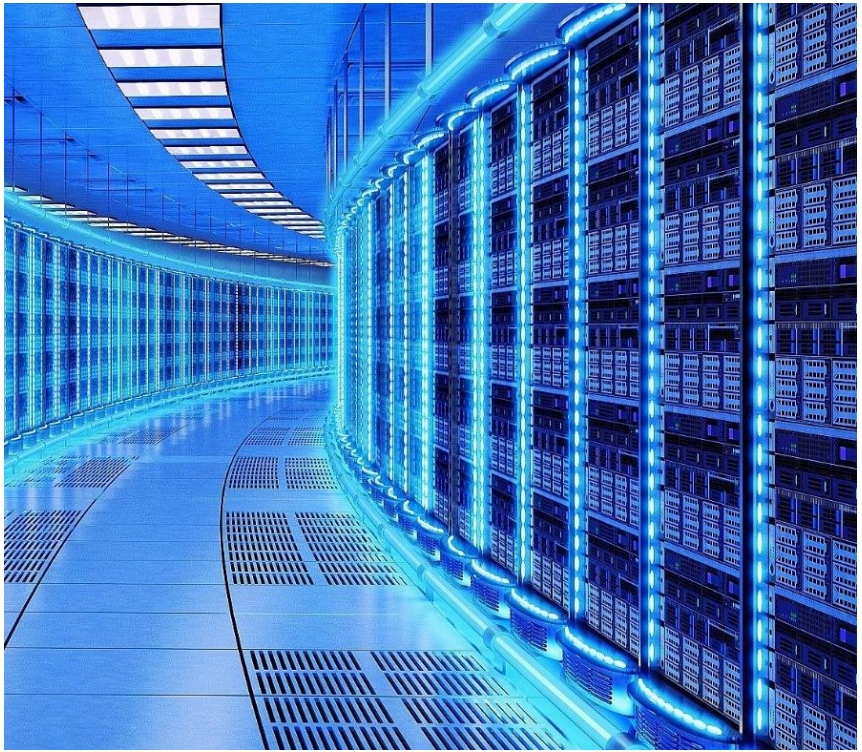
PCIE SPECIFICATION EVOLUTION

(GT/s x Lanes) / 8 = GB/s

PCIe Revision	Year	Transfer Rate	Encoding	Modulation	Lanes				
					x1	x2	x4	x8	x16
		GT/s			GB/s	GB/s	GB/s	GB/s	GB/s
1.0	2003	2.5	8b/10b	NRZ	0.25	0.50	1.0	2.0	4.0
2.0	2007	5.0	8b/10b	NRZ	0.50	1.0	2.0	4.0	8.0
3.0	2010	8.0	128b/130b	NRZ	0.98	1.97	3.94	7.88	15.8
4.0	2017	16.0	128b/130b	NRZ	1.97	3.94	7.88	15.8	31.5
5.0	2019	32.0	128b/130b	NRZ	3.94	7.88	15.8	31.5	63.0
6.0	2021	64.0	1b/1b	PAM4	8.0	16.0	32.0	64.0	128.0
7.0	tbd	128.0	1b/1b	PAM4	16.0	32.0	64.0	128.0	256.0

WHY ARE CABLES & CONNECTORS NEEDED?

- ► Dynamic Resource Requirements
  - Modern applications have dynamic resource requirements, addressed by modular computing architectures
- ► Key challenge
  - managing massive data transfer between computers and devices resources
- ► Growing Demand
  - high-speed cables & connectors supporting technologies like IEEE802.3 Ethernet, PCIe, USB, HDMI, DisplayPort…
- ► Widespread adoption
  - High-speed interconnects are widely used in various applications, including data center, consumer electronics, industrial IoT, 5G…



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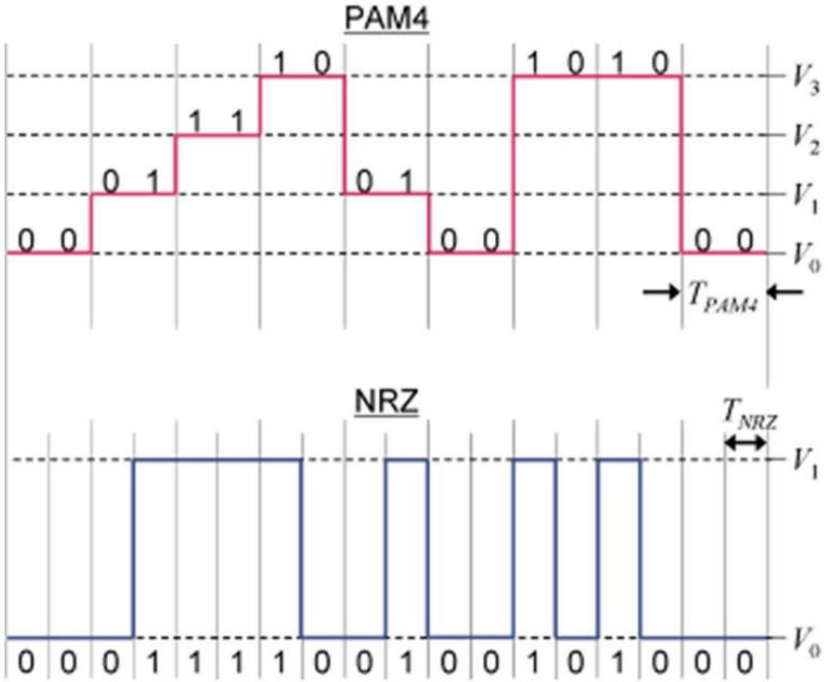
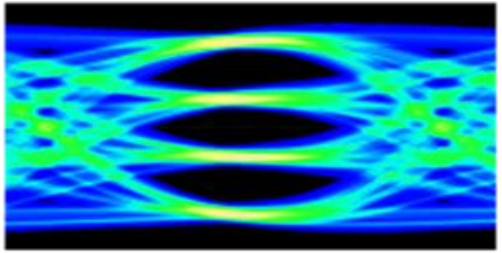
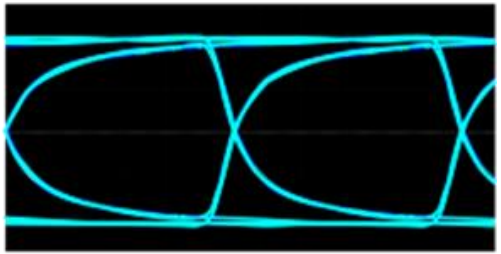
MORE SENSITIVE TO NOISE AND CROSSTALK

PAM4 VS. NRZ



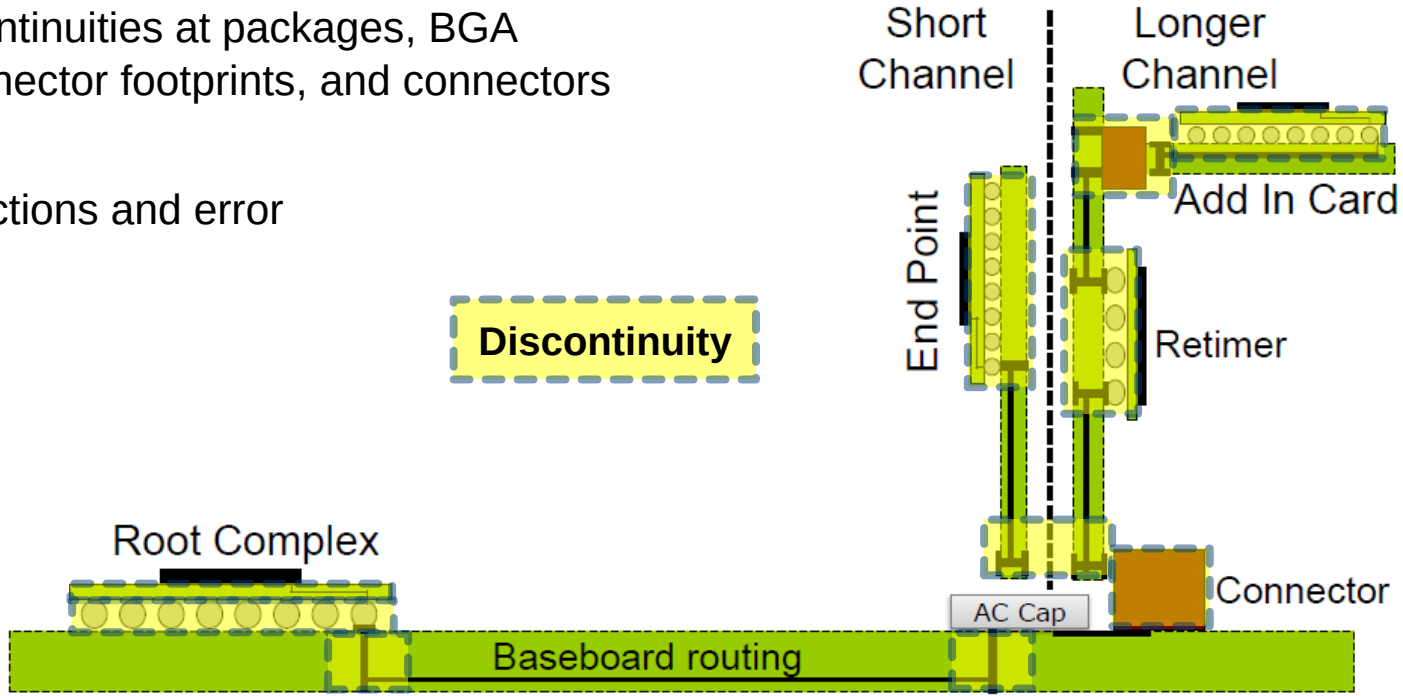




- 1/3 eye high
- SNR (signal to noise) drop by 9.5dB for PAM4
  20*log(1/3) = -9.54

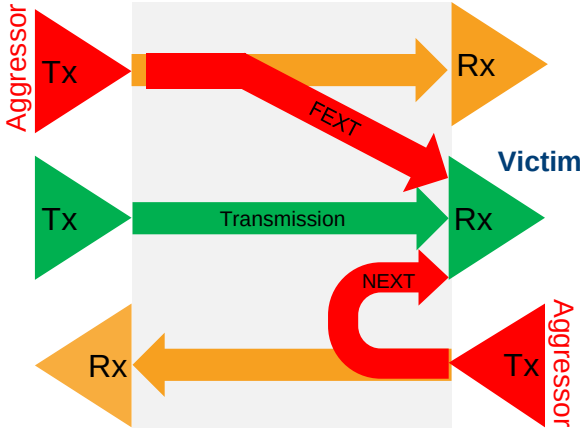
IMPEDANCE DISCONTINUITIES

- Impedance discontinuities at packages, BGA launch, vias, connector footprints, and connectors
- They cause reflections and error

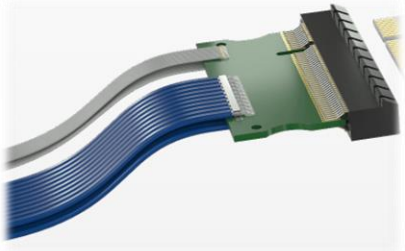


MULTIPLE AGGRESSORS AND HIGHER CROSSTALK

- Traditional cables are flat and have large form factor
- New connectors and cables are introduced being more compact and more dense
- Victim lanes have multiple significant aggressors



Type-C fixture



Riser cable

Reference: internet

MCIO cable

Amphenol

Array cable

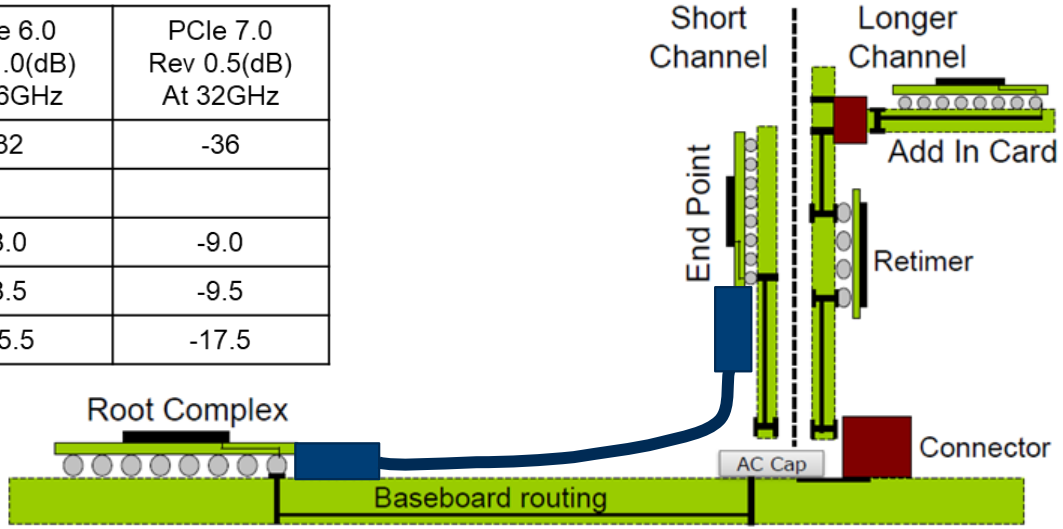
Samtec

TIGHTER PCB LOSS BUDGET IN PCIE

- Losses and frequency response of PCB material specified in standard

- PCB loss/inch requirement is below 1dB/inch at 16 GHz for gen 6.0

Loss Parameter	PCIe 5.0 Rev 1.0(dB) At 16GHz	PCIe 6.0 Rev 1.0(dB) At 16GHz	PCIe 7.0 Rev 0.5(dB) At 32GHz
Pad-to-Pad Loss	-36	-32	-36
Root Complex (RC)	-9.0	-8.0	-9.0
Add-in-Card (AIC)	-9.5	-8.5	-9.5
System	-17.5	-15.5	-17.5



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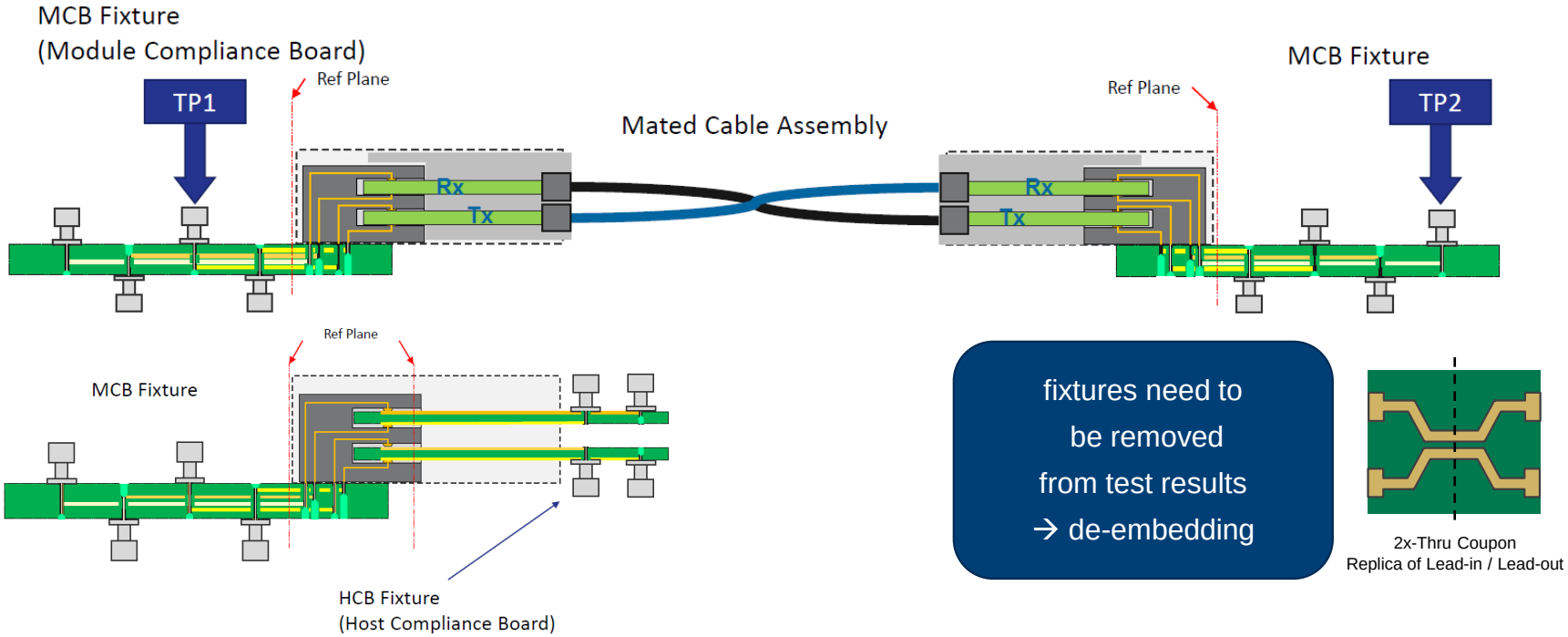
REFERENCE PLANE DEFINITION

EXAMPLE: PCIe 5.0 / 6.0 INTERNAL AND EXTERNAL CABLES

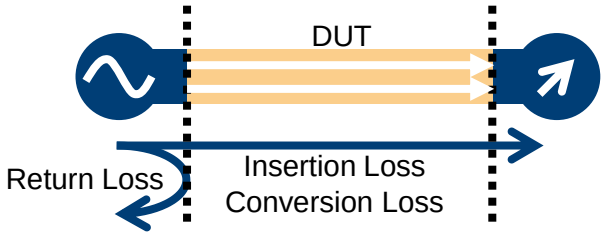


Source: PCI-SIG Electrical Work Group (EWG): PCIe 5.0/6.0 External Cable Specification

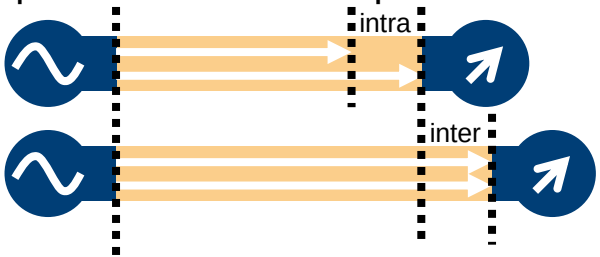
HIGH-SPEED INTERCONNECT TEST ITEMS

BASIC TEST ITEMS

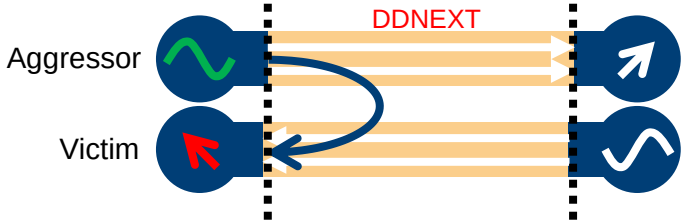
- Differential Insertion Loss (DDIL)
- Differential Return Loss (DDRL)
- Differential-to-Common Mode Conversion Loss



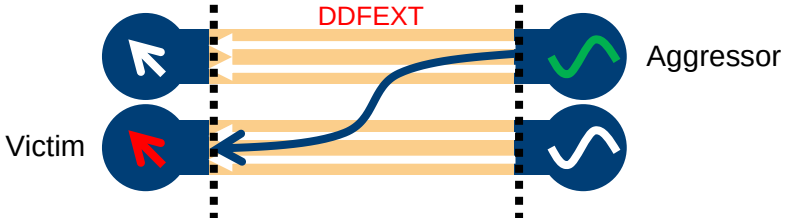
- Inter-pair Skew and Intra-pair Skew



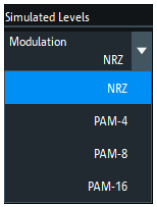
- Differential Near End Crosstalk (DDNEXT)

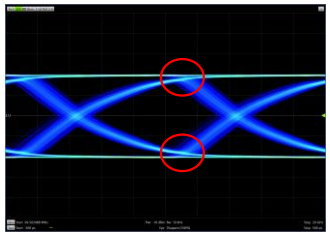


- Differential Far End Crosstalk (DDFEXT)



EYE DIAGRAM



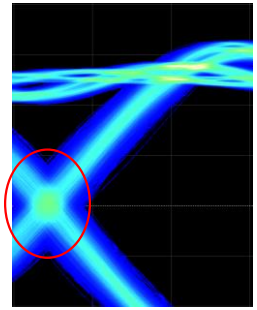


Emphasis

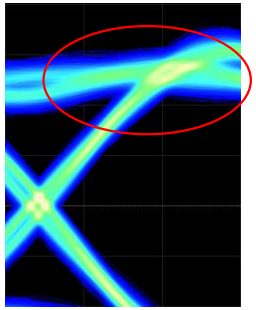
Generator

Channel

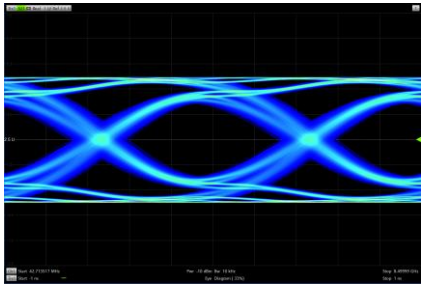
Receiver



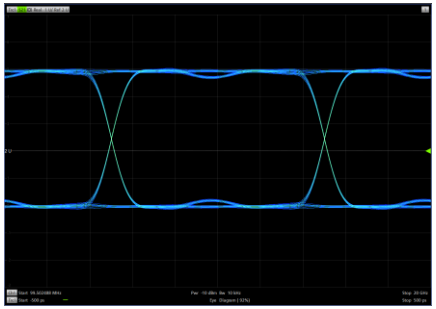
Jitter



Noise



Distorted Channel



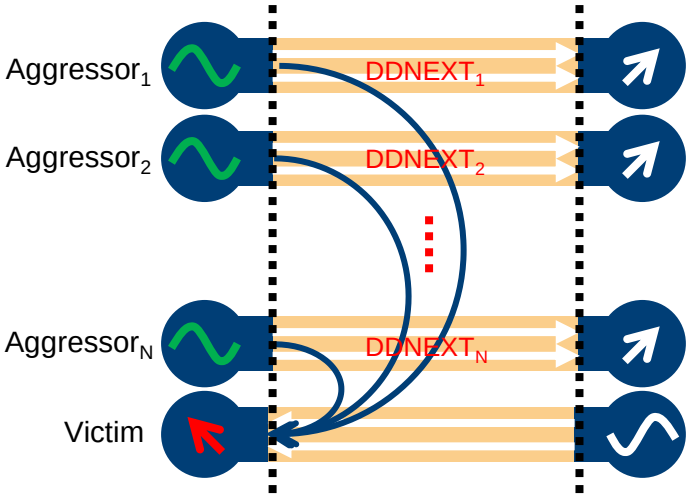
Equalization

HIGH-SPEED INTERCONNECT TEST ITEMS

ADVANCED TEST ITEMS

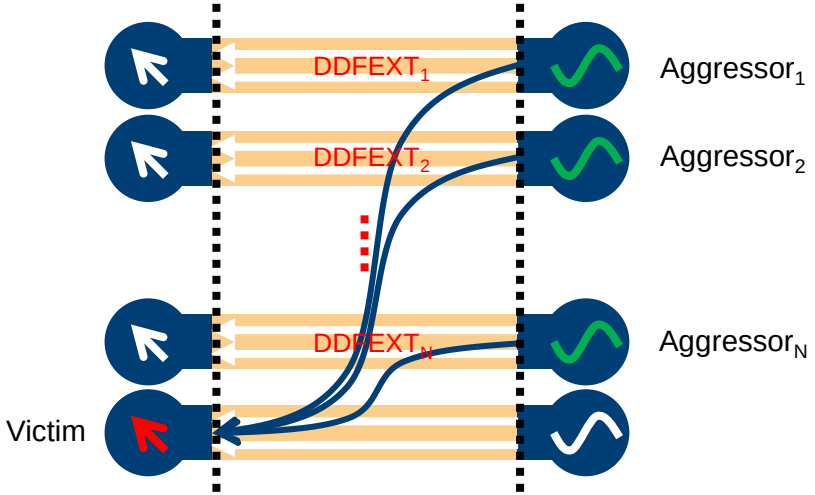
- Multiple Disturber Near End Crosstalk (MDNEXT)

Linear form: $MDNEXT(f) = \sum_{i=1}^{N} DDNEXT_i(f)$



- Multiple Disturber Far End Crosstalk (MDFEXT)

Linear form: $MDFEXT(f) = \sum_{i=1}^{N} DDFEXT_i(f)$

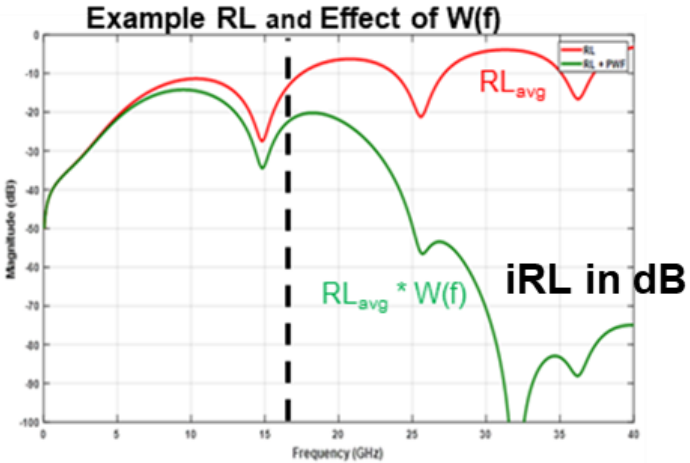


HIGH-SPEED INTERCONNECT TEST ITEMS

ADVANCED TEST ITEMS

iRL

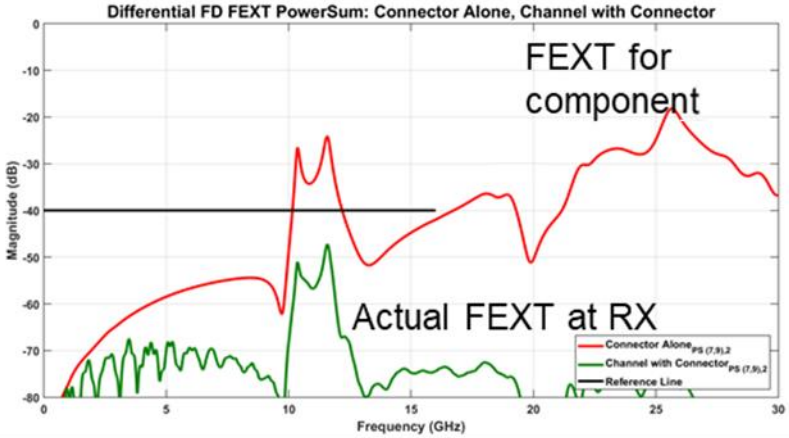
integrated Return Loss metric



courtesy of Samtec

ccICN

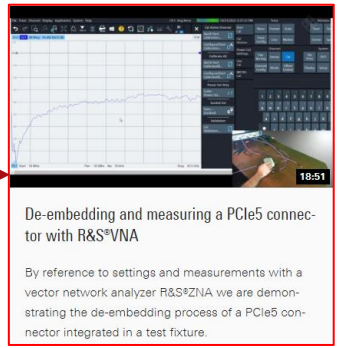
component contribution Integrated Crosstalk Noise



courtesy of Samtec

TEST FIXTURES DE EMBEDDING

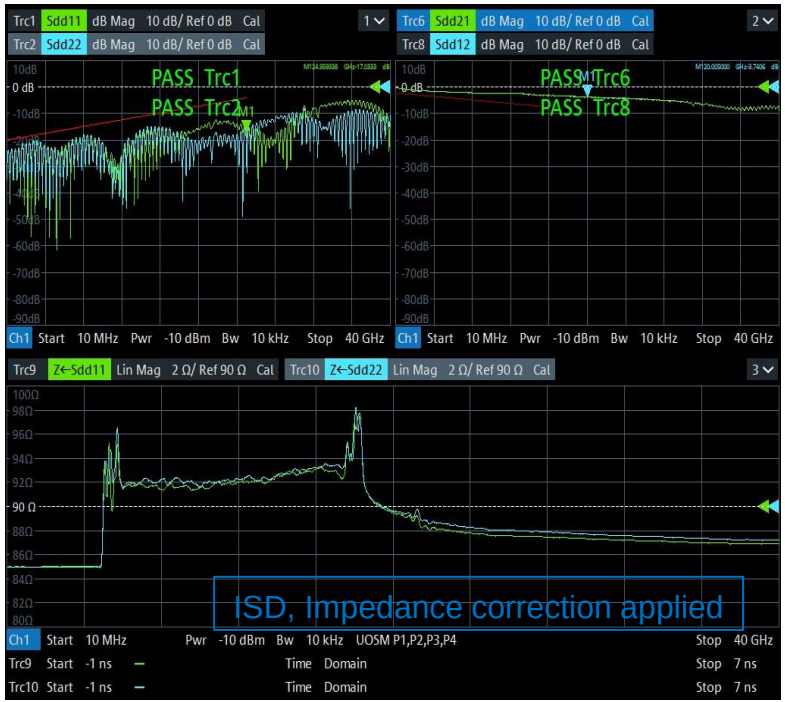
- Single Lane Fixture characterization recommended to be run up front by means of a single VNA K220.
- Test Fixtures may contain different 2x coupons due to different layers.
- At the moment best results being obtained by means of ISD with impedance correction.



De embedding video tutorial
„De-embedding and measuring PCIe5 connector with R&S VNA“
https://www.rohde-schwarz.com/de/produkte/messtechnik/netzwerkanalysatoren/rs-zna-vektornetzwerkanalysatoren_63493-551810.html

REF-224260-2.40-01 SI-FLY FLYOVER EVALUATION KIT

Measurements run on ZNB40 FW 3.60, single lane



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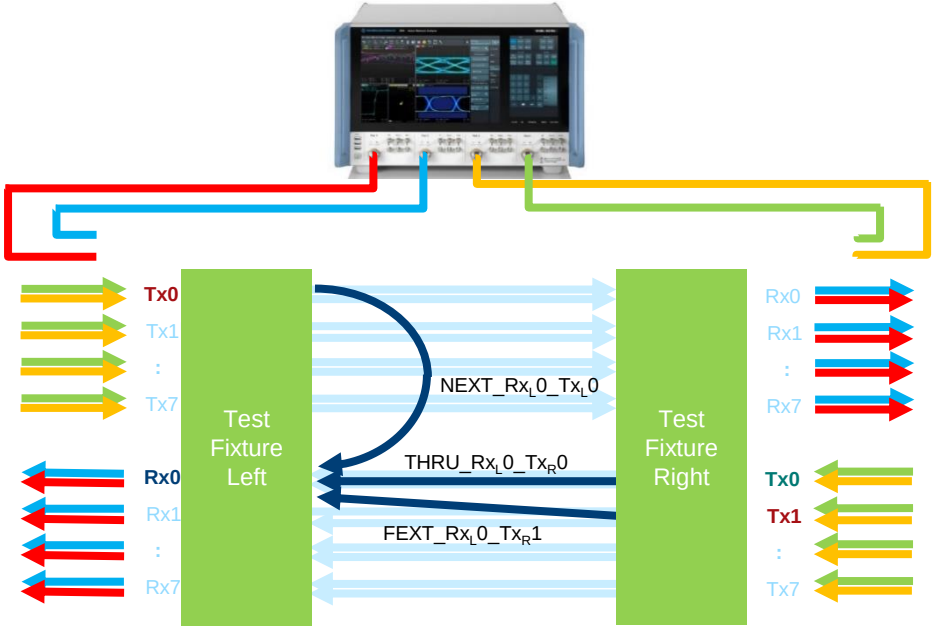
VERIFICATION OF CABLES AND CONNECTORS WITH VECTOR NETWORK ANALYZER

- **Required measurements:**
  - Insertion loss Sdd21
  - Return loss Sdd11 and Sdd22
  - Near-end crosstalk (NEXT)
  - Far-end crosstalk (FEXT)
  - Mode conversion (Scd21)
- **Postprocessing:**
  - Integrated return loss iRL
  - Power sum MDNEXT and $ccICN_{NEXT}$
  - Power sum MDFEXT and $ccICN_{FEXT}$
  - Intra-pair skew: EIPS
  - Inter-pair skew (lane-to-lane)
  - Channel operation margin COM
  - etc …

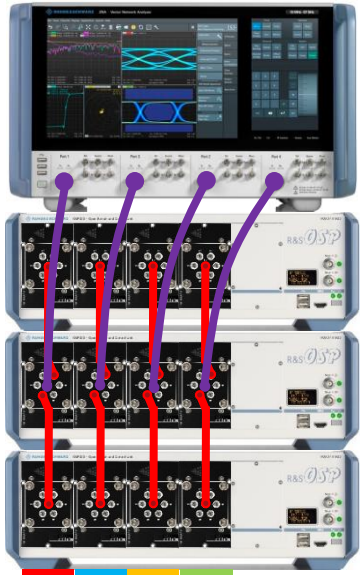
Testing with 4 port VNA requires multiple 4-port measurements



Example PCIe x8 cable

VERIFICATION OF INTERCONNECT
MEASUREMENT CONSIDERATIONS

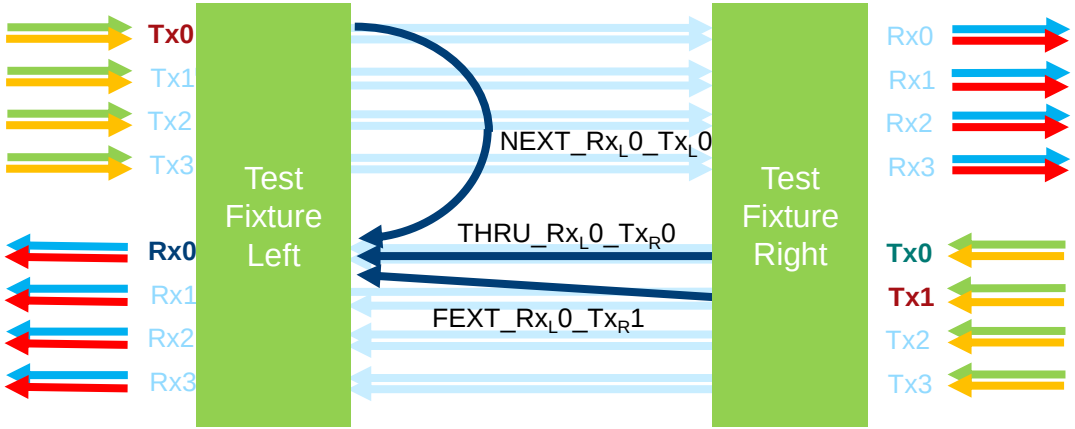
Measurements:
automation with switch matrix:



example for PCIe x8

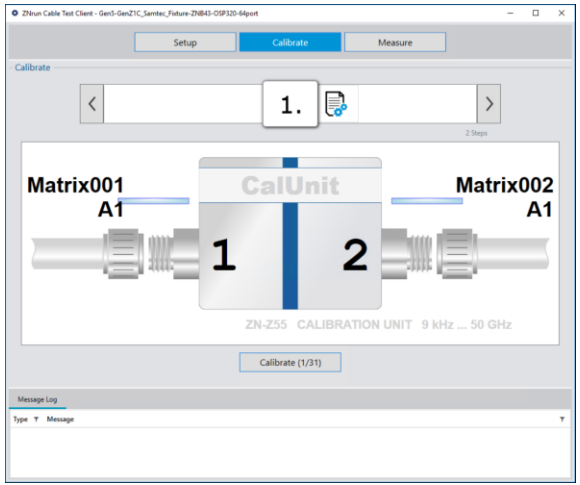
total test port = 64 ports

	x4	x8	x16
number of lanes (Tx + Rx)	4 Tx + 4 Rx	8 Tx + 8 Rx	16 Tx + 16 Rx
number of ports for full testing (all lanes and all crosstalk combinations)	32	64	128
number of 4-port measurements for full testing (all lanes and all crosstalk combinations)	8 x THRU 4 x 4 = 16 x NEXT_L 4 x 4 = 16 x NEXT_R 3 x 4 = 12 x FEXT_L 3 x 4 = 12 x FEXT_R total: 64 4-port meas.	16 x THRU 8 x 8 = 64 x NEXT_L 8 x 8 = 64 x NEXT_R 7 x 8 = 56 x FEXT_L 7 x 8 = 56 x FEXT_R total: 256 4-port meas.	32 x THRU 16 x 16 = 256 x NEXT_L 16 x 16 = 256 x NEXT_R 15 x 16 = 240 x FEXT_L 15 x 16 = 240 x FEXT_R total: 1024 4-port meas.



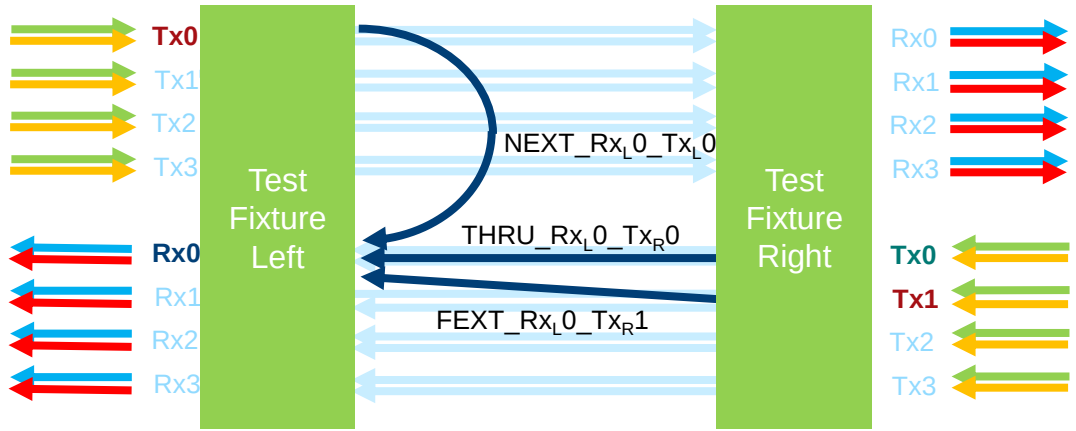
VERIFICATION OF INTERCONNECT
CALIBRATION CONSIDERATIONS

Calibration:
automation of calibration
example for PCIe x4 w. R&S ZNrun



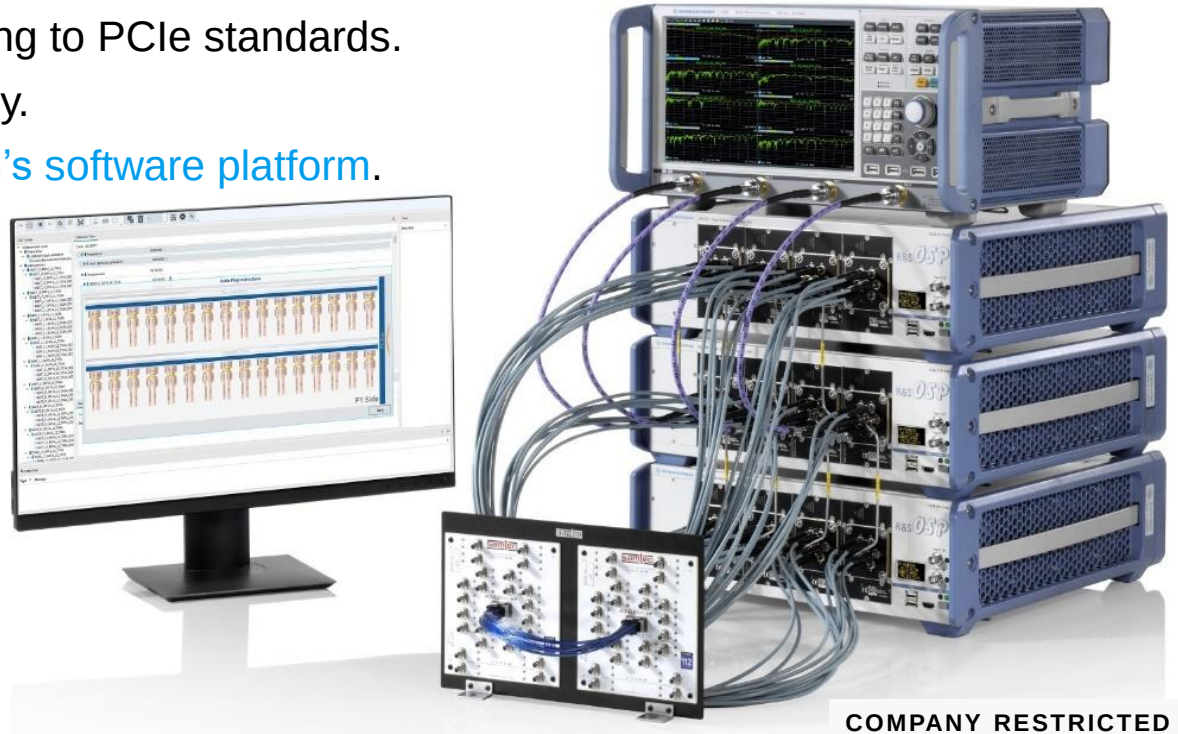
Calibration algorithm patent filed

	x4	x8	x16
number of lanes (Tx + Rx)	4 Tx + 4 Rx	8 Tx + 8 Rx	16 Tx + 16 Rx
number of ports for full testing (all lanes and all crosstalk combinations)	32	64	128
number of 4-port measurements for full testing (all lanes and all crosstalk combinations)	64 4-port groups:	256 4-port groups:	1024 4-port groups:
standard calibration (3 connections per 4-port)	64 x 3 = 192	256 x 3 = 768	1024 x 3 = 3072
optimized calibration	**31**	**63**	**127**



ROHDE & SCHWARZ AUTOMATED TEST SOLUTION

- Victim-based methodology with unique efficient calibration algorithm.
- Post-processing is done according to PCIe standards.
- Report is generated automatically.
- Customized operation with Allion's software platform.



Thanks for your time!

RSTW Application Engineer
Sam Tsai

sam.tsai@rohde-schwarz.com
Phone: (02) 2657 2668 ext. 317
Mobile: 0927 578 080

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