ANALYZING POWER DESIGNS FOR HIGH-SPEED SOCS WITH MULTI-PHASE BUCK CONVERTERS

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Make ideas real

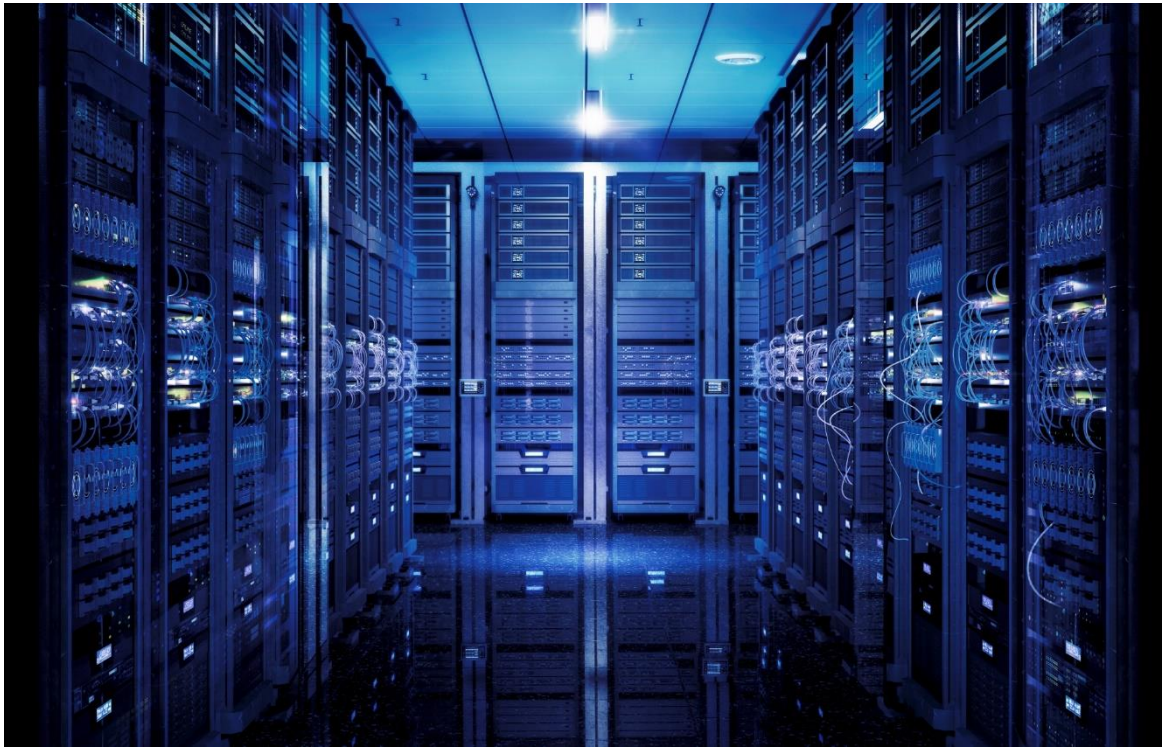
TEXAS INSTRUMENTS

SOC POWER DESIGNS W. MULTI-PHASE BUCK CONVERTERS:

AGENDA:

- INDUSTRY TRENDS
- HOW THEY WORK
- BENEFITS
- IMPLEMENTATIONS
- PERFORMANCE REQUIREMENTS
- VALIDATION AND DEBUG
- TESTING ASPECTS

INCREASING POWER CONSUMPTION OF HIGH-SPEED SOCS: BIG DATA AND ARTIFICIAL INTELLIGENCE



Increasing requirements regarding

- ► processing power
- ► I/O data rates
- ► power efficiency

Decreasing supply voltages with tighter tolerances

- ► fast response on load transients
- ► low ripple / noise

Increasing supply currents

INCREASING POWER CONSUMPTION OF HIGH-SPEED SOCS: VEHICLE ARCHITECTURE AND AUTONOMOUS DRIVING

Increase of complexity inside the various functional domains

- ADAS
- Infotainment
- Powertrain
- …

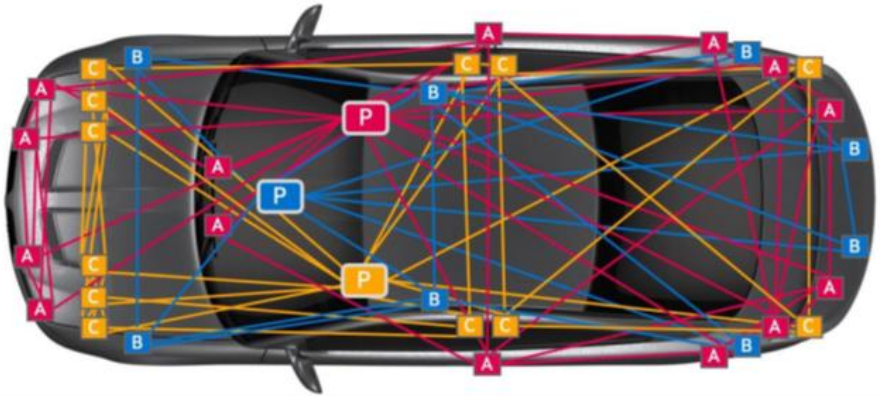
Shift of electronic vehicle architecture

- from decentralized electronic architecture (multiple, distributed ECUs)
- towards domain-based architecture with powerful domain controllers and gateways
- towards centralized architecture with powerful zone controllers and high-speed central computing

INCREASING POWER CONSUMPTION OF HIGH-SPEED SOCS: VEHICLE ARCHITECTURE AND AUTONOMOUS DRIVING

Domain architecture

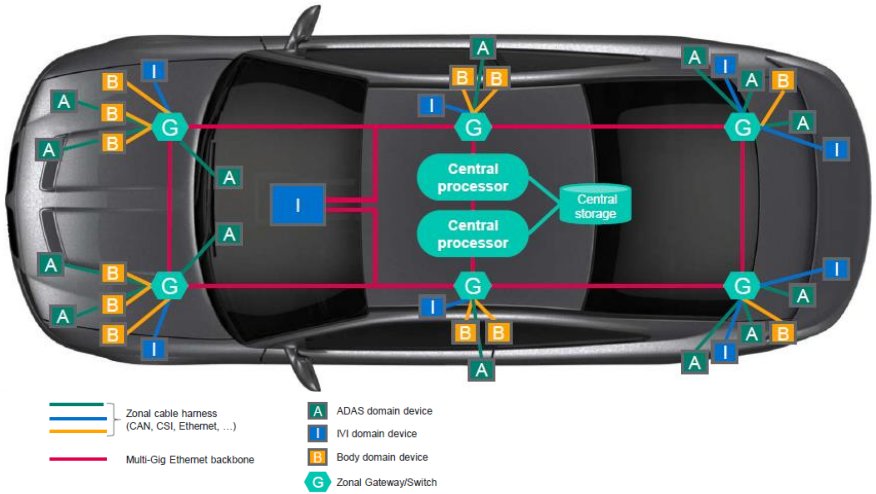
- Central domain controller/high performance computer
- Ability to handle more complex functions
- Consolidation of functions (cost optimization)
- But: cable harness is rigid and expensive



Source: Marvell Automotive Ethernet Congress 2022

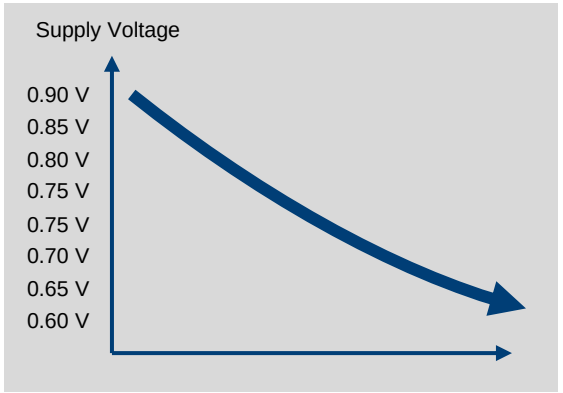
Zonal architecture

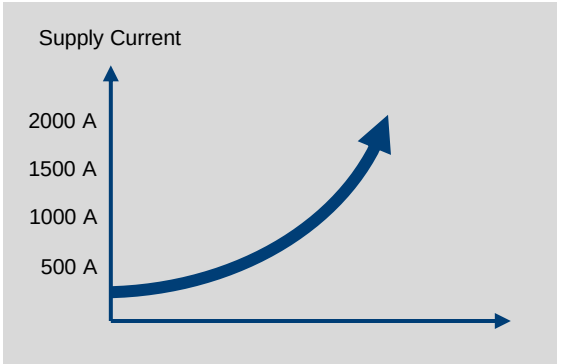
- Local ethernet gateway per zone
- Ultra high-speed secured backbone between zones
- Centralized SW
- Central computing & storage



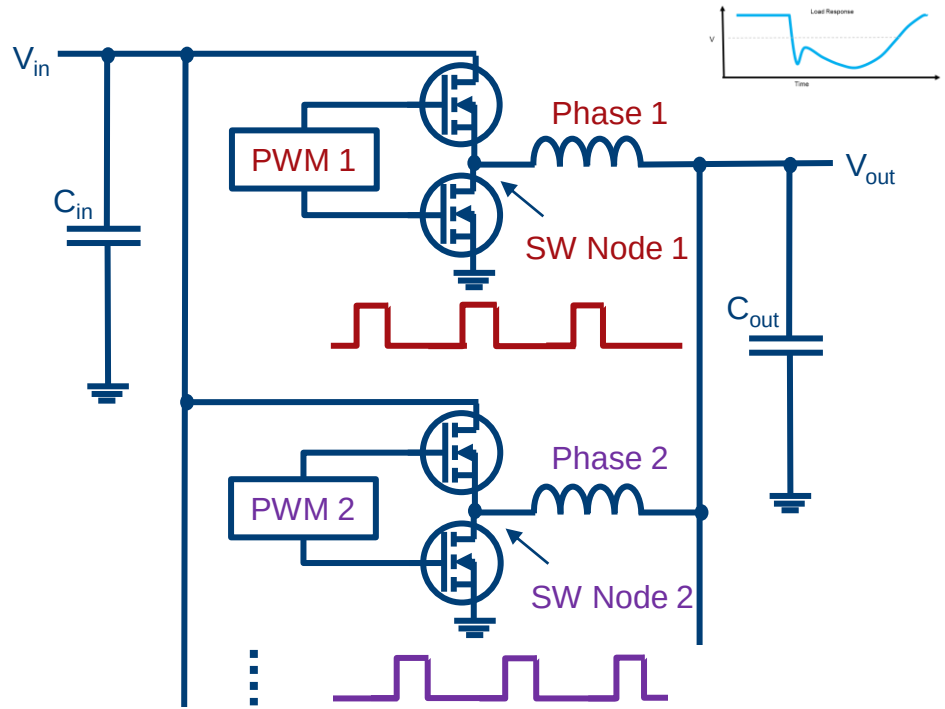
POWER MANAGEMENT FOR SOCS AND RFSOCS: INDUSTRY TRENDS AND CHALLENGES

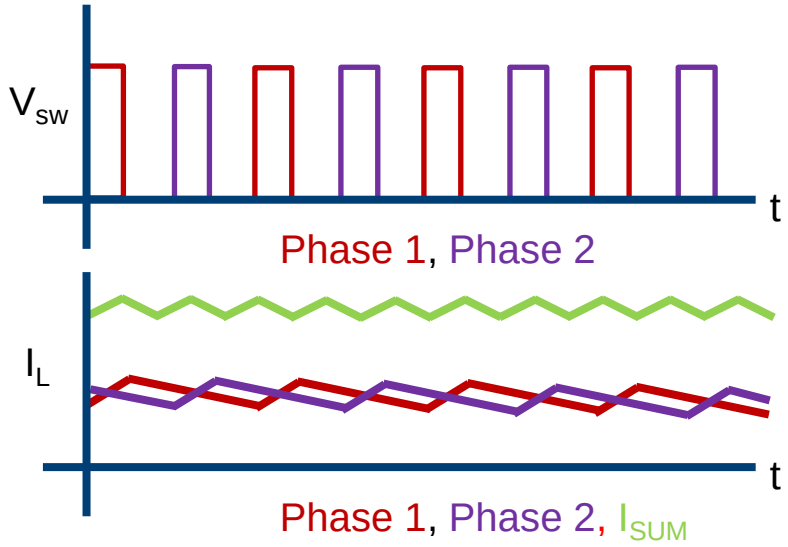
- Growing demand of high-performance SoCs and RFSoCs in
  - data centers
  - fixed and wireless network infrastructure
  - automotive
  - aerospace / defense
- Power delivery solutions need to provide a high number of low-voltage power rails with
  - precise sequencing for power-up / power-down
  - high currents on core power rails
  - fast response on load transients, low ripple / noise
  - high efficiency
- Increasing use of multi-phase buck converters to supply core power rails





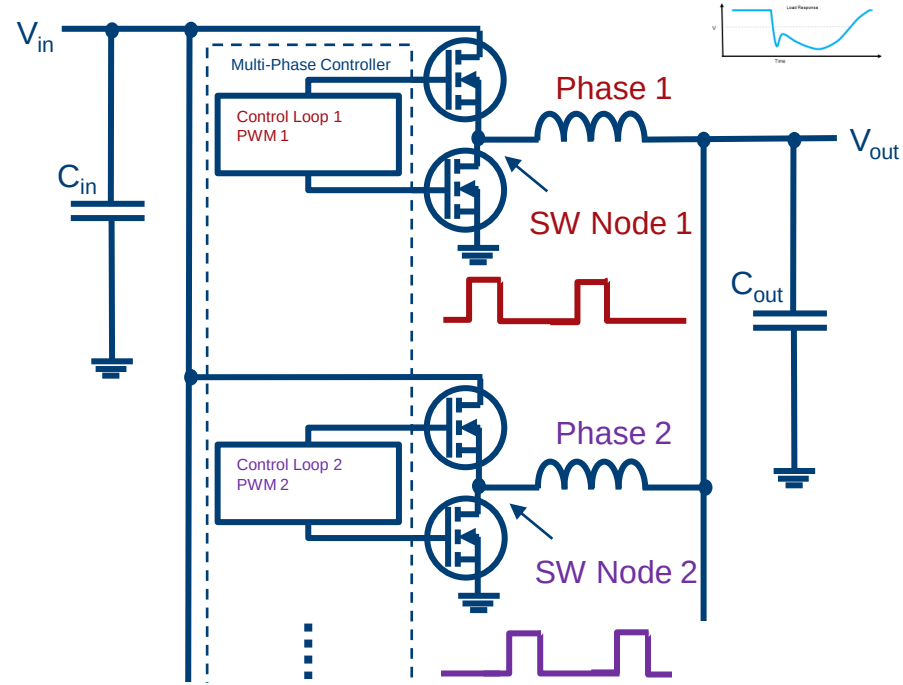
SOC POWER DESIGNS W. MULTI-PHASE BUCK CONVERTERS: FUNCTIONAL PRINCIPLE AND BENEFITS



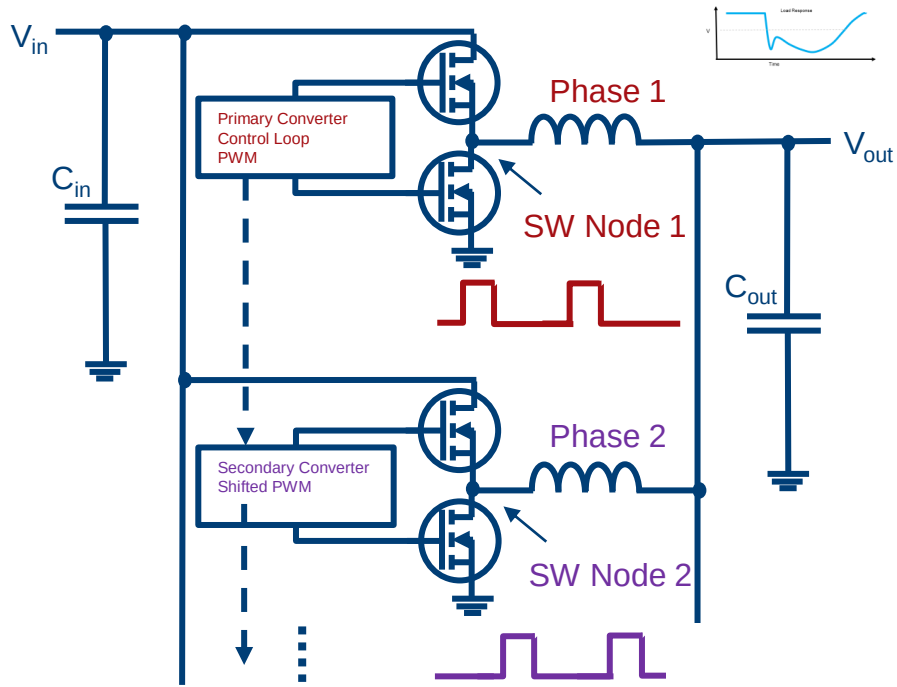


SOC POWER DESIGNS W. MULTI-PHASE BUCK CONVERTERS: FUNCTIONAL PRINCIPLE AND BENEFITS

Design w. Multi-Phase Controller



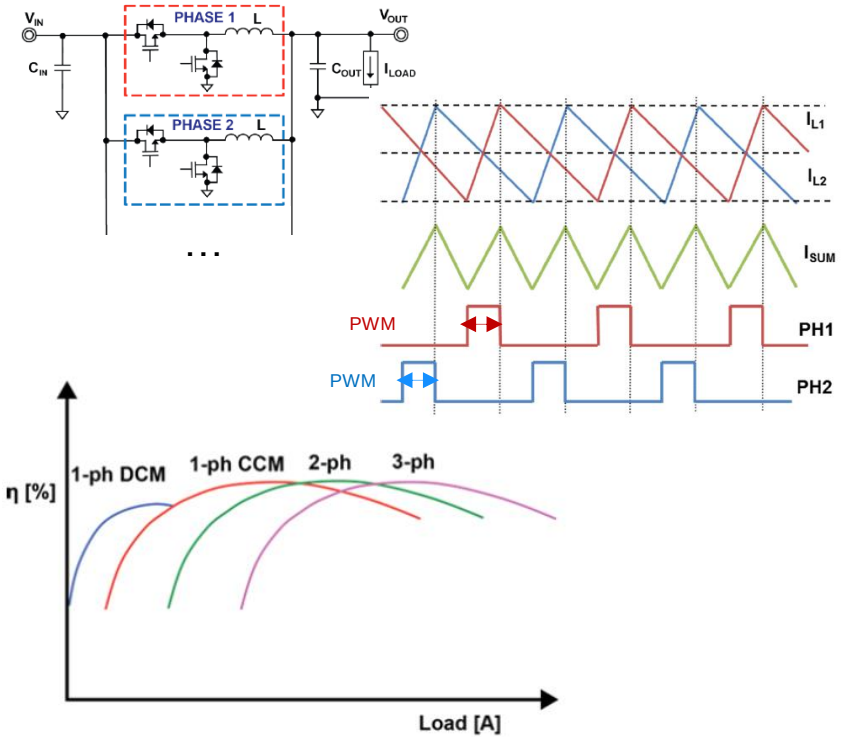
Stacked Design w. Primary and Secondary Converters



SOC POWER DESIGNS W. MULTI-PHASE BUCK CONVERTERS: FUNCTIONAL PRINCIPLE AND BENEFITS

Benefits:

- reduced voltage ripple (input and output)
  → reduction of input and output capacitance
- reduced thermal load and improved efficiency in multi-phase mode for high currents
- flexible phase management to optimize efficiency across a wide range of loads:
  - enabling / disabling of phases
- improved load transient response time by reaction at next phase after load step and active phase management:
  - load step up: controller overlaps phases
  - load step down: controller turns off phases



Source: Texas Instruments
Application Report: Multiphase Buck Design From Start to Finish (Part 1)

SOC POWER DESIGNS W. MULTI-PHASE BUCK CONVERTERS:

AGENDA:

- INDUSTRY TRENDS
- HOW THEY WORK
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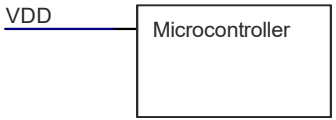
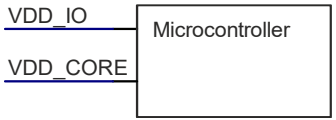
PROCESSOR POWER SUPPLIES

One supply rail
5V or 3.3V
<1A supply current, DC

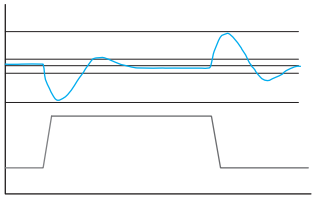


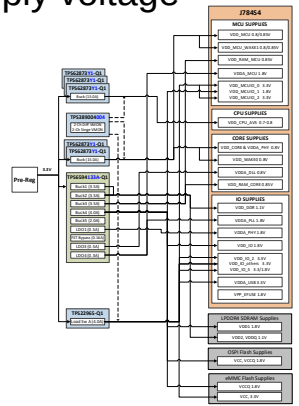
Separate supply rails
for core and I/O
I/O voltage 3.3V or 1.8V
Core voltage 1.8V or below
<10A core supply current
Fast load transients



Multiple supply rails
for different functional blocks

Core voltage <1V
>10A core supply current
Fast load transients
Dynamically adjust supply voltage



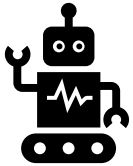


LEVELS OF DRIVING AUTOMATION

Level 0	Level 1	Level 2	Level 3	Level 4	Level 5
No driving automation	Driver assistance	Partial driving automation	Conditional driving automation	High driving automation Some conditions	
	Feet off	Hands off	Eyes off	Attention off	

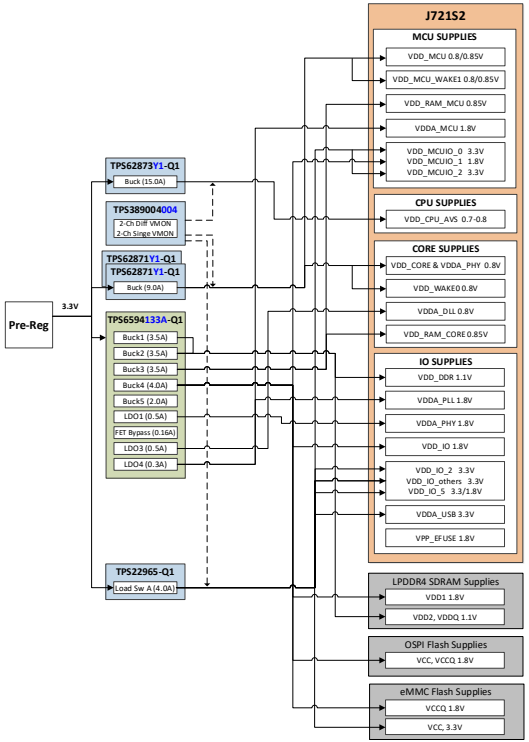


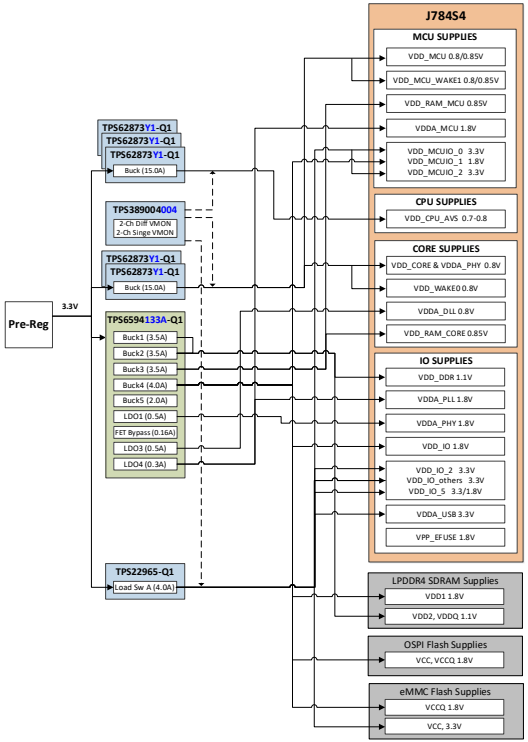




More computation, higher current demand

SOC POWER STRUCTURE - EXAMPLES

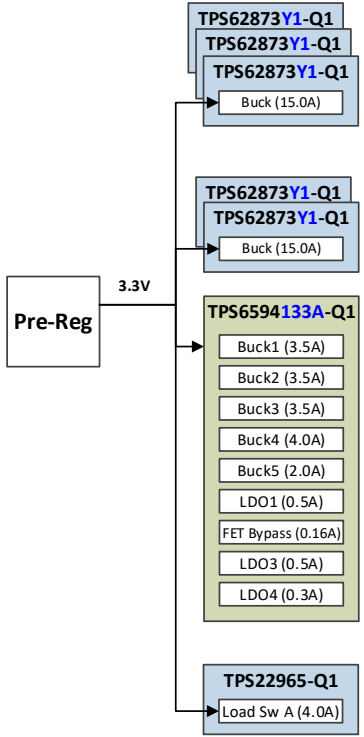




DCDC CONVERTERS IN THE POWER TREE

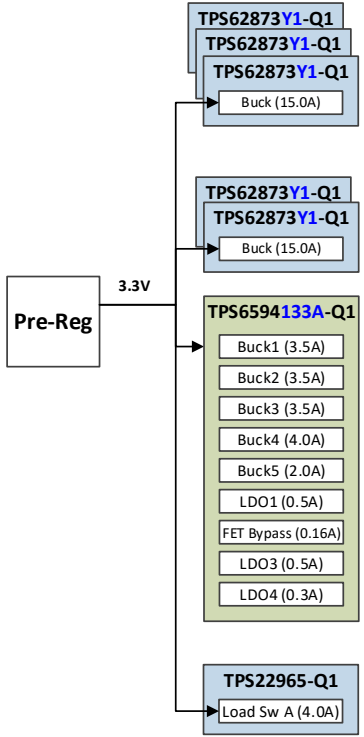
- High power section
  - Low voltage core supply
  - High load current variations
  - Dynamically adjust output voltage

- Lower power section
  - Infrastructure, housekeeping, safety
  - Power up and down sequencing
  - Constant power consumption, on or off



PREREGULATOR FOR HIGH POWER SECTION

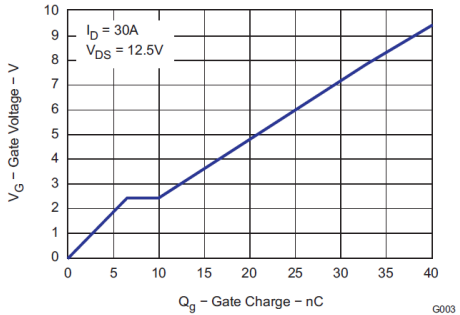
- Filtering towards infrastructure
- Efficiency improvements
- Higher switching frequency

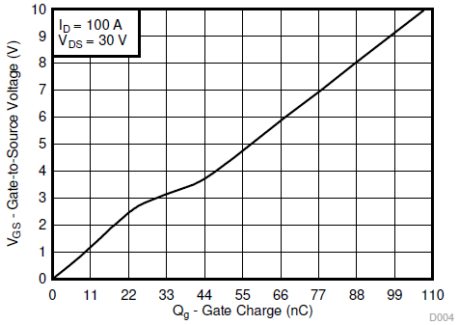


PREREGULATOR FOR HIGH POWER SECTION

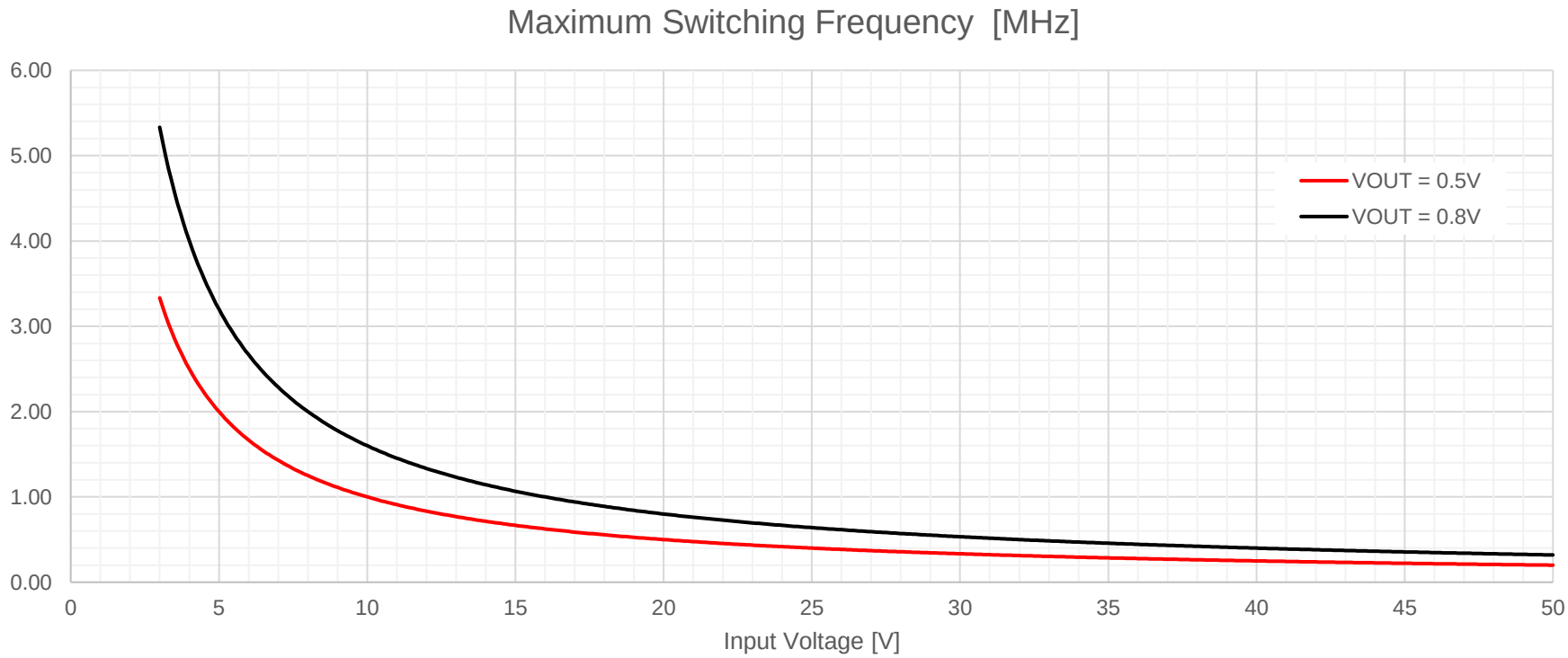
V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	18		nC
Q_{gd}	Gate Charge Gate to Drain	3.5		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3 V	2.1	mΩ
		V_{GS} = 4.5 V	1.7	mΩ
		V_{GS} = 8 V	1.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.1		V

V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10V)	108		nC
Q_{gd}	Gate Charge Gate-to-Drain	14		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5V	1.7	mΩ
		V_{GS} = 10V	1.3	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V



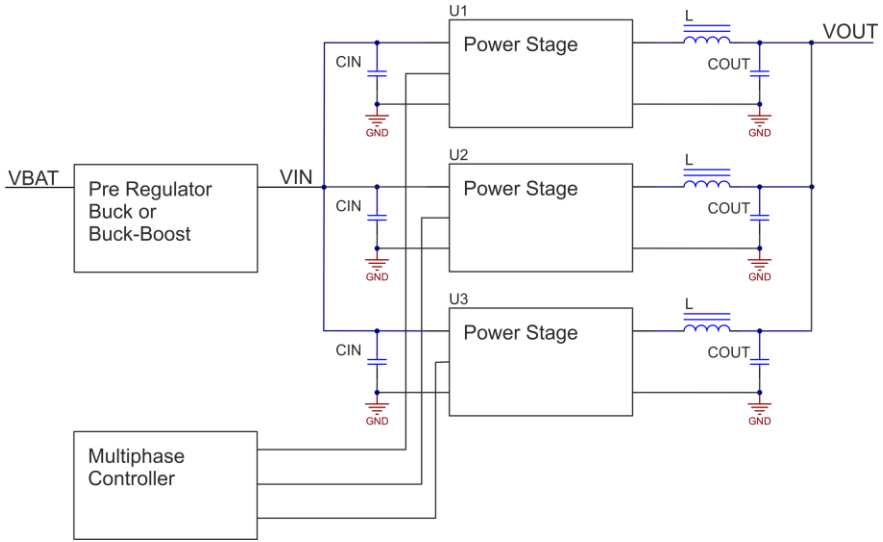


SWITCHING FREQUENCY

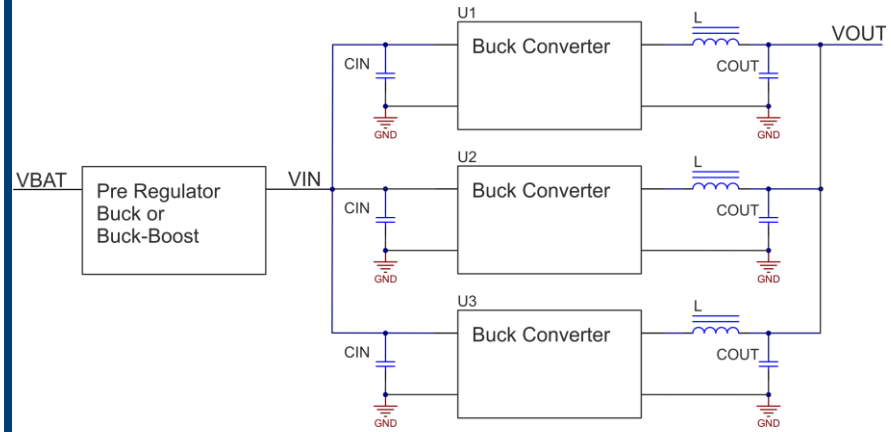


COMPARISON - INPUT TO CORE

Controller based VR power tree

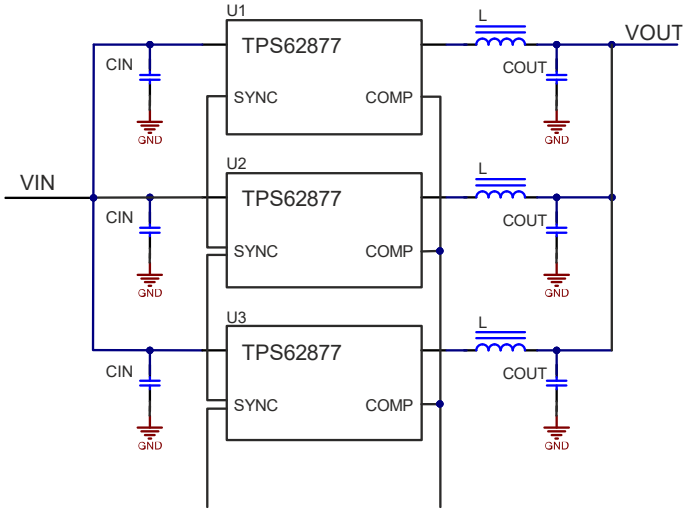


Converter based VR power tree

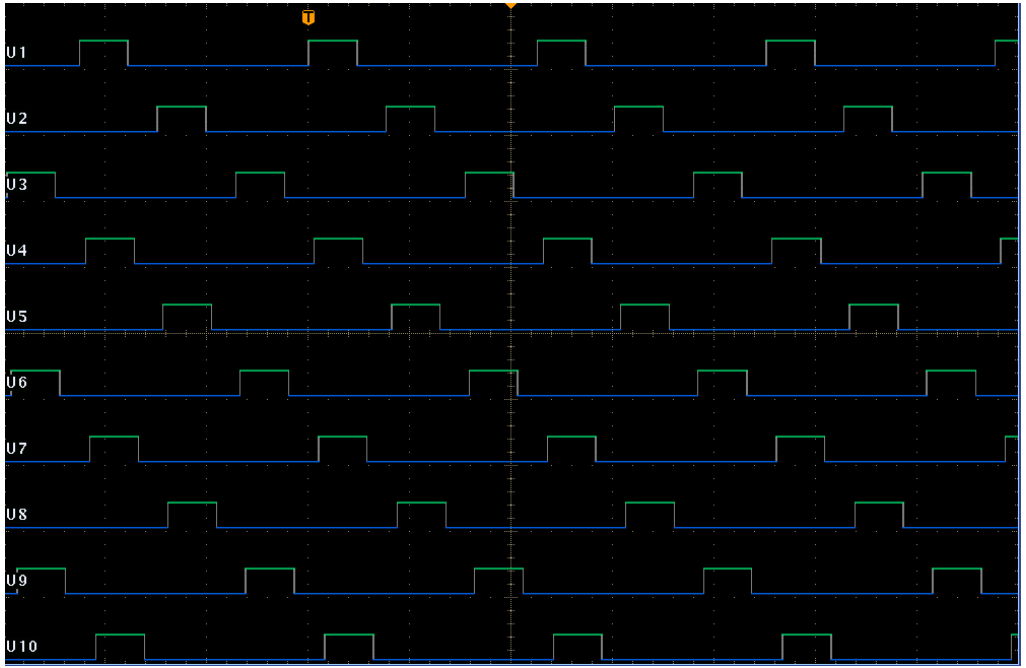


EXAMPLE

- Supply voltage range 3V to 5V
- Output voltage 0.8V, +/-3%
- Maximum continuous output current 300A
- 10 TPS62877 converters in parallel
  - Synchronized, interleaved operation
  - Primary device senses output differentially
  - Shared COMP signal for current sharing

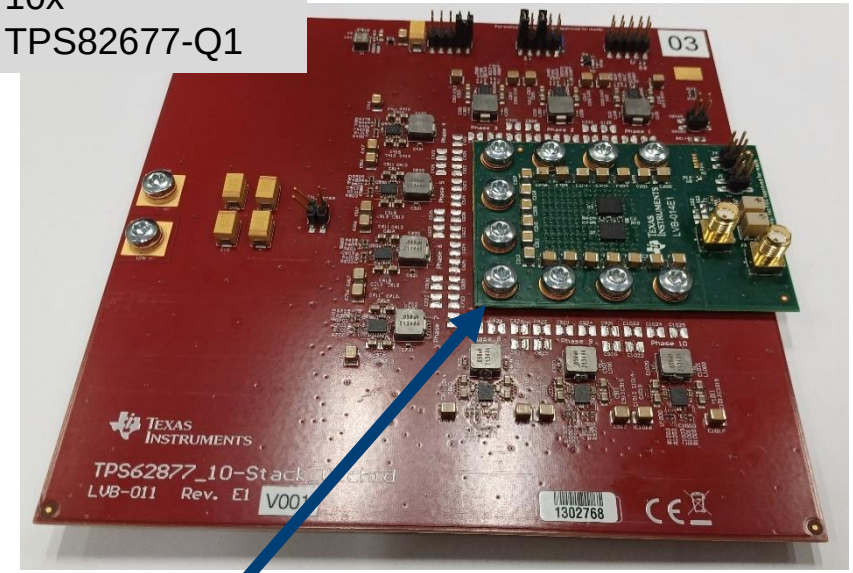


PHASE SHIFTED SYNCHRONIZATION



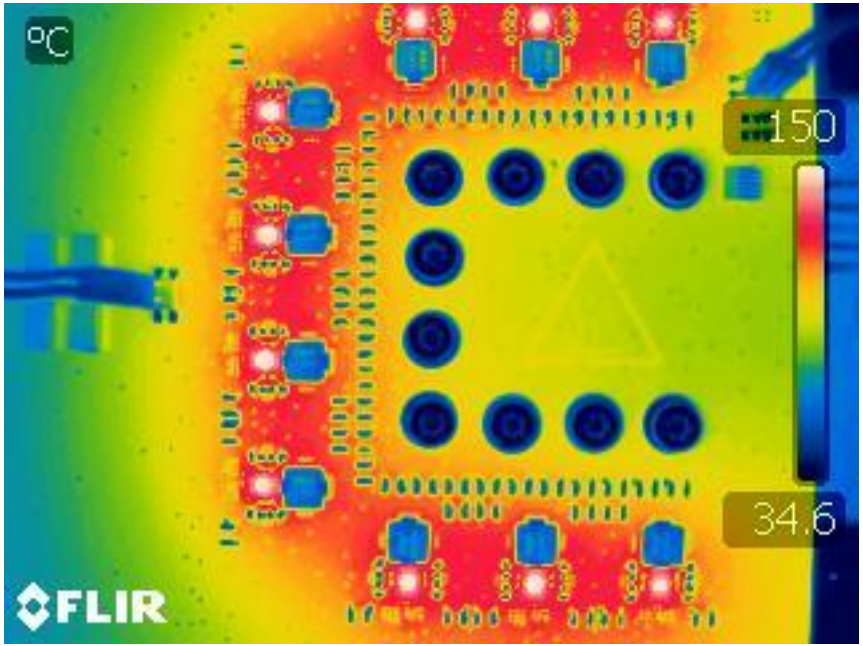
HARDWARE TEST RESULTS

10x
TPS82677-Q1

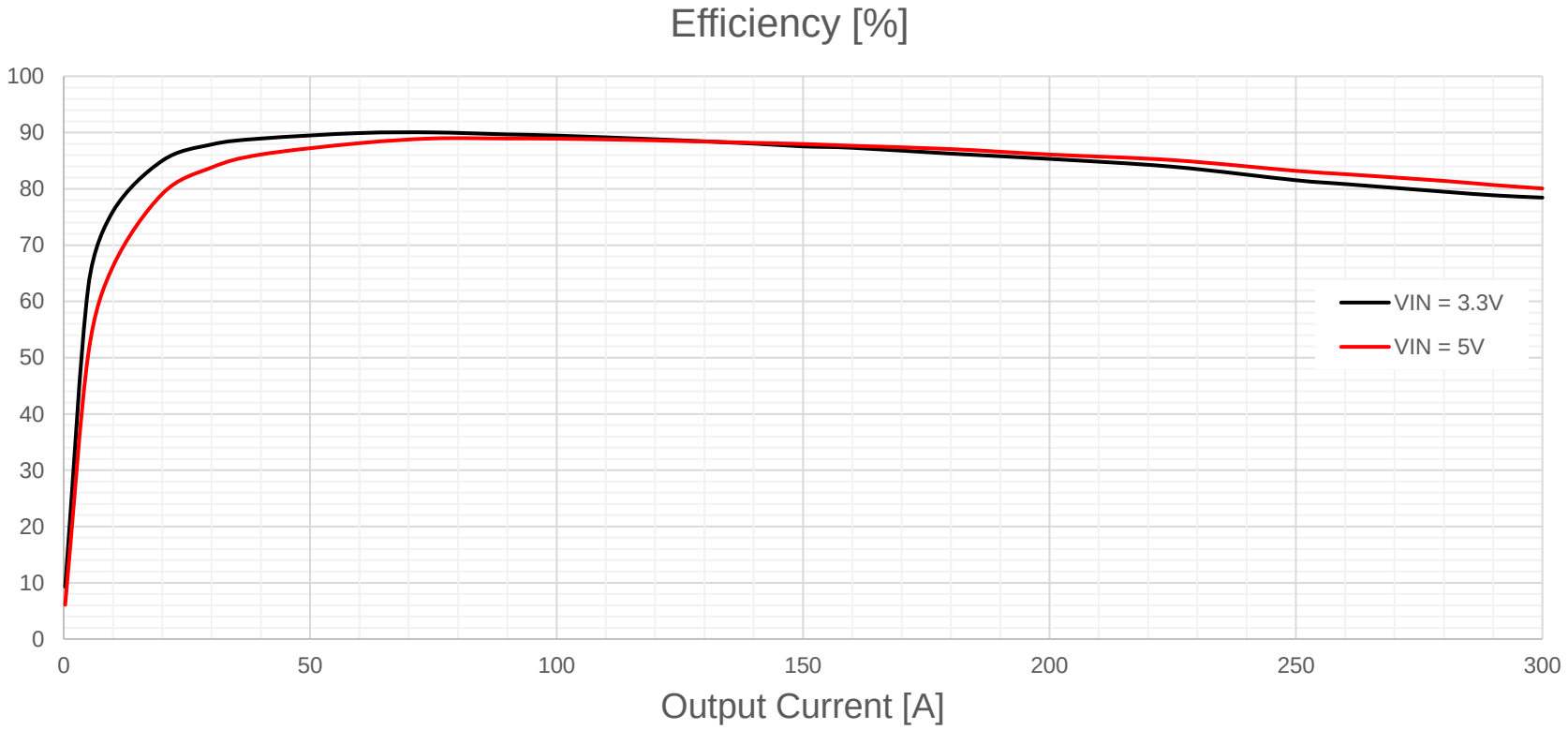


Load transient test board

Thermal image (3.3V in, 300A out)



HARDWARE TEST RESULTS



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MEASUREMENT CHALLENGES

- ► Efficiency
- ► Load step response
- ► Power integrity
- ► Bus control signal response
- ► Feedback loop gain

→ R&S MXO 5 Oscilloscope

MXO5 KEY BENEFITS FOR POWER CONVERTER ANALYSIS

8 analog
+16 digital channels

12 -bit ADC 18-bit HD

500 Mpts memory /ch

Digital trigger

> 45 k FFT / sec

Standard MSO

R&S® PROBES FOR YOUR APPLICATION

Passive

- General purpose
- Extensive accessories
- Up to 700MHz

Power rail

- High sensitivity
- ±60V offset
- 2GHz or 4GHz

EMC near field

- E-field probes
- B-field probes
- High spatial resolution

Differential

- High input impedance
- Low input capacity
- Up to 4.5GHz

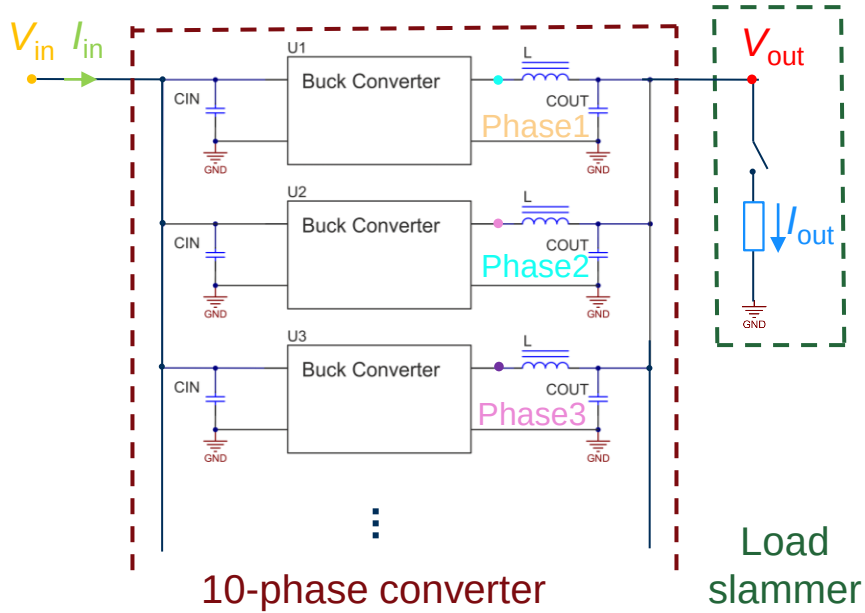
Current

- Non-intrusive
- DC to 120MHz
- Up to 2kA

Logic

- 16 additional digital channels
- 5GSa/s
- Powerful trigger

MEASUREMENT SETUP



Load slammer:

- 5mΩ load
- 15µs pulses with 200 Hz
- Current measurement across load

Measurement points:

- Input voltage V_{in} & current I_{in}
- Output voltage V_{out} & current I_{out}
- Switch nodes of phase 1, phase 2, phase 3 and phase 4
- Digital channels: phase 5 to 10, I^2C signal

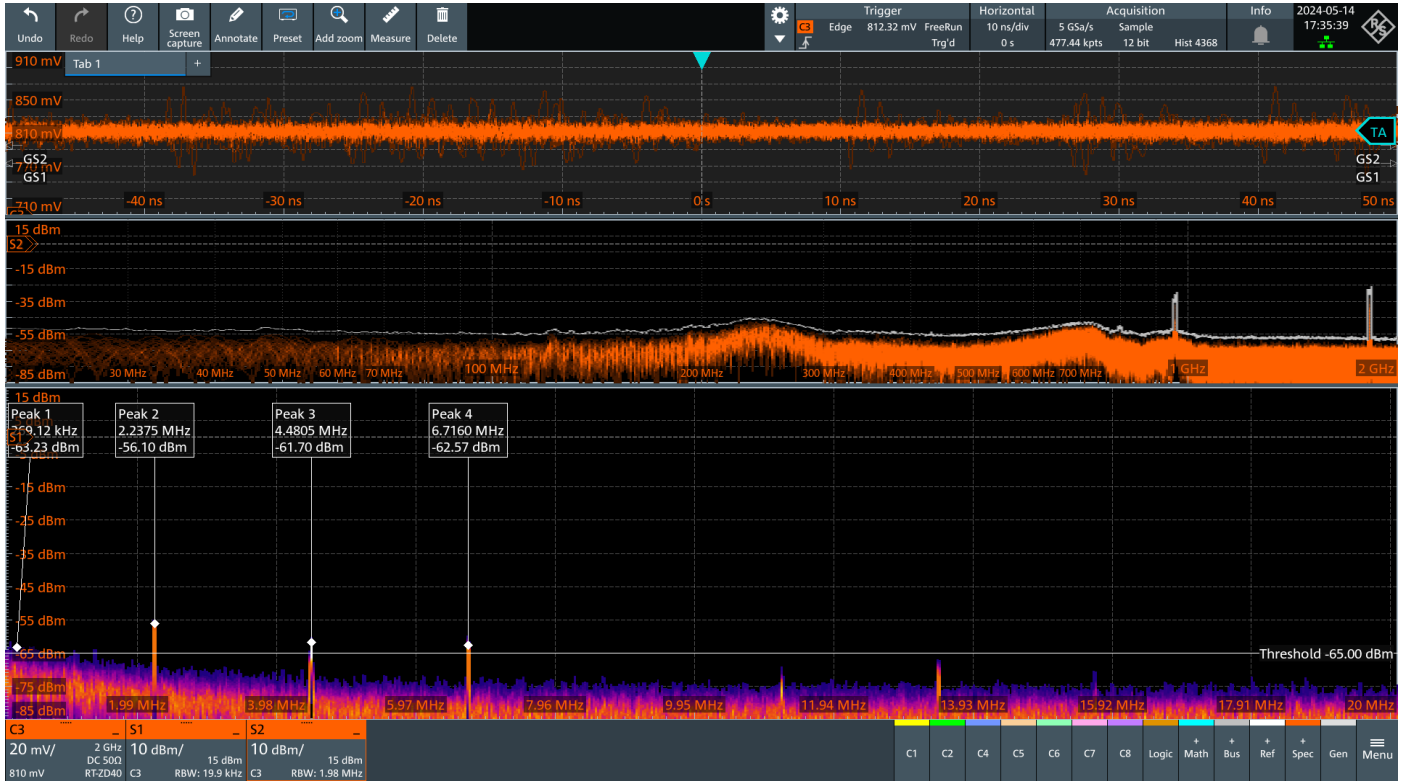
EFFICIENCY


Undo
Redo
Help
Screen capture
Annotate
Preset
Add zoom
Measure
Delete
Trigger
Edge
801.6 mV
Auto
Trg'd
Horizontal
2 ms/div
0 s
Acquisition
500 MSa/s
Sample
10 Mpts
16 bit
Hist 79
Info
2024-05-14
16:34:09
Tab 1
3.6 V
3.5 V
3.4 V
3.3 V
3.2 V
3.1 V
3 V
2.9 V
2.8 V
2.7 V
-8 ms
-6 ms
-4 ms
-2 ms
0 s
2 ms
4 ms
6 ms
8 ms
10 ms
200 V
160 V
120 V
80 V
40 V
C4
TA
-40 V
-80 V
-120 V
-160 V
-200 V
14.25 V*A
12.75 V*A
11.25 V*A
9.75 V*A
8.25 V*A
6.75 V*A
5.25 V*A
3.75 V*A
2.25 V*A
750 mV*A
-50 mV*A
M1
200 V*A
160 V*A
120 V*A
80 V*A
40 V*A
M2
-40 V*A
-80 V*A
-120 V*A
-160 V*A
-200 V*A
Measure
Current
Max
Min
Mean
RMS
σ (S-dev)
Event count
Wave count
1 M1 CMean
2.66 V*A
2.68 V*A
1.51 V*A
2.67 V*A
2.67 V*A
23.3 mV*A
2599
1161
2 M2 CMean
2.41 V*A
9.25 V*A
-5.27 V*A
2.33 V*A
2.38 V*A
514.56 mV*A
2730
1314
C1- V_in
100 mV/
100 MHz
DC 1MΩ
3.1 V
C2- I_in
400 mA/
100 MHz
DC 1MΩ
RT-ZC20B
1.9 A
C3- V_out
40 mV/
100 MHz
DC 50Ω
RT-ZD40
800 mV
C4- I_out
40 V/
100 MHz
DC 50Ω
RT-ZD10
260 mV
M1
1.5 V*A/
C1*C2
6.75 V*A
M2
40 V*A/
[C3*C4][V*A]
0 V*A
C5
C6
C7
C8
Logic
Math
Bus
Ref
Spec
Gen
Menu

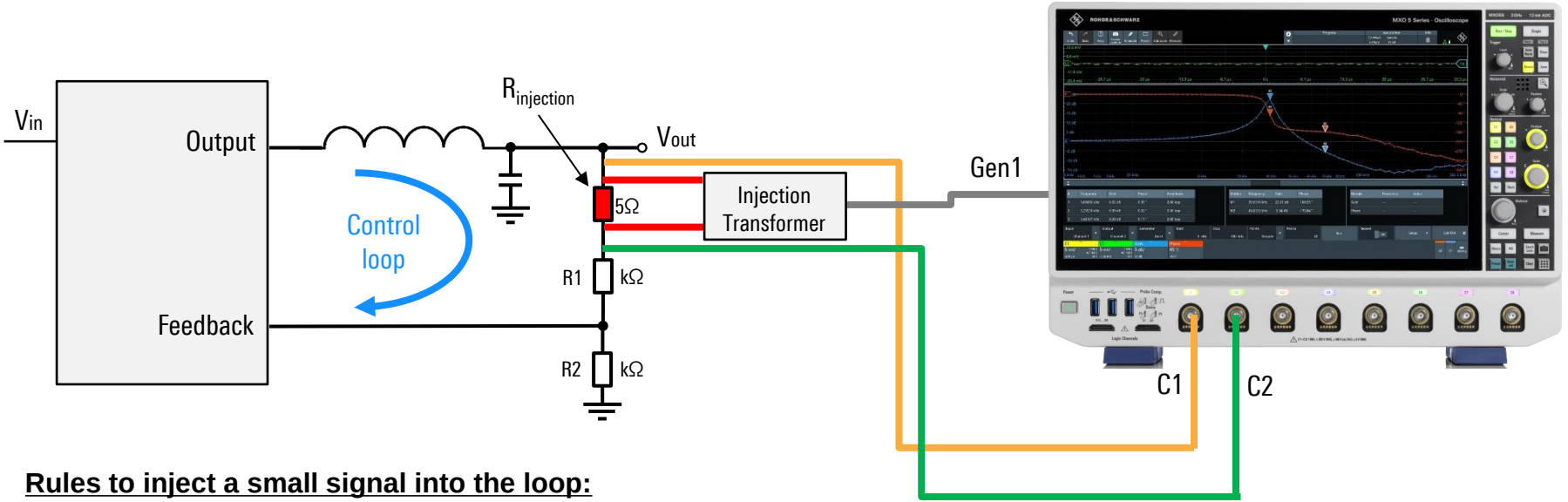
LOAD STEP RESPONSE

VOLTAGE CHANGE RESPONSE TIME

POWER INTEGRITY



CONVERTER STABILITY VERIFICATION



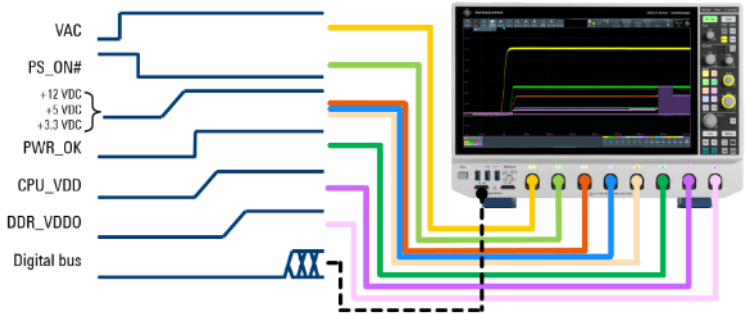
Rules to inject a small signal into the loop:

1. Output impedance of the output stage is much lower compared to the input impedance of the feedback loop
2. Ensure that all relevant components which are part of the loop are included

FREQUENCY RESPONSE ANALYSIS FOR CONTROL LOOP RESPONSE

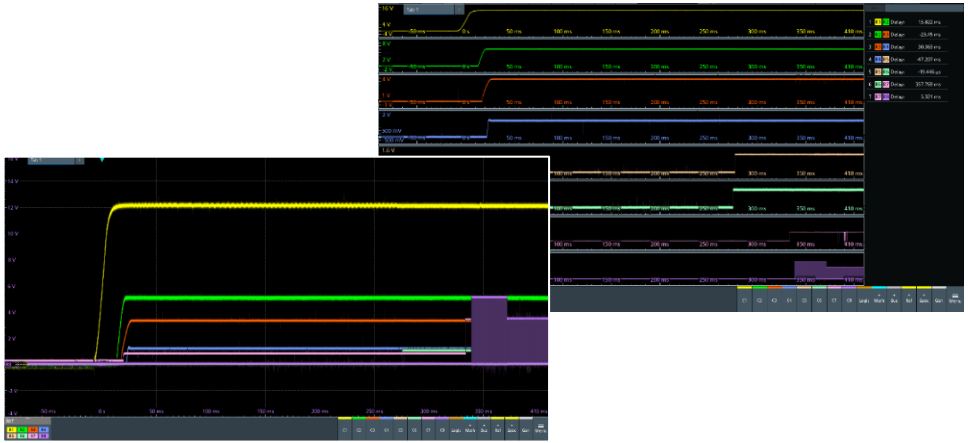
- Bode plot oscilloscope application
- 10mHz to 100MHz
- Custom amplitude profile
- Result table
- Cursor analysis
- Gain & phase margin

VERIFICATION OF POWER SEQUENCING IN POWER DELIVERY DESIGNS WITH MULTIPLE POWER RAILS



Sampling rate	Capture Duration (500 Mpoints)	Capture Duration (1Gpoints)
5 Gsample/s	100 ms	200 ms
500 Msample/s	1 s	2 s
5 Msample/s	100 s	200 s
8 Ksample/s	17h 21m 40s	1d 10h 43m 20s

- Multiple channels to see more events
- Deep record length for longer observations
- Flexible and intuitive waveform setup
- Configurable delay measurement setup



SOC POWER DESIGNS W. MULTI-PHASE BUCK CONVERTERS:

SUMMARY:

- HIGH POWER DEMAND OF HIGH SPEED SOC
- MULTI-PHASE BUCK CONVERTER FOR HIGH CURRENT SUPPLY
- VARIOUS MEASUREMENTS REQUIRED

Find out more

www.rohde-schwarz.com

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Thank you!

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Make ideas real